Manufacturing-friendly curvilinear standard cell design

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ABSTRACT

The integration of curvilinear shapes in semiconductor technology is explored. Curvilinear shapes are classified into forms using Manhattan, rectilinear, and curvilinear representations. The primary objectives of employing curvilinear shapes in Optical Proximity Correction (OPC) and mask technology are identified as error reduction and the effective representation of complex shapes. Leveraging the path optimization characteristic inherent in curvilinear shapes, their utilization was studied for semiconductor layout design. Standard cell design serves as a demonstrative example to highlight these benefits. Using the DTCO Power-Performance-Area-Cost (PPAC) assessment metric, enhancements in both electrical performance and cost efficiency are showcased, compared with designs using Manhattan shapes. We propose a step-by-step adoption strategy of curvilinear design, ranging from restrictive to partial use, and even free-form routing. In addition, we address concerns regarding data volume, outlining how curvilinear representation can effectively mitigate such issues, in OPC, mask technology and layout designs.

Keywords: Curvilinear, OPC, mask, standard cell, design, DTCO, PPAC

1. INTRODUCTION

Recently, curvilinear shape has emerged as a promising technology within the semiconductor industry, and active exploration is currently underway to uncover its potential applications in Optical Proximity Correction (OPC) and photomask technologies [1-2]. The introduction of the multi-beam mask writer (MBMW) in photomask manufacturing has helped to facilitate the integration of curvilinear shapes into practice [3].

On the contrary, their application within semiconductor design remains largely unexplored. Particularly, its incorporation into logic semiconductor design hasn't yet been proactively pursued. This is due to the challenges of nanometer-scale features and handling large data volumes associated with semiconductor design.

This paper aims to report the application and challenges associated with the adoption of curvilinear shapes into logic semiconductor design. We begin with our classification of curvilinear shapes, examining their applications in the OPC and photomask technologies. We then provide analogues of the challenges for implementing curvilinear shape into the technologies. Subsequently, we present our findings of incorporating curvilinear shapes into logic semiconductor design, which has progressively transformed into 1-D Manhattan style. Design Technology Co-Optimization (DTCO) methodology is proposed to be used to demonstrate the figure-of-merit and optimize the curvilinear design. It will be shown that more area-and-cost effective designs are achievable by evading the limitations of traditional Manhattan design.

Finally, we conclude by discussing the future works and envisioning the strategy in implementing the curvilinear design into semiconductor design.

2. CLASSIFICATION OF SHAPES

Shapes are classified into three groups as illustrated in Figure 1.

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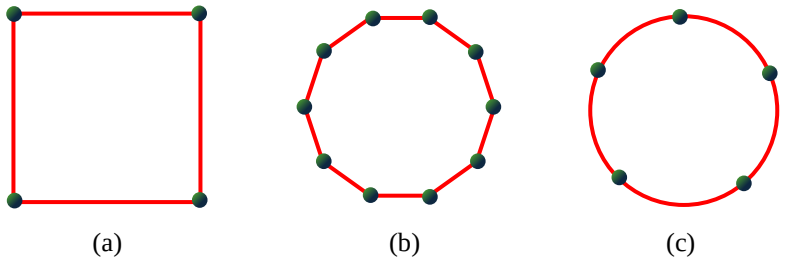


(a) (b) (c)

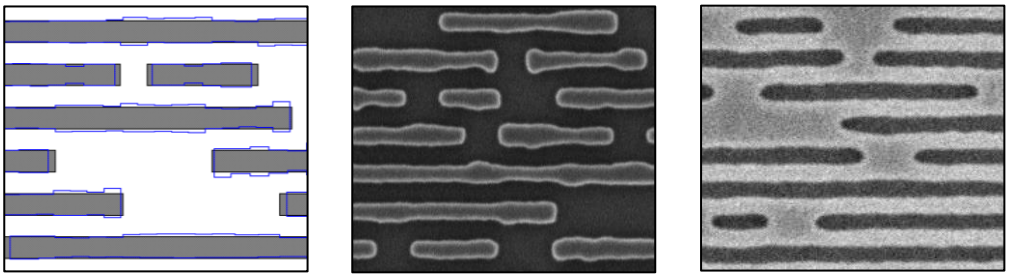
Figure 1. Classification of shapes. (a) Manhattan shape. (b) Rectilinear shape. (c) Curvilinear shape.

A Manhattan shape is distinguished by structures aligned only along vertical and horizontal directions. A rectilinear shape comprises straight lines connecting points at various angles. Conversely, a curvilinear shape incorporates curves to connect points, and curvilinear data representations such as Bezier and B-Spline are utilized to represent curves [4]. Regarding data volume, a Manhattan shape typically employs two coordinates, such as lower left and upper right in Cartesian coordinates. In contrast, representing a curved shape with a rectilinear representation involves approximating the curve using multiple straight-line segments, with two coordinates for each straight-line segment. Increasing the number of segments is necessary to minimize the error between this approximated shape and the curved intent. The permissible error between the approximated shape and the curved intent determines the data volume. A curvilinear shape, in contrast to Manhattan and rectilinear shapes, utilizes control points and curvilinear representations between two control points. Control points are not necessarily placed on the curvilinear intent. More control points are required to accurately approximate the design intent. Curvilinear shapes can be approximated through Manhattan, rectilinear, and curvilinear representations. The data volume increases in direct proportion to the number of coordinates or control points employed.

3. EXPLORING CURVILINEAR SHAPE IN OPC AND PHOTOMASK

Curvilinear shapes are explored in OPC and photomask technologies to offer two key benefits: error reduction or complex shapes representation.

Firstly, curvilinear shapes can be employed to reduce errors that occur during the transfer of Manhattan-shaped designs through manufacturing processes. Figure 2 demonstrates the errors that appear in the mask and wafer fabrication processes. A logic metal design of 32-nm pitch experienced Manhattan OPC, mask fabrication using e-beam and photolithography process using NA0.33 EUV to fabricate the wafer. In Figure 2 (a), the Manhattan design intent is superimposed with the post-OPC output. Both design and OPC were conducted using Manhattan shapes. Figure 2 (b) displays the photomask CDSEM image corresponding to the post-OPC output, while Figure 3 (c) presents the printed wafer image corresponding to the design and the mask.



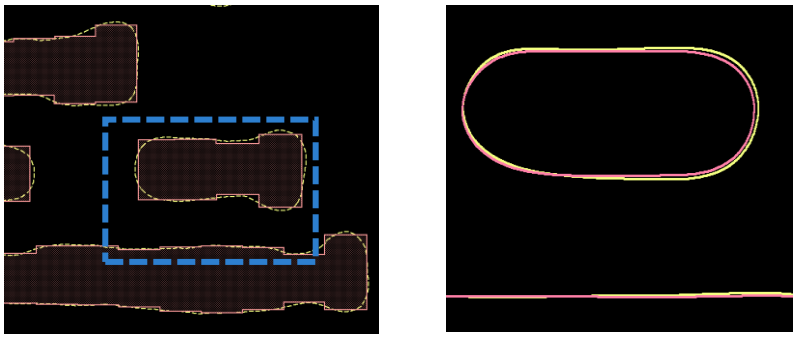
(a) (b) (c)

Figure 2. Logic metal layer of 32-nm pitch. (a) Design intent (solid) overlapped with post-OPC output layout (empty). (b) CDSEM image of photomask fabricated using the post-OPC shape shown in (a), exhibiting corner rounding. (c) CDSEM image of printed wafer that experiences severer corner rounding.

As shown in Figures 2 (b) and (c), designs initially featuring Manhattan geometry end up with rounded corners. It is because both e-beam and NA0.33 EUV photolithography are subject to bandwidth constraints and exhibit low-pass filter characteristics. This leads to the loss of high-frequency information from the original designs when they are transferred through the photolithography and photomask fabrication systems. Since the wavelength of the photolithography (λ =

13.4nm) is longer than the e-beam used for the mask fabrication, the corner rounding appearing in the photolithography process is severer.

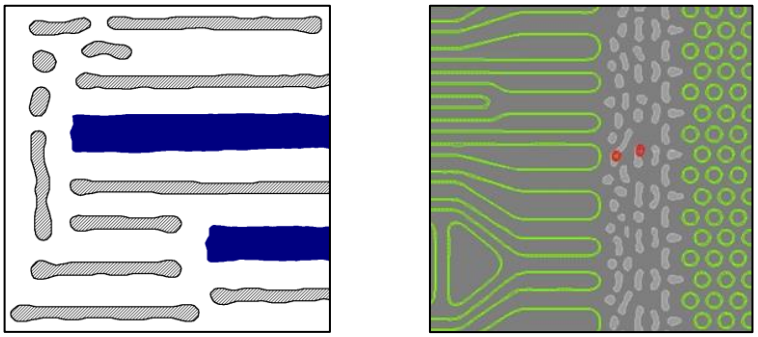
To assess the impact of mask corner rounding, simulations were conducted comparing the aerial images from both the post-OPC layout (Manhattan) and the corner-rounded mask image. The mask image was extracted using the mask CDSEM. Figure 3 clearly shows the discrepancies, revealing errors evident in the comparison of simulated aerial images. Quantitatively, for the selected geometry of target CD 16-nm, 0.7-nm error was observed. It's worth noting that subsequent processes in the lithography process may further influence the error.



(a) (b)

Figure 3. Comparison of aerial images between Manhattan OPC output and actual photomask contour that experiences corner rounding. (a) Manhattan OPC output (solid lines) is superimposed with photomask contour (dotted curvy lines). (b) Overlayed simulated aerial images between the two within the thick dotted box in (a) shows 0.7-nm error.

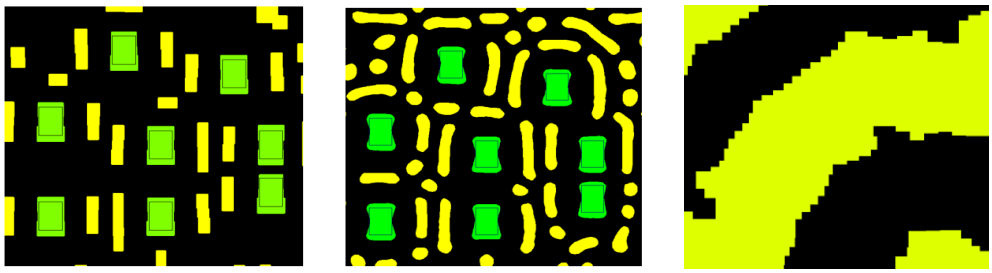
Figure 4 provides OPC and mask design of the effort to reduce the error by using curvilinear shapes. In Figure 4 (a), curvilinear assist features are used with curvilinear design, and Figure 4 (b) showcases Inverse Lithography Technique (ILT) on curvilinear DRAM design, applied to mask fabrication.



(a) (b)

Figure 4. (a) Curvilinear OPC output GDS of logic metal layer for design (solid blue) and assist feature (shaded grey). (b) Photomask CDSEM overlaid on a curvilinear DRAM design (green).

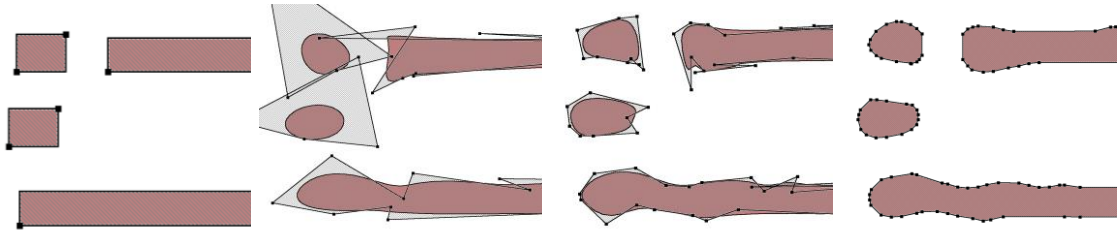
Secondly, curvilinear shapes can be used to represent complex geometry. Figure 5(a) depicts a random logic via layout experienced Manhattan OPC including Manhattan sub-resolution assist features (SRAF). Curvilinear OPC utilizes curvilinear shapes to generate more complex geometries to enhance the lithographic process window (Figure 5(b)). In this scenario, rectilinear curvy representation is utilized. Figure 5(c) depicts an approach to using Manhattan primitives to represent complex curvilinear geometry. Notably, each design grid in Figure 5(c) converted to Manhattan geometry to approximate the curvilinear geometry, and this results in a substantial increase in data volume. Employing curvilinear shapes intends to directly mitigate this issue.



(a) (b) (c)

Figure 5. (a) Manhattan OPC with Manhattan SRAF of random logic via. (b) Curvilinear OPC. (c) Manhattan representation of complex geometry.

While curvilinear shape shows its potential as shown above, the industry remains concerned about the increase in data volume and the challenges associated with handling the large data. Figure 6 depicts a comparison of the data volume linked to curvilinear geometries, utilizing a corner of the SRAF design appearing in Figure 4 (a).



(a) (b) (c) (d)

Figure 6. Data comparison among Manhattan and other curvilinear representations. (a) Manhattan shape (6 data points). (b) B-spline (26 control points). (c) B-spline (48 control points). (d) Rectilinear representation (90 data points).

Each data point or control point translates into a coordinate and the number of coordinates directly impact the data volume. Compared with the rectilinear representation, which employs 90 data points, B-spline curves utilize fewer data points, with 48 and 26 control points. Manhattan shape can use only 6 data points. Simplifying the curvilinear format with a smaller number of control points reduces data volume. However, this simplification will introduce an increase in errors between the rectilinear intent and simplified representations.

4. EXPLORING CURVILINEAR SHAPE IN SEMICONDUCTOR DESIGN

Expanding focus of curvilinear utilization

In employing curvilinear shapes within OPC and photomask technologies, the primary focus is on minimizing error and representing complex shapes using the flexibility of curved geometries. We propose expanding the focus to include path representation for semiconductor design.

In semiconductor technologies, circuit design is physically implemented through layout design. Transistors are electrically interconnected with metal wires and vias within standard cells and among standard cells by place-and-route (PNR) designs. Routing wires in the layout design plays a critical role in the electrical performance of the circuit, aiming to establish connections between transistors with the minimum wiring path length to reduce signal delay. Utilizing curvilinear paths offers benefit as it can provide an alternative, shorter path when a direct and unbent path is obstructed. This concept can be likened to real-world logistics, where the objective is to determine the most efficient transportation route, as observed in trucking and shipping operations. In scenarios where a direct path is blocked by an obstacle, curvilinear paths allow for alternative paths with the shortest travel distance.

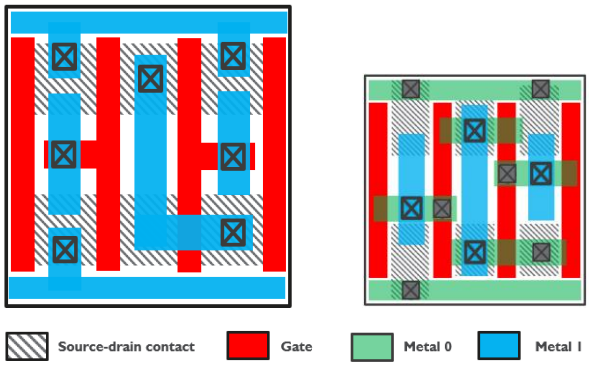
Curvilinear design philosophy and its implementation

We advocate for continuing the use of the Power, Performance, Area, and Cost (PPAC) metric to assess the effectiveness of curvilinear design, in line with the figure of merit of DTCO study. Historically, the PPAC optimization closely aligned

with the industry's effort of continually increasing transistor density. Optical scaling initially drove the trend, and the semiconductor industry shifted its focus toward design scaling combined with continued optical scaling.

Optical scaling primarily leverages photolithography to decrease the minimum feature size to increase transistor density. Central to this method is Rayleigh's law: $P/2 = k_1 * \lambda/NA$, where P represents the pitch of the minimum feature, k_1 refers the process coefficient, λ denotes the wavelength of light, and NA refers to the numerical aperture of the photolithography system optics. In general, optical scaling based on λ/NA reduction offers omni-directional pitch scaling. However, optical scaling through k_1 reduction beyond allowable 2-D (also known as bidirectional) design-limit demands design style modifications into 1-D (also known as unidirectional) design. 1-D design separates vertical and horizontal wiring into distinct layers, necessitating increased photomasking layers and advancements in the patterning process. To achieve further reduction in k_1 beyond the lithographic resolution limit of 1-D features, multiple patterning techniques must be employed. In summary, shifting from 2-D to 1-D, transitioning from a single patterning solution to multiple patterning solution results in an escalation in the number of photomasks and process steps. This directly influences the cost and potentially the design area, a key metric in DTCO analysis.

Figure 7 illustrates the design style advance in a standard cell by reducing k_1 of a metal interconnect layer, while maintaining λ/NA constant. As described, reducing cell height for area reduction involves transforming the metal design from 2-D to 1-D. This necessitates the addition of an extra metal layer. Metal 0 and Metal 1 layers are utilized to complete 1-D design in Figure 7 (b), while only Metal 1 is needed to complete the standard cell design in Figure 7 (a).



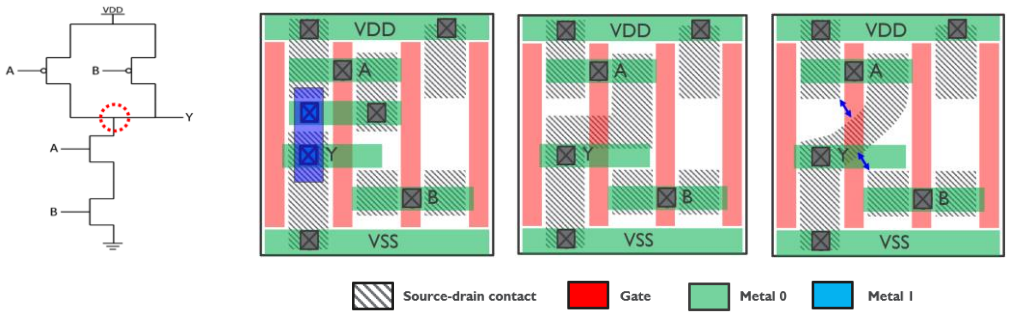
(a) (b)

Figure 7. Illustration of standard cell layouts. (a) 2-D cell level routing using Metal 1. (b) 1-D cell level routing with Metal 0 and Metal 1.

The evolution of design styles presents a challenge when it comes to curvilinear design. As curvilinear shapes naturally adopt a 2-D form, their incorporation in routing can adversely impact the optical scaling using k_1. Thus, careful optimization is necessary to prevent an increase in k_1. Previous report has addressed the implementation of curvilinear design in standard cell layout without compromising k_1 [5]. It was reported that the standard cells using curvilinear shape exhibit reduced total metal length, decreased number of vias, and eliminated the need for an extra metal layer when compared to 1-D Manhattan-only standard cell designs.

Compared with optical scaling, design scaling involves optimizing the design to enhance the transistor density within a specified area, with or without utilizing optical scaling techniques. The term DTCO encompasses the design scaling effort used with the patterning scaling booster technologies, often referred to "DTCO special architectures" [6].

Contemplating design scaling through path optimization concept, curvilinear design can be classified into three categories based on its level of utilization and technology readiness. Initially, there is the "restrictive use" scenario, wherein curvilinear shapes are employed in a constrained manner. Figure 8 illustrates this scenario using a NAND gate standard cell design. For visual clarity, the active layer is omitted in completing the cell designs.



(a) (b) (c) (d)

Figure 8. Illustration of the limited use of curvilinear shape. (a) Schematic circuit diagram of a NAND gate. The dotted circle indicates the electrical connection where the curvilinear shape is employed. (b) Standard cell design layout using Manhattan 1-D shape. (c) Standard cell design layout using Manhattan 2-D shape. (d) Standard cell design layout using curvilinear shape. Curvilinear design is utilized in source/drain contact (shaded).

The NAND gate necessitates an electrical connection between the drains of the PMOS and the NMOS to produce an output Y. Employing a curvilinear design facilitates a direct connection between the drains (Figure 8 (d)), combined with a gate-pass-through scaling booster. It is used to guide the wiring through the gate. It effectively avoids design rule violation by using corner-to-corner space check instead of line-to-line space violation appearing in Figure 8 (c). Corner-to-corner space rule is smaller than line-to-line space rule in general. As a result, the utilization of direct drain-drain connection allows sparse utilization of metal 0 routing resource to provide an opportunity to further reduce the cell height and eliminate the need of Metal 1 layer.

Subsequently, “partial use” scenario can be considered. The incorporation of curvilinear design takes on various forms while satisfying existing manufacturing environments. Current electronic design automation (EDA) tools can be used. In this scenario, conventional design rules and design rule checks (DRC) are applied. The specifics of the design procedure, physical verification, and manufacturability check are reported elsewhere [5]. In the report, curvilinear design is employed to decrease the total metal length, thereby obviating the necessity for additional metal layers and vias. The dimensions of the cell, including height and width, remain consistent with those of conventional 1-D Manhattan designs.

Figure 9 demonstrates several standard cell layouts from this approach. For visual clarification, only Metal 0 layer and Metal 1 layer are shown.

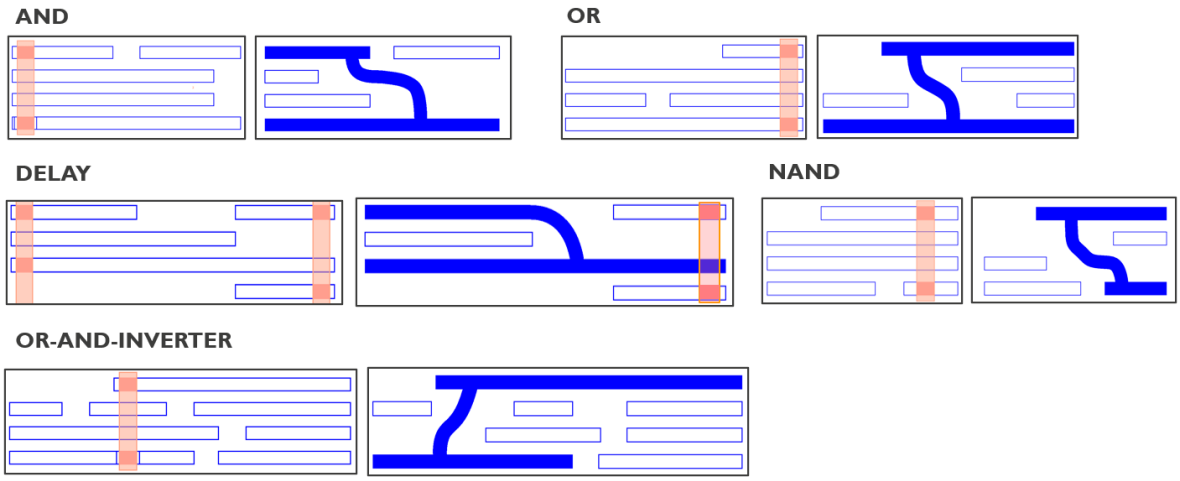


Figure 9. Curvilinear design implementation of Metal 0 layer of standard cell layouts (solid lines). Some designs exhibit the use of Metal 1 (vertical Manhattan shapes). For each logic gate, 1-D Manhattan design is compared (left) with curvilinear design (right) side-by-side.

AND, OR, DELAY, NAND, and OR-AND-INVERTER logic standard cells used curvilinear design. A side-by-side comparison with 1-D Manhattan design highlights the potential elimination of the Metal 1 layer and accompanying vias. The benefits of the curvilinear design are evident in the illustrated examples. In realizing the curvilinear design, B-spline curve representation is employed. The number of control points were restricted within 12, effectively reducing data volume. Other than the curvilinear shape, Manhattan shapes are used.

Ultimately, curvilinear design offers the possibility to route the wires in a “free form” manner. Achieving this necessitates fully enabled EDA solutions with advancements in design methodologies. Specifically, increased computational power and leveraging Artificial Intelligence (AI) may be essential to accommodate the increased degree of freedom in design.

When examining the power and performance implications of curvilinear design, it is advisable to perform analyses at the system level. In other words, analyses should encompass either IP or chip level evaluations, integrating curvilinear design into standard cells and conducting PNR with fully interconnected metal layers [7]. As a result, system-level evaluation was not included in this study, and it will be addressed in our future work.

5. CONCLUSION

We present our investigation of curvilinear shapes for adoption in semiconductor technology. The shapes are categorized into Manhattan, rectilinear, and curvilinear forms. Error reduction and the representation of complex shapes are major focuses when employing curvilinear shapes in Optical Proximity Correction (OPC) and mask technology. It is shown that curvilinear representation can effectively reduce errors and represent complex shapes with reasonable data volume compared to Manhattan and rectilinear representations. By utilizing the path optimization characteristic of curvilinear shapes, investigation into semiconductor layout design demonstrates its potential. The Design Technology Co-Optimization (DTCO) PPAC metric is proposed to assess its value. Careful optimization was made to maintain k_1 similar to the k_1 from Manhattan 1-D design while enhancing electrical performance, power efficiency, and reducing costs. Considering its maturity, curvilinear design is proposed for adoption in restrictive, partial, and free-form routing applications.

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