Low Landing Energy as an Enabler for Optimal Contour Based OPC Modeling in the EUV Era

Ran Alkoken*[a], Mor Baram[a], Gadi Oron[a], Nivea Schuch[b], Frederic Robert[b], Thiago Figueiro[b], Omri Brand[a], Matan Geta[a], Kasturi Saha[a], Elias Miller[a], Tal Zavhon[a], Dipayan Tiwari[a], Deepakkumar Singh[a], Sujan Kumar Sarkar[c], Paulina Delgadillo[c], Gian Lorusso[c], Christophe Beral[c], Chih-I Wei[f], Gabriel Curvacho[f], Young Chang Kim[d], Germain Fenger[e]

(a) PDC business group, Applied Materials, Rehovot, Israel
(b) Applied Materials, 4 place Robert Schuman, 38000, Grenoble, France
(c) imec, Kapeldreef 75, Heverlee, Belgium 3001
(d) Siemens EDA, 46897 Bayside Pkwy 200, Fremont, United States
(e) Siemens EDA, 8005 Boeckman Rd, Wilsonville, United States
(f) Siemens EDA, Interleuvenlaan 68, Leuven, Belgium

ABSTRACT

OPC (optical proximity correction) is a well-known and widely used RET (resolution enhancement technique) in optical lithography, which main purpose is improving pattern fidelity and process window. OPC relies on CD-SEM (critical dimension scanning electron microscope) images as a source of information for EPE (edge placement error) measurement, as input for the OPC modeling flow. However, as the pitch scales, stricter OPC modeling specifications, reduced metrology error budget, and increasing pattern complexities, create challenges for traditional CD-SEM metrology. Also, parameters like materials, landing energy and other scanning conditions, may have a different impact in the final image in terms of shrinkage, charging and distortion. All these effects need to be characterized during the modeling step to optimize OPC. Examples of EPE uniformity and pattern shrinkage are illustrated in Figure 1, for different scan conditions.

With the increasing adoption of EUV (extreme ultraviolet) technology in the field of patterning and the upcoming introduction of High-NA (high numerical aperture) EUV, the need for further understanding of the EUV resist material interaction with a CD-SEM electron beam is also increasing [1]. Low landing energy scanning approach is a way to minimize EUV resist damage during image acquisition and provide a more accurate view of EUV lithography effects [2].

Also, to improve the design space coverage, resist (or lithographic) and etch modeling require thousands of measurements over different types of structures. Additionally, massive EPE statistics makes model building more robust [3]. A contour may provide the equivalent of hundreds of different measurements – using the entirety of the contour instead of only relying on the placement of gauges, as in conventional measurement, further increases the sampling and the coverage of the produced model, which make contours the suitable choice [4,5]. The influence of low landing energy is expected to be seen in the etch modeling step, where it should have higher accuracy and lower etch bias when compared to litho SEM data. However, a drawback of using low landing energy for image acquisition is a lower SNR (Signal-to-Noise ratio) compared to standard imaging conditions. This may represent extra challenges to the contour extraction algorithm which needs to be robust. These challenges can be addressed by using a model-based approach [6,7].

In this work, different CD-SEM scanning conditions were studied in order to find optimal working points for modeling purposes. Since different patterns have varied outcomes under different e-beam conditions, thus affecting the model residues, more than 600 distinct patterns from EUV lithography – going from 1D to complex 2D – were selected to provide enough sensitivity to when building the litho and the etch models. Contour metrology is used to detect the edges, for EPE analysis, and to provide inputs for the modeling flow. At last, one of the key aspects of this work is the use of low landing energy (150eV) scan approach to minimize the resist shrinkage effect, while accounting for resist charging in the modeling. All these factors will provide further insight and optimization into this new era of metrology.

Metrology, Inspection, and Process Control XXXVIII, edited by Matthew J. Sendelbach,
Nivea G. Schuch, Proc. of SPIE Vol. 12955, 1295516 · © 2024 SPIE
0277-786X · doi: 10.1117/12.3010898

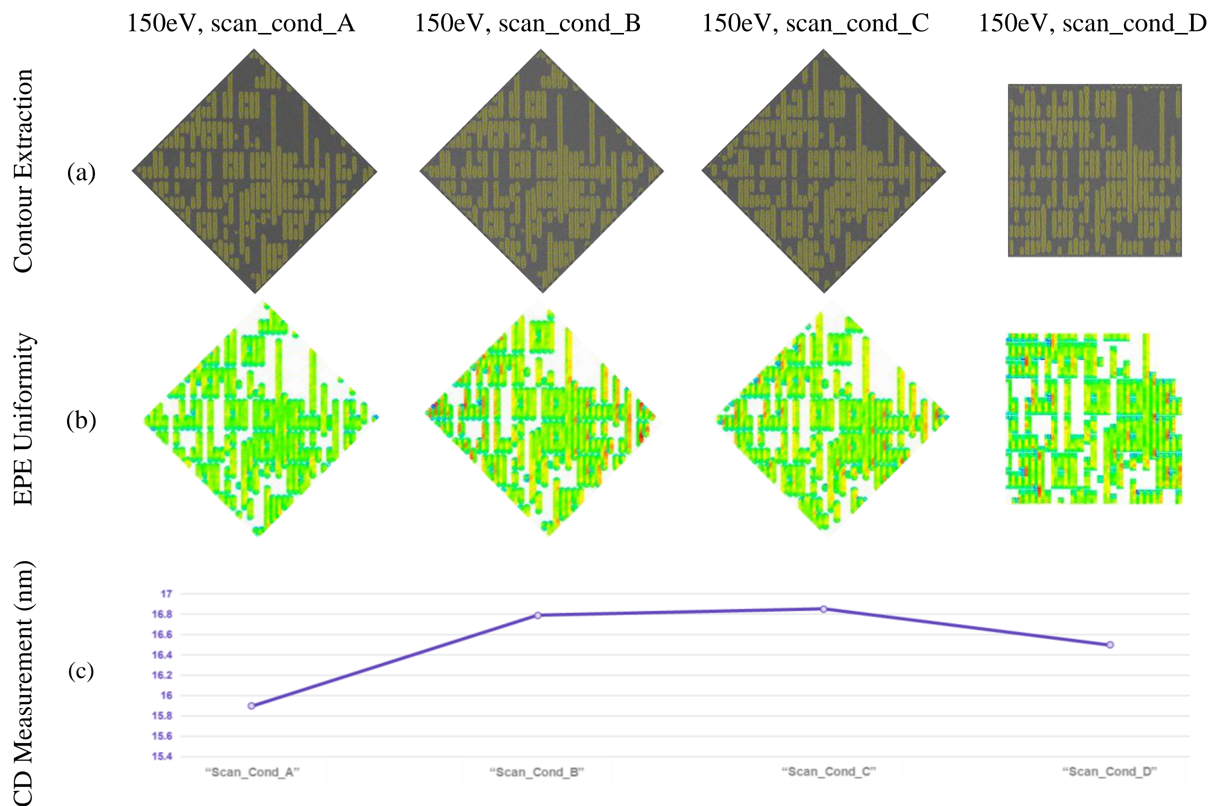


Figure 1: This figure illustrates the impact of different scan conditions being applied to the same pattern. The images were acquired at low landing energy (150eV), over 10 different die. Also, they were acquired from different locations of the die, to avoid multiple exposures while keeping same process variation. In a), the extracted contours are shown for a single die. In b), the EPE uniformity is analyzed over the average contour from the 10 die. The coloring represents the distance of the contours compared to the intended layout. The closer the color is to 'green', the closer the contour is to the intended layout. When color goes to 'red' or to 'blue' it means the extracted contour is farther to the target design – red means the extracted contour is 'external' to the intended design, while 'blue' is 'internal'. From the illustration it is possible to see that, depending on the scan conditions, 'higher' or 'lower' EPE uniformity can be observed. In c), the CD measurement is presented for the different scan conditions, showing that the scanning parameters (other than the landing energy) also influence the pattern shrinkage. The patterns under measurement are trenches, which means that smaller CD values indicate less shrinkage. In the illustrated example, "Scan_cond_A" presents less shrinkage and better EPE uniformity compared to the other conditions.

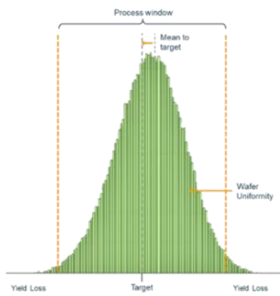
Keywords: Low Landing Energy, EUV, High-NA, CD-SEM, OPC, Contour Metrology

1. INTRODUCTION

1.1. Patterning control playbook

When looking into controlling the process window there're two areas to focus on. First, the traditional process control approach, centering the process histogram to the target. This application drives tight matching and high sensitivity to enable process centering to the fraction of nm. Second is the variation control reflecting yield. In order to capture the yield loss area, increase in statistics is mandatory to have better prediction of process variation and control.

Set the wafer pattern on target



Minimize and control variation and cross layer alignment

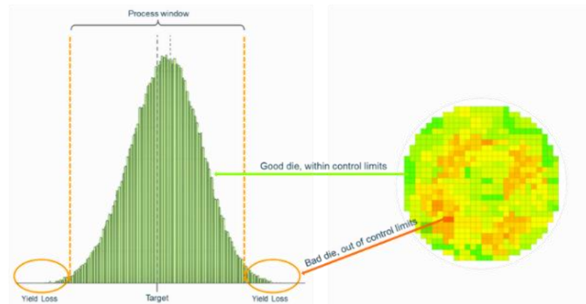


Figure 2. Controlling The Patterning Within the Process Window

1.2. Keys to Enable EUV Metrology

In recent years, high focus was put into defining the optimal conditions for EUV metrology. The first module that was defined was related to the imaging of thin resist (30-60nm) looking ahead towards possible insertion of even thinner resist (10-30nm) with the introduction of the 0.55NA EUV scanner. The methodology [1] to define the optimal EUV metrology takes into consideration the metrology bias (resist shrink) as key factor without compromising on other critical metrology parameters such as image quality (Contrast to Noise, Sharpness), roughness sensitivity while meeting precision and matching in high volume manufacturing.

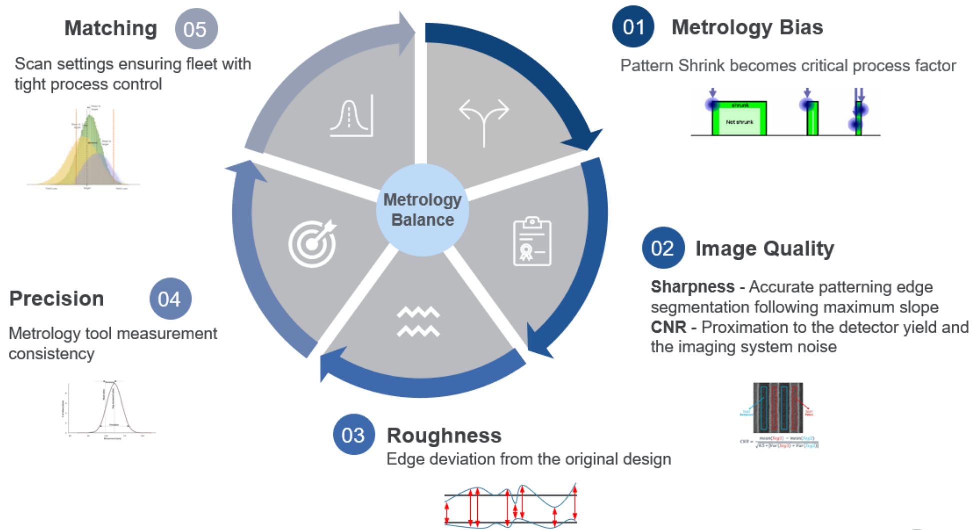


Figure 3. Metrology Balance Methodology

Once the Metrology balanced condition obtained, implanting them for the next phases in the definition of EUV metrology - true process window characterization and accurate robust OPC modeling.

The first step in the methodology process begins with simulation, higher landing energy generates bigger interaction volume between the resist and the eBeam which in return results in severe resist deformation and shrinkage. This phenomenon is intensified once moving to thinner film thickness.

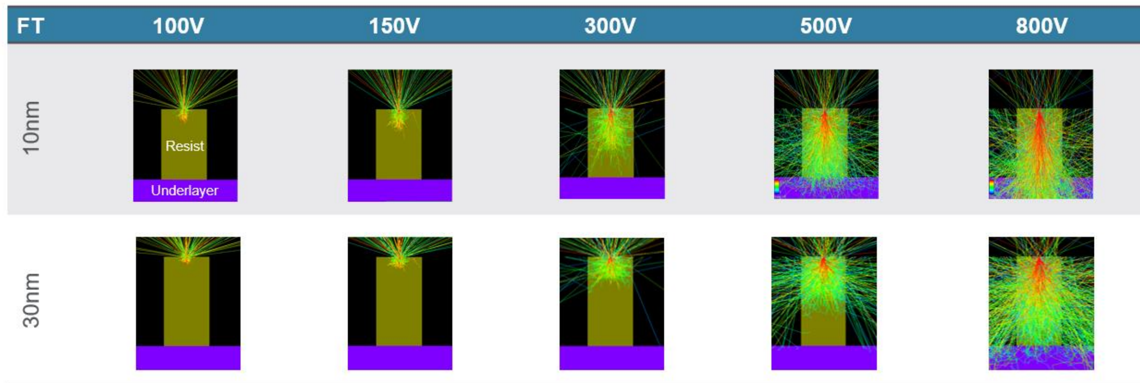


Figure 4. Monte Carlo simulation on different film thickness and landing energies.

Going down in landing energy help to better control the interaction volume of the eBeam and the question on where the optimal point per each stack is, was determined within the next steps of the methodology. Higher landing energy increases the resist shrink and affect the CD data integrity. Lowering the landing energy can reduce the shrinkage, however, below a certain point, local electrical field becomes more dominant. This process needs to be optimized per stack and not to be a pre-defined selection. For most of the stack that we observed [1]
the 150V was found to be the balanced metrology conditions which eventually was selected for the focus of this study which is implementing the best condition for the OPC modeling.

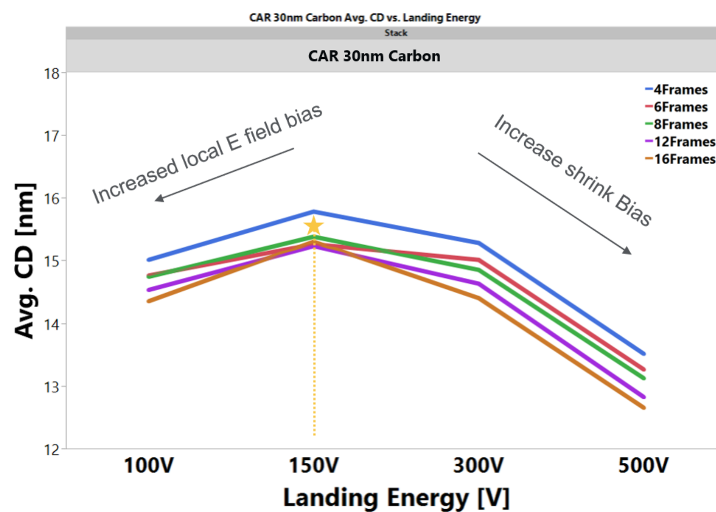


Figure 5. Recap on selecting the balanced metrology.

1.3. Patterning OPC Application Space

The patterning OPC application is divided into two focus area which drives different architectural requirements. Our focus for this study will be the OPC modeling which needs higher sensitivity, tight matching between the OPC modeling recipe to in line recipe and implementing the balanced metrology for the EUV metrology. Both applications need the support of contour-based metrology.

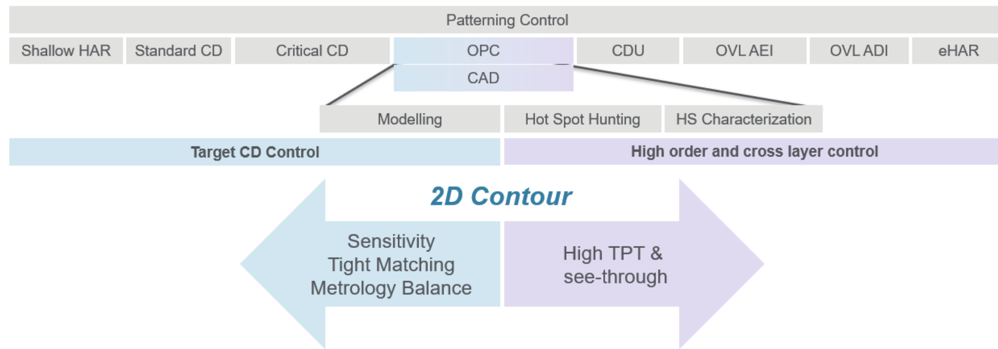


Figure 6. Patterning OPC application Space

1.4. Contour-based OPC Modelling

Traditionally, OPC modeling is relying on CD gauge measurements coming from a CD-SEM image. In this approach, OPC modeling usually requires thousands of measurements over different types of structures. This usually provides limited information for the modeling process. In order to produce more information for the modeling flow, a larger variety of patterns are required and this comes with the cost of increasing image acquisition time (as more images are required) as well as the modeling time. Moving to full contour can cover all edges which results in maximal information content that can be harvested. This approach allows to select high pattern information density, reduce the calibration computational load and lower down the metrology cost.

Extracted contours may be aligned to CAD in order to perform measurements. This enables a massive distance-from-design (DFD) statistics that makes model building more robust [3]. Figure 7 illustrates the measurement of distance-from-design over 2D features. A single contour may provide the equivalent of hundreds of different CD measurements. Moreover, by using contours for calibrating the model, the reproduction of 2D features, corners and line-ends is improved [3]. Those areas are the most sensitive to stochastic effects.

Another approach relies on using directly the contours to represent the aerial image of the simulated OPC model. This enables even further model coverage and even richer information for the OPC modeling flow. On those cases, often average contours are used as a way to mitigate stochastic effects in order to better capture the process systematic signature.

Using contours for OPC modeling, besides improving overall results, may also enable reducing the number of SEM image acquisitions required. This may be obtained by selecting patterns with higher complexity. In this way, a single image containing a complex pattern may provide much more information as compared to multiple images of CD, space and densities configurations. Moreover, by using more complex patterns and, for this reason, being able to reduce the total number of patterns, one may reduce overall cycle time by reducing number of image acquisitions, and also computational cost of the model calibration process [6].

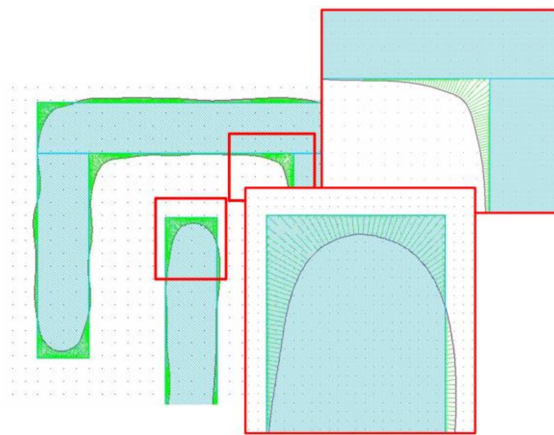


Figure 7. Contour (purple) and CAD layout (light blue) overlapped, and the distance-from-design measurement gauges (green arrows).

1.5. Contour-based OPC Modelling utilizing Low Landing Energy

One important aspect when providing information to the OPC modeling flow is how accurately they represent the phenomena the model intends to represent. This, of course, depends on the quality of the measurement or contour extraction algorithm used, obtaining the most accurate information from the data available on the SEM images. Another important aspect is the impact of the image acquisition over the sample. OPC modeling often relies on SEM images acquired over resist, which is very sensitive to the energy used for the image acquisition.

One may improve the pattern segmentation and measurement by providing very high quality SEM images. This is often obtained by the quality of the sensors on the CD-SEM tool but also by adjusting the acquisition conditions such as number of frames, acceleration voltage, current density and so on. Those adjustments allow to significantly improve signal-to-noise ratio (SNR) but also may lead to damage of the sample (e.g. resist shrinkage) for more sensitive materials. This damage is not uniform but rather dependent on the pattern structure, dimension, and density. As previously discussed, looking only on CD shrink in the OPC modeling results in limited information. Moving to contour-based OPC modeling also helps to more accurately quantify the resist shrink in inner and outer corners as well as in line-ends. Overall, this enables better prediction of the material behavior without the SEM image effect and, therefore, better OPC modeling.

Finally, better than estimating the damage and handling it is to first minimize as much as possible. For this reason, adopting acquisition conditions that have less impact over the observed structures is paramount. One way of improving the resist shrinkage is to reduce the total energy used for acquiring the SEM images by, for instance, reducing the acceleration voltage. Figure 8 shows the difference in the contours obtained over a SEM image acquired at 500V and another at 150V. Notice the significant dimensional change between the two patterns. However, the reduction on the shrinkage comes with a cost on the SNR of the image, increasing the importance of the algorithms used for performing pattern segmentation in order to provide the best information possible for the OPC modeling flow.

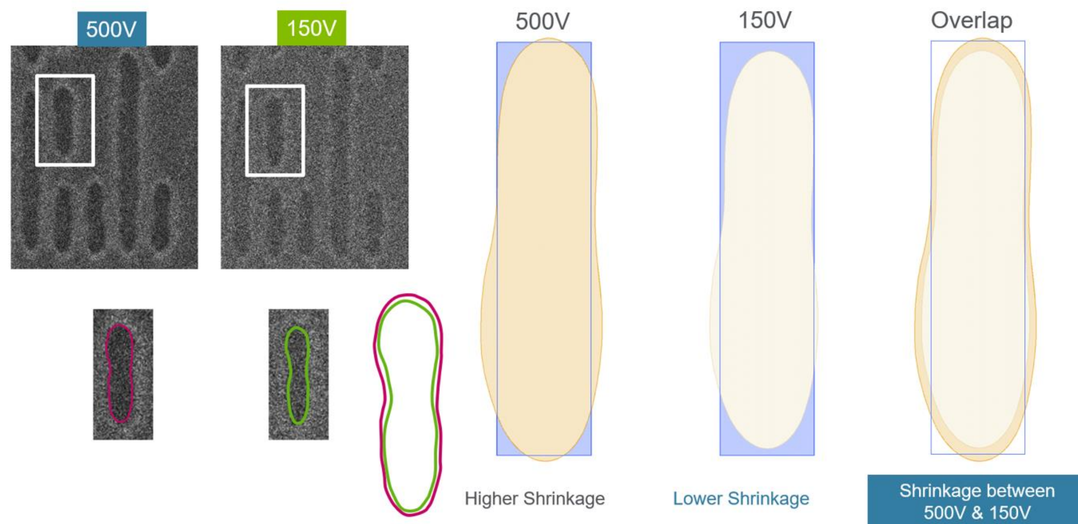


Figure 8. Contour extraction and shrinkage comparison between images acquired using acceleration voltage of 500V and 150V.

2. EXPERIMENT

2.1. Sample Set Definition

The layout and features chosen for this project came from IMEC iN3 BEOL design. The lithography process used an EUV CAR (chemically amplified resist) with PTD (positive tone development) and was illuminated with the OSCAR2 curvilinear mask provided by IMEC with post SMO done by Calibre RET Selection^{TM} based on a vertical dipole source shape optimized for pitches 32nm to 45nm.

The DOE (design of experiments) utilized a total of four wafers, two specified for litho conditions and two for etch, being one of each for nominal condition exposure and one for process window targeting. Seven different locations for each feature were specified as: the center location is designed for nominal condition targeting in the nominal wafer, and first process window condition in FEM (focus exposure matrix) wafer, and six other locations were set around the center with 2um afar in the x direction, y, or both, for no interactions between the SEM image conditions. The nominal wafer used locations 2 through 7 to optimize the eBeam scan conditions, while the FEM wafer had each location on different dies, which were submitted under different exposure conditions.
In the nominal wafer 50 features were chosen, and the FEM wafer had 42 locations chosen.

Layer type	Target type	Number of targets	Number of repetitions	SEM Landing Energy (eV)
Litho CDU	1D Features	50	10	500, 150
Litho CDU	2D Features	42	10	500, 150
Etch CDU	1D Features	50	10	800
Etch CDU	2D Features	42	10	800

Table 1. 4xOPC wafer, 2 post-litho and 2 post-etch

2.2. Source Mask Optimization

Based on the IMEC lithography process, the freeform source is optimized by Calibre RET Selection™ with the evaluation matrix of process window band width, Error per Edge (EpE) in nominal condition, mask error enhancement factor (MEEF) and normalized image log slope (NILS). By changing the location and intensity of each illuminated pixel in the pupil, the final optimized freeform source can find the best balanced among all evaluations in the matrix along with curvilinear mask globally.

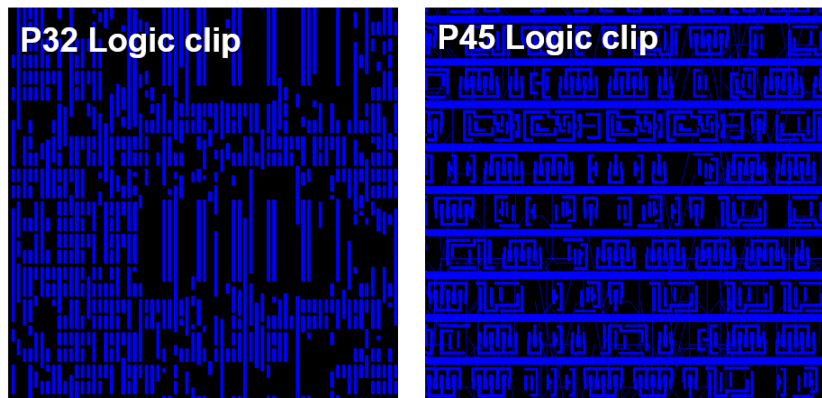


Figure 9. The example of optimized designs. Smaller clips size of several hundred nm width is made after pattern selection procedure.

In this practice, the EUV mask tonality is dark field with standard Ta-based EUV mask film stack. Also, the resist and developer (CAR and PTD) are applied in simulation. The process variation band (PVB) conditions are focus from -30nm to 30nm with a 15nm step; exposure latitude percentage (EL%) from +5% to -5% with a 2.5% step; and global mask bias +0.25nm to -0.25nm with a 0.25nm step. Meanwhile, we mainly focus on IMEC iN3 BEOL metal-like logic design with the pitches 32nm, 34nm, 36nm to 45nm in vertical orientation. Figure 9 shows examples of logic features per pitch used

in the experiment, the total number of 45 smaller clips with both 1D through pitches and 2D designs are considered in the simulation.

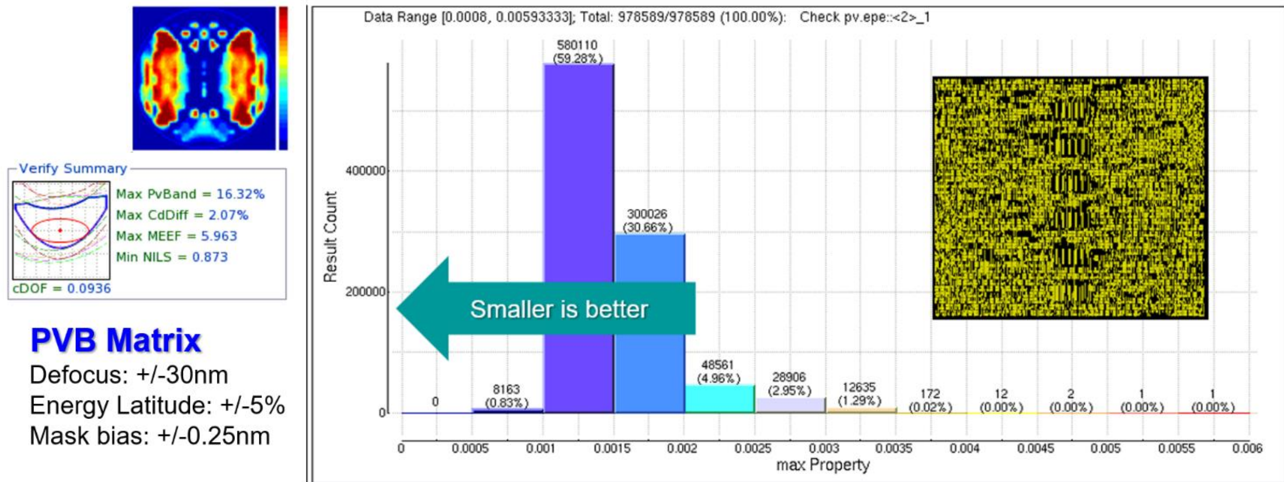


Figure 10. left hand plots show continuum spectrum illumination shape, cDoF plot and PVB conditions. In the right-hand chart, it shows the PVB widths distribution over all sites in P32 logic full clip.

After the optimization, the freeform illumination can reach a good common Depth-of-focus (cDoF) larger than 90nm with <10% CD variation criteria in EUV center slit optical simulation. The source is rendered into pixel shape before place into the EUV scanner. The 32nm logic full design also put into simulation with PVB width checking in Calibre OPCVerify^{TM}. The verification result shows PVB width distribution in figure 10. The left-hand intensity plot shows the continuum spectrum illumination shape (before source rendering); below, bossing plots with cDoF and PVB conditions which are used during source optimization and verification. In the right-hand side, it shows the PVB widths distribution over all sites in P32 logic full clip. In the 99.9% of all inspected edges, they show < 3.5nm PVB width. This source matches the criteria of fine wafer printing.

2.3. OSCAR2 OPC Modeling Sample

After the source was installed and the wafer exposed, the next step was to determine the OPC model sampling plan. In IMEC full curvilinear test vehicle, OSCAR2, there are regular 1D through-pitch Line-Space (LS) arrays from pitch 32nm to isolated pitch 320nm and 2D post-OPC BEoL designs. Post-OPC pattern was used on various design pitches from 32nm to 45nm. For wafer metrology, 50 1D LS patterns and 42 2D clips have been selected.

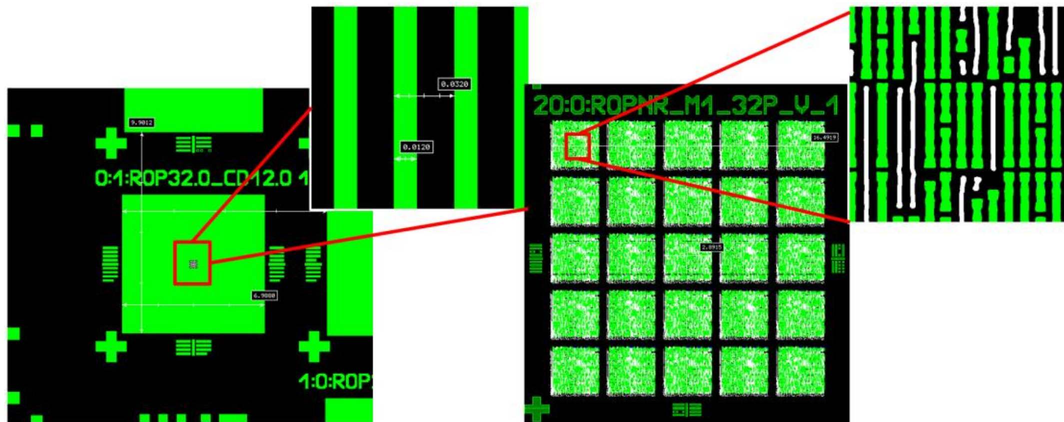


Figure 11. OSCAR2 wafer sampling. The left-hand shows 1D design and right hand shows 2D Logic clips.

Figure 11 shows the 1D and 2D logic design on OSCAR2. For 1D array, it is a 7*7um^2 large pad for each design CD and pitch. We assigned 50 different designs of 1D array from dense to isolated pitch; +/-1nm mask bias is also applied when select 1D LS patterns; and 9 wafer shots were used for accumulating repetitive data for average contour creation. For 2D logic features, there are 25 repetitive unit cells inside a design pad for each pitch. We assigned 30 2D designs from pitch 32nm to 45nm for metrology; 10 different locations in the nominal shots were inspected for creating average contours as well.

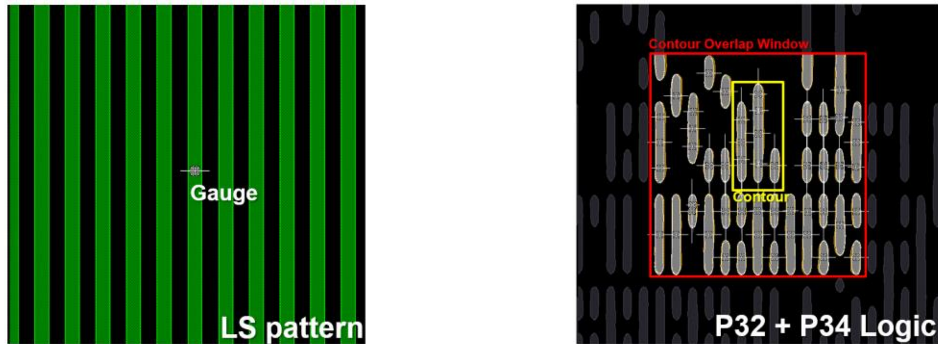


Figure12. L/S pattern gauges and P32+P34 contour overlap window.

Due to the nature of the design, a hybrid OPC modeling input plan was formed. To get better statistics results, the contours are extracted and averaged from metrology SEM images firstly. Then, we used an automatic CD extraction method from measurements contours by placing gauges in a 1nm step over the field of view (FoV). For 2D logic clips, we also applied hybrid mode by placing gauges across the center of design polygons, and then extracting CD for the averaged contours for each gauge, as shown in figure 12 left-hand plot. To improve the OPC model in 2D shape prediction, we also utilize Calibre ContourCal^{TM} from contour-based modeling. In figure 12 right-hand plot, the yellow frame of the FoV were brought into contour modeling for each clip.

Both measurement CD (1D+2D) and contour information were used for OPC modeling. A total of 700 gauges + 15 contours were used for the calibration phase and 1.4 thousand gauges + 42 contours for verification phase.

2.4. Metrology Balance Definition for OPC Modelling

High image quality and CD linearity are the main requirements for modeling. With low landing energy, advanced scan is mandatory for uniform signal collection.

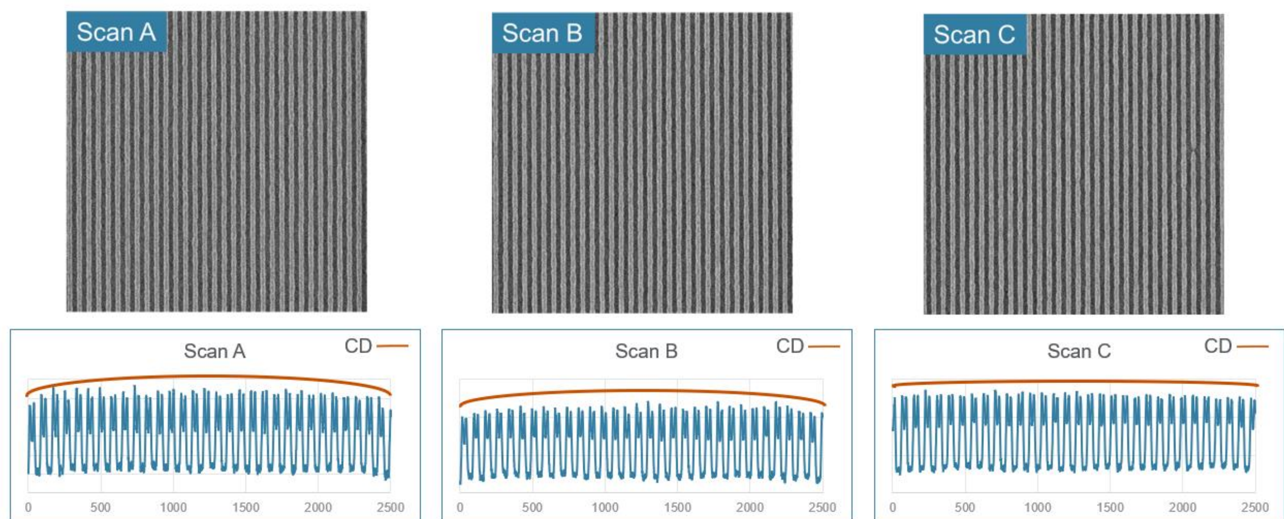


Figure 13. 1D Logic Pattern Scan Uniformity Optimization

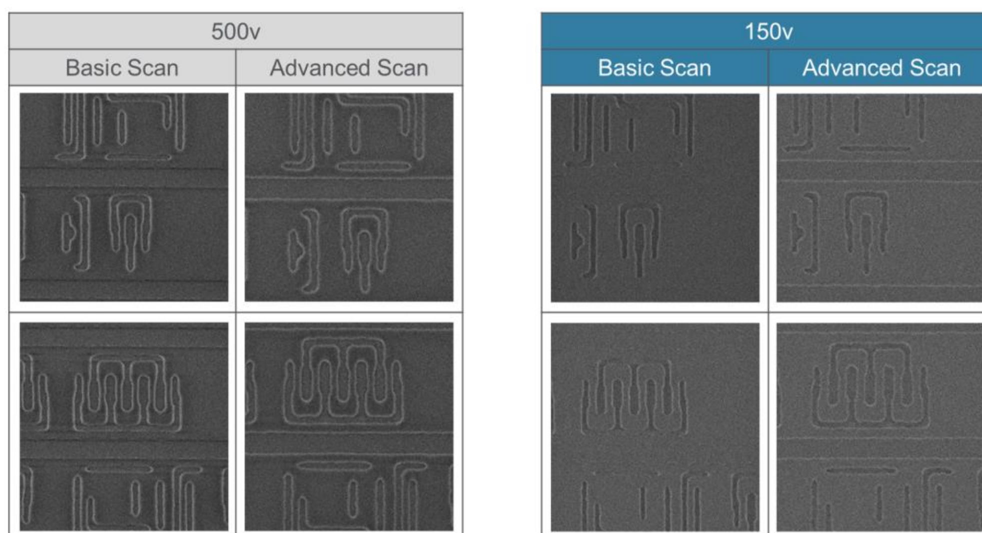


Figure 14. 2D Logic Pattern Imaging Optimization

3. RESULTS AND ANALYSIS

3.1. Etch Bias Analysis

After we overlap the measurement contours of 500V and 150V Litho and 800V Etch, there are two pairs of ADI-AEI bias generated. The firs pair is 500V Litho + 800V Etch measurement contours. The second pair is 150V Litho + 800V Etch measurement contours. Therefore, we have two different etch bias data set from two ADI metrology setups. To understand better the ADI metrology impacts between normal and low landing energy, it is good to have the information of Etch Bias per site (EBPS) in 2D clips.

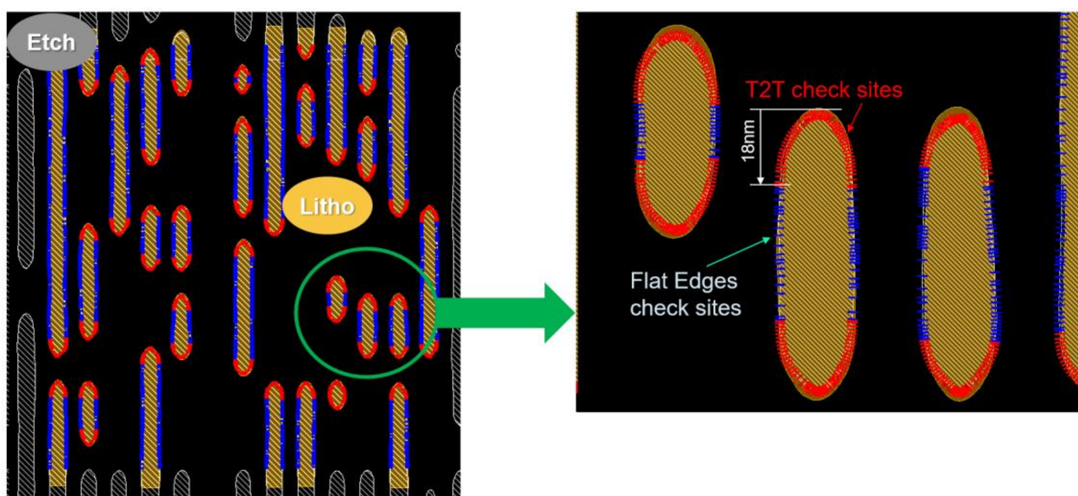


Figure 15. Example of “flat edges check sites” and “T2T check sites” in Etch Bias per site (EBPS).

EBPS analysis is carried out on two main regions of interest: flat edges and tip-to-tip (T2T) check regions. In Calibre OPCVerfy^{TM}, users are allowed to create customized markers and site placement for EpE probing. Figure 15 shows an

example that we defined T2T sites in red markers, which is pulled back 18nm from the horizontal design edges due to optical proximity effects. For the rest of the sites, they are defined as flare edge check sites.

For both 150V and 500V ADI-AEI contour pairs, the EpE from ADI to AEI contours can be measured along the detecting orientation of each check site. Those EpE values denote the etch bias for the entire geometry in general.

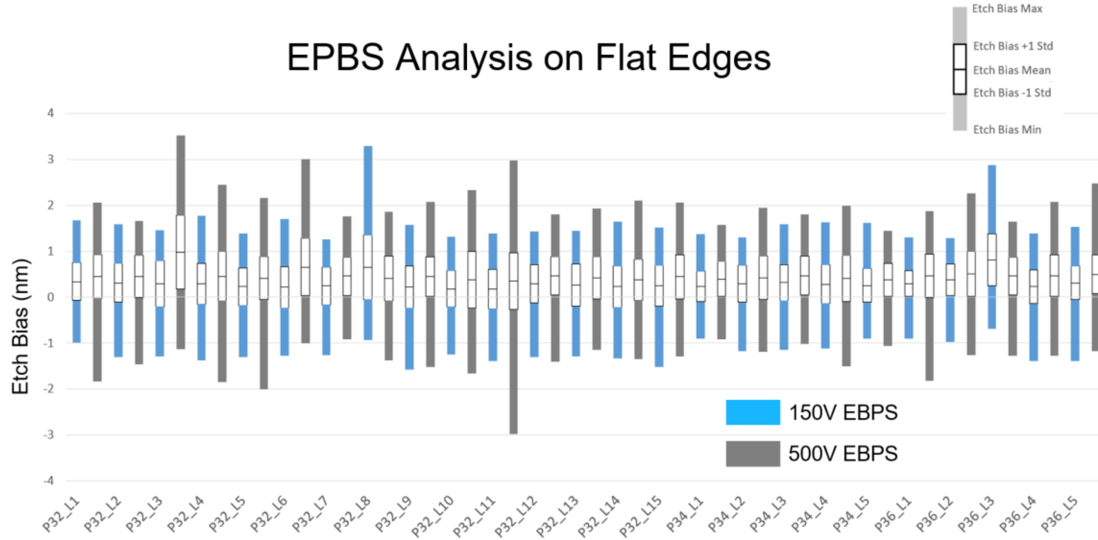


Figure 16. Chart of EBPS analysis on flat edges. Y-axis is the ADI to AEI etch bias in nm. For each logic clip, each box center is the mean value of etch bias and its 1 sigma standard deviation. The filled bars are the max. and min. values if the etch bias.

Figure 16 shows the EBPS chart from flat edges, defined in figure 5. The statistics box charts show the mean/ 1 sigma standard deviation/ min/ max of EBPS by EpE measurement of all sites in an individual logic clip. Mean EBPS is 0.29nm for 150V and 0.464nm for 500V. Averaged 1 standard deviation is 0.425nm for 150V and 0.484nm for 500V. It is shown the 150V metrology gives not only a lower overall etch bias but also a more uniform etch bias than that of 500V metrology.

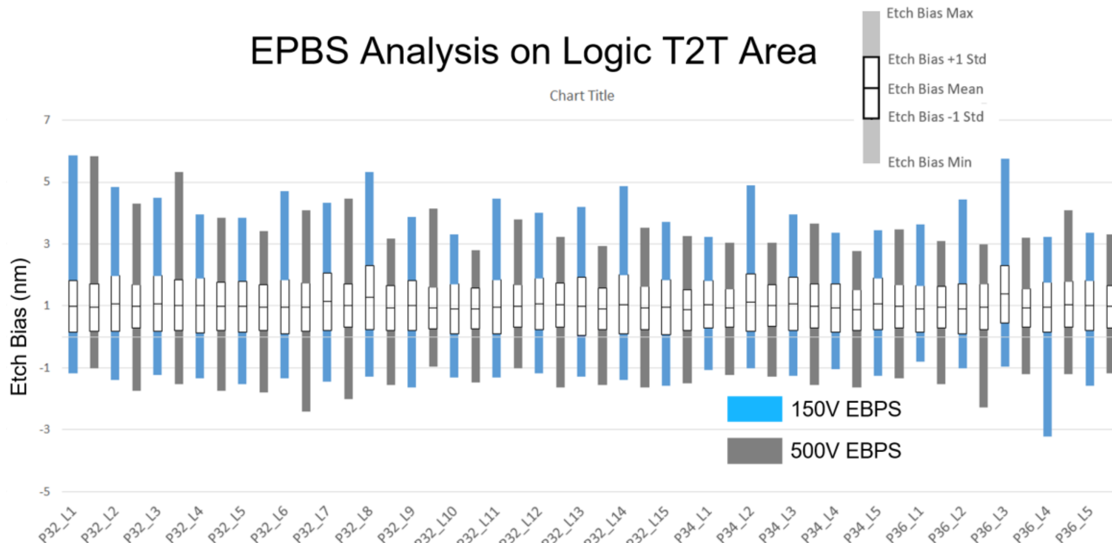


Figure 17. Chart of EBPS analysis on vertical edges. Y-axis is the ADI to AEI etch bias in nm. For each logic clip, each box center is the mean value of etch bias and its 1 sigma standard deviation. The filled bars are the max. and min. values if the etch bias.

Figure 17 shows the EBPS chart from T2T edges which are also defined in figure 5. Mean EBPS is 1.03nm for 150V and 0.96nm for 500V. Averaged 1 standard deviation is 0.86nm for 150V and 0.7nm for 500V. In the T2T region, it shows the

150V metrology gives comparable etch bias results with 500V metrology. It is probably contributed from the different E-beam scan orientations between 150V (diagonal) and 500V (orthogonal). In the future, we plan to match the metrology setup between low and normal landing energy metrologies.

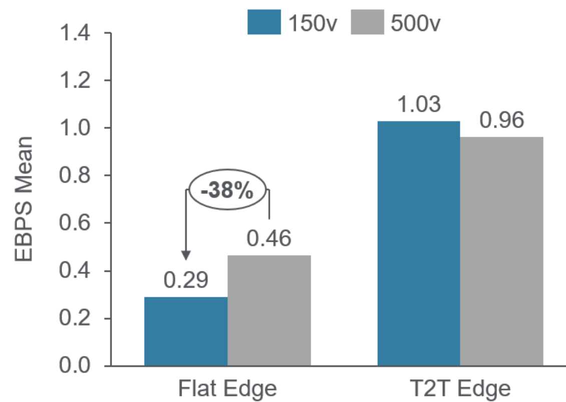


Figure18. EBPS Mean results comparing Flat Edge and T2T Edge between 150V and 500V metrology.

In the summary chart shown in figure 18, 150V metrology gives smaller mean EBPS than 500V metrology on flat edges. It is ~38% smaller etch bias in lower landing energy comparing to 500V metrology. On T2T area, there is comparable etch bias performance between the 2 different metrologies.

3.2. Variable Etch Bias Model Results (VEB)

Calibre^{TM} Variable Etch Bias (VEB) modeling was performed on the samples. In this study, a light compact model form of 2 Gaussian and 3 geometrical Visible kernels was used.

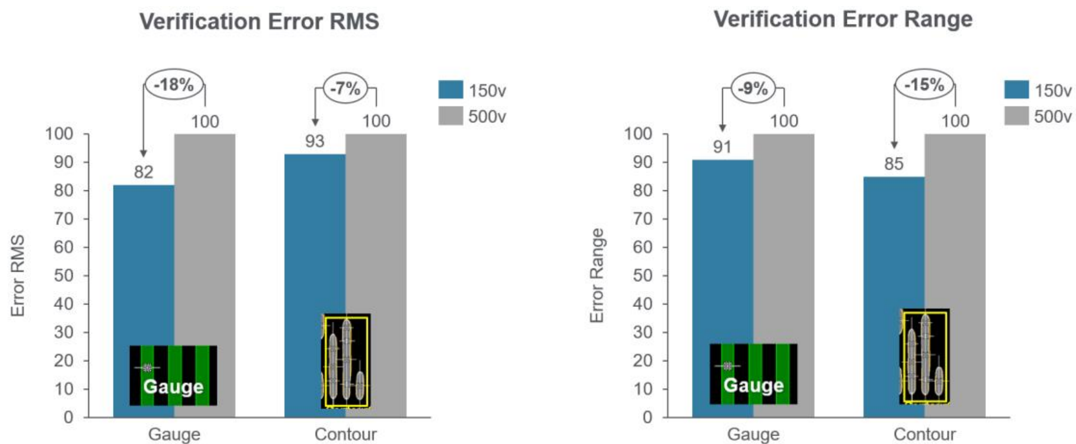


Figure19. Normalized Variable Etch Bias (VEB) Modeling Results.

Model calibration is based on the hybrid input of gauges and contour clips. 50% of the gauges and 35% of contours were used in model calibration. The calibration results show 150V metrology gives ~25% error RMS smaller. It is strongly correlated to the EBPS analysis in figure 18.

In model verifications with full data set, VEB with 150V metrology shows better error RMS and error range than that of 500V as shown in figure 19. The overall improvement from 500V to 150V is 7% and 18% for the gauges and the contours simulation error rms. For error range, the overall improvement is 9% in gauge and 15% in contour.

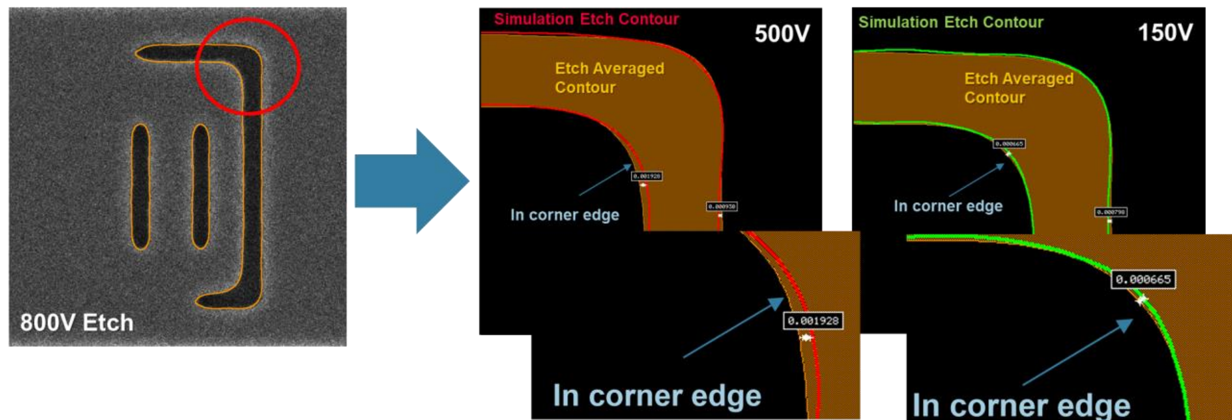


Figure 20. Litho/Etch Image Overlap Corner Edges - P45 L4 Logic Clip

Moreover, we overlapped the 150V and 500V ADI contours with the etch contours and SEM images in figure 120. The left-hand plot shows the overlap of AEI SEM image with its extracted measurement contours. The red circle highlights the 90-degree turning corner which is usually difficult to be predicted perfectly in this high curvature region. In the right-hand figures shows the overlapped images of simulations of 150V and 500V ADI to the AEI measurement contours. It demonstrates that the simulation results from 150V OPC etch model can generate better prediction on the in-corner region of that 2D area than that of 500V OPC etch model.

The results show low landing energy reducing metrology artifacts when compared to the higher landing energy. Such results help the modeling phase to optimize ADI and AEI contours prior to OPC generation. This concept still needs a comprehensive wafer data to prove reliable for OPC etch model.

4. CONCLUSION & NEXT STEPS

IMEC iN3 BEOL lithography process with EUV CAR PTD is applied. Calibre RET Selection™ freeform source is optimized with anchor P32 + metal routing design. Utilizing next generation CD SEM VeritySEM10 applying low landing energy at high resolution. Contour technology allows better prediction on 2D structures. Robust contour extraction is mandatory for EUV imaging (Low landing energy leads to low SNR images). VEB model with 150V metrology present improvement of 18% in error RMS comparing to 500V metrology. For contour based OPC modeling 150V metrology is better representative for compact etch model.

The current results show us a good confidence by using low landing energy metrology for etch bias inspection. In the future, a more comprehensive wafer sampling plan of both 0.33 and 0.55NA are needed to prove the full strength of low landing energy metrology in applications of OPC modeling.

REFERENCES

[1] Ran Alkoken, Sandip Halder, Hyo Seon Suh, Mor Baram, Gadi Oron, Kasturi Saha, Kevin Houchens, Yarden Melamed, "Effects of 0.55NA EUV material stack on eBeam metrology performance," Proc. SPIE 12496, Metrology, Inspection, and Process Control XXXVII, 1249616 (30 April 2023);
[2] Mary A. Breton, Karen Petrillo, Jennifer Church, Luciana Meli, Jennifer Fullam, Stuart Sieg, Romain Lallement, Nelson Felix, Shimon Levi, Susan Zollinger, Felix Levitov, Sean Hand, Jason Osborne, and Weijie Wang "Resist shrink characterization methodology for more accurate CD metrology", Proc. SPIE PC12053, Metrology, Inspection, and Process Control XXXVI, PC120530C (13 June 2022);
[3] Yuri Granik "Calibration of compact OPC models using SEM contours", Proc. SPIE 5992, 2005;

[4] George E. Bailey, Thuy Do, Yuri Granik, Ir Kusnadi, and Andrew Estroff "Intensive 2D SEM model calibration for 45nm and beyond", Proc. SPIE 6154, Optical Microlithography XIX, 61542W (20 March 2006);

[5] Kunal N. Taravade, Ebo H. Croffie, and Andrew Jost "Two-dimensional image-based model calibration for OPC applications", Proc. SPIE 5377, Optical Microlithography XVII, (28 May 2004);

[6] Nivea Schuch, Frederic Robert, and Thiago Figueiro "The rise of contour metrology from niche solution to versatile enabler", Proc. SPIE 12496, Metrology, Inspection, and Process Control XXXVII, (27 April 2023);

[7] Alexandre Moly, Nivea Schuch, Frederic Robert, Thiago Figueiro, Jessy Bustos, Loïc Perraud, Jonathan Pradelles, and Elie Sezestre "Self-supervised deep learning neural network for CD-SEM image denoising using reduced dataset", Proc. SPIE 12496, Metrology, Inspection, and Process Control XXXVII, 124961D (27 April 2023);