Overlay Metrology Performance of Dry Photoresist Towards High NA EUV Lithography

Eren Canga[a], Victor Blanco[a], Anne-Laure Charley[a], Cyrus Tabery[b], Gabriel Zacca[c], Nader Shamma[d], Benjamin Kam[e], Mohand Brouri[e]

[a]IMEC, Kapeldreef 75, Leuven 3001, Belgium
[b]ASML, 399 W. Trimble Road, San Jose, CA 95131, USA
[c]ASML Veldhoven, De Run 6501 5504 DR, Netherlands
[d]Lam Research Corp., 4650 Cushing Parkway. Fremont, CA 94538
[e]Lam Research Corp. Belgium, Kapeldreef 75, Leuven 3001, Belgium

ABSTRACT

In this work, we study the optical overlay metrology performance and impact of an integrated hard mask etch step using the dry resist process with High Numerical Aperture Extreme Ultraviolet Lithography (High NA EUVL)-related thicknesses. Diffraction-based overlay measurements were performed after dry development and integrated hard mask etching for different overlay target designs. The measurement precision for the after-dry development measurement is shown, and the benefits of using integrated hard mask etch overlay metrology with respect to after-dry development are discussed.
Keywords: μDBO, cDBO, ADI Overlay, Precision, Dry Photoresist, High NA

1. INTRODUCTION

As the semiconductor industry keeps advancing towards smaller feature sizes, the EUV patterning requirements for improved resolution, defectivity, and overlay are becoming more critical. At the same time, improved metrology precision and reproducibility would be required for high-volume manufacturing of the scaled devices. Dry photoresist (PR) has been demonstrated to meet these requirements in terms of defectivity and process window improvement [1]. Recently, dry resist has been studied to investigate its readiness for High Numerical Aperture (HNA) EUV lithography using various e-beam and optical methods [2]. However, overlay metrology performance with dry photoresist in the context of high NA EUV has not been explored yet.

One of the key requirements of high-NA EUV lithography is the photoresist thickness. Due to the reduced depth of focus (DOF) of the High HNA EUVL system, the photoresist thickness that is used is expected to be 20nm or less. This requirement will also have an impact on the optical overlay metrology after the photoresist development step since it is sensitive to the material properties and thicknesses. As the dry photoresist is also a critical candidate for high NA EUV lithography, the overlay metrology performance should be investigated.

In this study, we evaluated the optical overlay metrology performance of dry resist after the development step and investigated the impact of a subsequent hard mask (HM) etch process that can be run in an integrated flow. A dual-layer short loop stack was used in this study with two different dry photoresist and HM thicknesses, which is also compatible with high NA EUV patterning requirements. Diffraction-based overlay metrology (DBO) was performed after dry development (ADI) and after HM etch (AEI).

The ADI overlay results indicate that patterning with dry photoresist provides enough optical contrast for high quality overlay measurements with less than 0.2nm dynamic reproducibility on certain target designs. Furthermore, overlay metrology after integrated HM etch improves the dynamic reproducibility up to three times for the underperforming targets with respect to ADI metrology, especially for the thinnest dry photoresist. This enhancement could provide more flexibility for the overlay target design and measurement profile selection. Thanks to improved contrast, performing overlay metrology at the HM AEI step also lowers the overlay measurement and recipe setup time. Combining the reworkable characteristics

Metrology, Inspection, and Process Control XXXVIII, edited by Matthew J. Sendelbach, Nivea G. Schuch, Proc. of SPIE Vol. 12955, 129551R · © 2024 SPIE
0277-786X · doi: 10.1117/12.3010115

and inherent cost-saving advantages of dry resist, integrated HM etch overlay metrology would be the preferred method instead of ADI metrology.

2. EXPERIMENTAL

2.1. Process Flow

A dual-layer short-loop process flow is used to form the overlay gratings as shown in Fig 1. 30nm SiN and 10nm SiO2 are deposited on the Si 300mm substrates. The three-layer EUV lithography stack consists of a dry-deposited ashable hard mask (AHM), an underlayer, and dry photoresist. The dry photoresist is imaged by using NXE:3400B to form minimum 36nm pitch pillars. The dry-developed resist patterns are transferred into the Si using RIE. A thick oxide layer is deposited onto the Si pillars to mimic a front-end-of-line (FEOL) flow. The oxide layer is planarized by using the chemical mechanical polishing (CMP) method. To achieve an ultra-flat surface and avoid overlay metrology based on the topography, a second set of oxide deposition and CMP steps is performed, which was used at Imec in previous studies [3]. For the second layer, 15nm TiN and 5nm SiO2 are deposited on top of the planarized SiO2. Two sets of wafers are used for the three-layer lithography stack with different thicknesses. Table 1 summarizes the thickness splits (relatively) in the lithography stack for the 2nd layer. As in the first layer, the second layer EUV exposures are performed using the NXE 3400B scanner. Overlay metrology is performed after the dry development step and after transferring the resist patterns into the AHM by using the Yieldstar-375 diffraction-based overlay (DBO) system. The transmission electron microscopy (TEM) cross section of an overlay target that indicates the flatness of the intermediate SiO2 layer is shown in Fig 2.

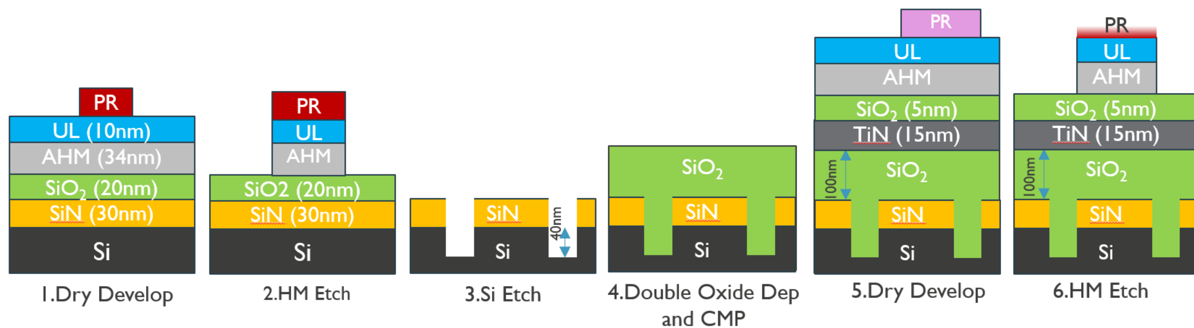


Figure. 1 Process flow to form overlay targets used in this study

Table 1. Two thickness splits of the materials used in the litho stack

	1st set	2nd Set
Resist	POR	0.6xPOR
Hard Mask	POR	0.6xPOR

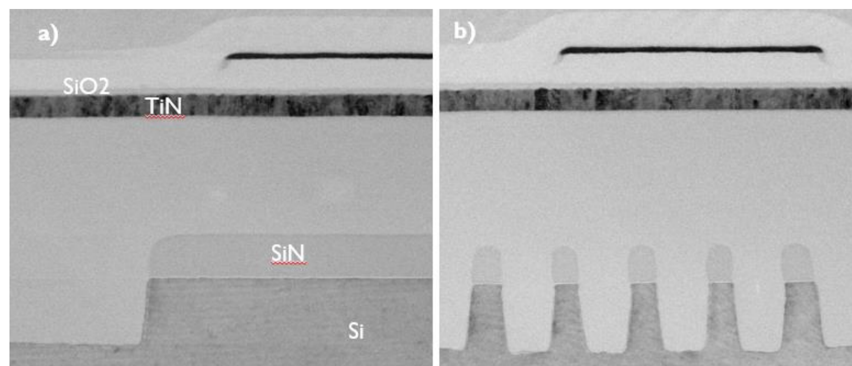


Figure 2. Cross section TEM images after HM patterning process. From left to right: a) non-segmented overlay target grating pair, b) pair of segmented bottom grating with non-segmented top grating

2.2. Diffraction Based Overlay Metrology

The overlay measurements performed in this study are diffraction-based, using the ASML Yieldstar 375 system. The overlay is measured by utilizing the diffraction of the incident light from an overlay target. The overlay target consists of two sets of grating that are patterned in two different layers of a fabrication process with an intentional bias. When the target is illuminated by the light source, the gratings form a diffraction pattern, which is captured by the measurement sensor. The zero-order intensity of this diffraction pattern is independent of the overlay between the gratings, whereas the +1 and -1 order intensities change asymmetrically depending on the overlay, as shown in Fig 3. An overlay consists of combinations of four gratings: two for the x direction and two for the y direction, as shown in Fig 4. In each grating pad, there is a known offset between top and bottom gratings, d, called bias.

The intensity difference between the +1 and -1 orders of the diffracted light can be defined as asymmetry and represented as $A = I_{+1} - I_{-1}$. The asymmetry, A, is a function of overlay and is linear if the overlay errors are relatively smaller than the pitch of the target gratings. From the two measurements (+d and -d grating pairs), the overlay can be approximated as below:

$$\sim Overlay \sim d\,\frac{A^{+}+A^{-}}{A^{+}-A^{-}} \quad \text{where } A^{+}, A^{-} \textit{ is the} \text{ asymmetries for +d and -d pads}$$

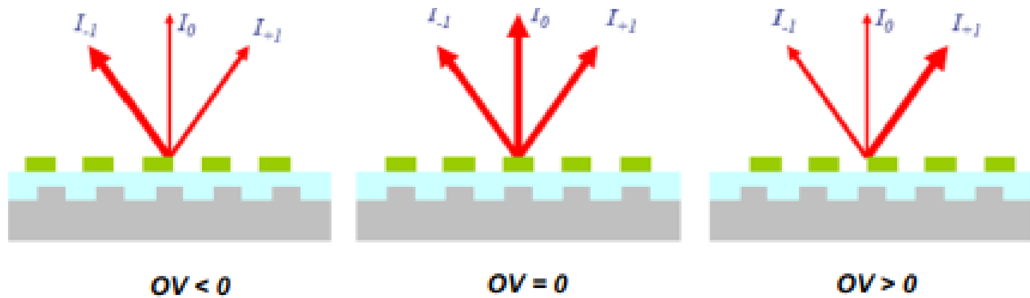


Figure 3. The schecmatic of diffraction based overlay principle. First order asymmetries varies as a function of overlay.

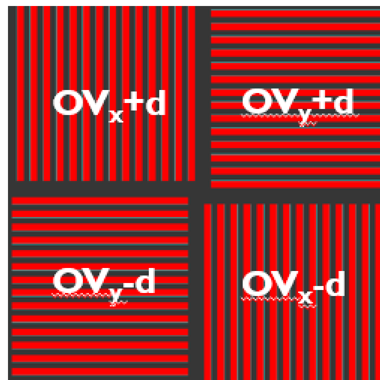


Figure.4 Top view of and µDBO target, indicating the x,y directions and bias.

A good signal contrast between the diffraction orders from the top and bottom gratings is desired for a healthy DBO measurement [4]. This signal contrast is defined by a parameter called stack sensitivity (SS), which can be formulated as below: It is an important parameter for the overlay measurement and depends on the layer thicknesses, optical constants, target pitch, and wavelength. The typical required SS for a healthy measurement should be greater than 0.1.

$$SS = \frac{A^{+} - A^{-}}{A^{+} + A^{+}}$$

ASML introduced continuous bias diffraction-based overlay (cDBO) targets [5]. Unlike the µDBO targets, the bottom and grating of the cDBO targets have an un-equal pitch to form Moiré fringes, which also includes phase information since the diffraction directions are not equal (compared to µDBO). As a result, the usable wavelength range is improved, along with the robustness to the process variations.

2.3. Metrology Setup

The primary performance metric that is considered is the dynamic reproducibility of the overlay measurements. A wide range of µDBO and cDBO target designs are evaluated since target design has a severe impact on metrology performance. Overlay target designs are selected to cover different application cases. For example, we are using unsegmented targets for applications where design rules are relaxed, such as the upper back end of line layers. Apart from that, a target type in which the top grating CD is half of the bottom grating is included. This type can be useful for cut processes (such as gatecut on top of gate). Since the top grating is etched into the same material as the bottom grating, the width of the final grating pattern would be sufficient to not peel from the surface. Another type that is used is segmented bottom grating, which is commonly used to increase compatibility with CMP (chemical mechanical polishing) processing. Also, targets with both top and bottom grating segmentation versions are added to the evaluation for cases where strict density design rules are needed. Another aspect of evaluating different target designs is stack sensitivity. The stack sensitivity depends on the balance between the diffraction efficiencies (DE) of the top and bottom gratings [6]. The selected designs have a variety of top/bottom grating CD combinations, which results in different signal contrast for us to evaluate different cases. The measurement profiles (wavelength, dose, and polarization) are optimized by using ASML's holistic metrology qualification (HMQ) method [4]. The dynamic reproducibility measurements were performed on 26 points in the field using 10 fields. The wafers underwent a 10-load/unload cycle.

Table 2. Summary of the variations of the overlay targets

Type	Size (um)	Bottom CD/Pitch (nm)	Top CD/Pitch (nm)	Segmentation
DBO	10	250/500	250/500	No
DBO	16	275/550	275/550	No
DBO	16	300/600	150/600	No
DBO	16	250/500	250/500	yes
DBO	16	250/500	250/500	yes/Both
cDBO	16	250/500	250/500	no
		275/550	275/550	
cDBO	16	250/500	250/500	no
		300/600	300/600	

3. RESULTS AND DISCUSSION

First, we measured the stack sensitivity variation through the wavelengths, or so-called swing curves. These curves are helpful to access the robust regions of wavelengths for a given stack, which gives valuable information for recipe selection. The swing curves for each µDBO and cDBO target design for different lithography stack thicknesses (dry resist and hard masks) are shown in Fig 5 and Fig 6. The blue curves represent the swing curves after the dry photoresist development (ADI), whereas the red ones represent the measurements after the hard mask etch (AEI) step. The orange band (where stack sensitivity goes below 0.1) is the region where the overlay sensitivity is too low to be used for recipe selection.

As can be seen, the thick lithography stack (POR thickness) provides a good enough stack sensitivity (SS) to determine a robust wavelength region for recipe optimization for all target types. The thin lithography stack (0.6 of the POR thickness) however, fails to provide a robust wavelength region for the low contrast targets at ADI. The two µDBO targets, segmented gratings (both top and bottom at pitch 50 nm) and the 150nm top grating CD, show SS <0.1 throughout all wavelengths studied. After hard mask etching, the stack sensitivity through the wavelength improved drastically for all target designs,

providing more robust wavelength regions for profile selection. This is more critical for the low-contrast targets (top cd 150nm and both gratings segmented) since they provide a robust wavelength region after hard-mark etch measurements, which makes them measurable. cDBO targets also show a similar trend for SS improvement. One important remark is that they offer more wavelength than the µDBO for profile selection.

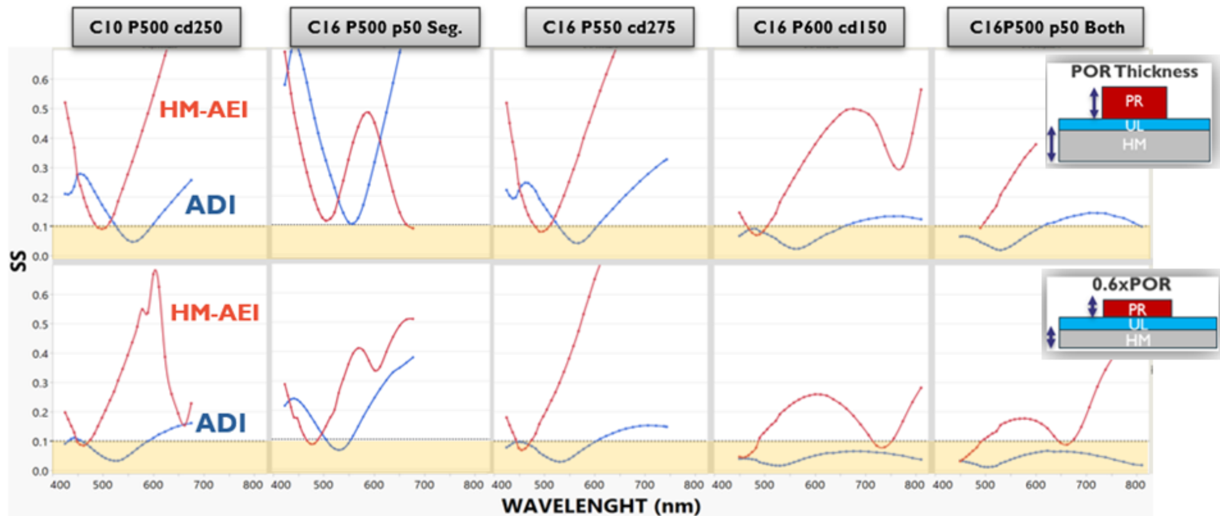


Figure 5. Swing curves for each µDBO target for thick (upper) and thin (lower) lithography stacks The red curves indicate the swing curves after the HM etch, and blue is for the ADI. Each curve pair (from left to right) represents a different target design, as indicated by the headers. The orange band represents the SS region that yields inadequate overlay sensitivities. The stack sensitivity is better after hard mask etch measurements, especially for thin lithography stacks.

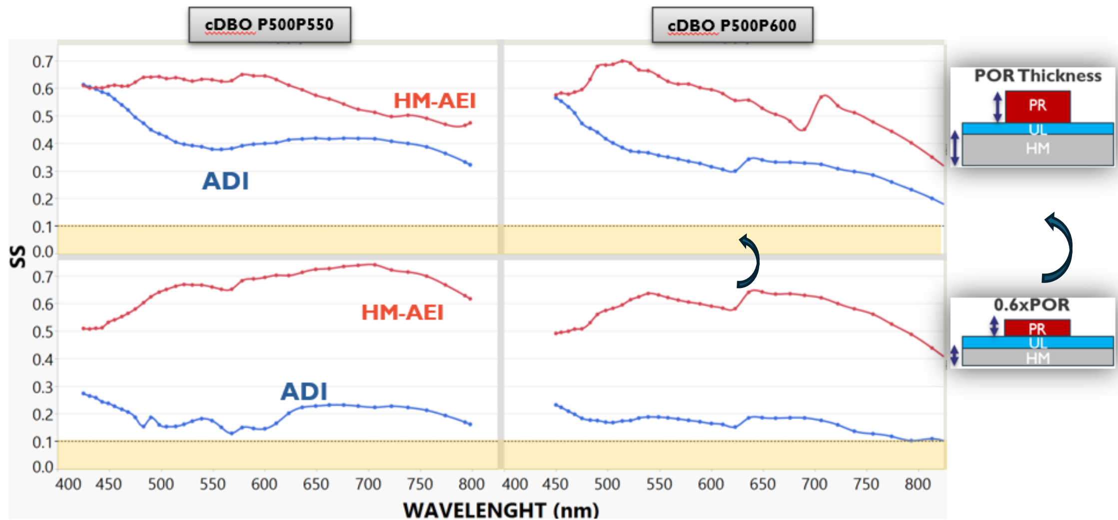


Figure 6. Swing curves for each cDBO target for thick (upper) and thin (lower) lithography stacks The red curves indicate the swing curves after the HM etch, and blue is for the ADI. Each curve pair (from left to right) represents a different target design, as indicated by the headers. The orange band represents the SS region that yields inadequate overlay sensitivities. The stack sensitivity is better for after-hard mask etch measurements and provides more single-wavelength options than µDBO.

Next, we evaluated the impact of the dry lithography stack thickness on the repeatability of the measurements both after dry development and hard mask etch steps for different targets. The repeatability of the diffraction-based measurements is inversely proportional to the stack sensitivity (higher SS means improved repeatability). The repeatability dependence on the SS is shown in Fig 7 for two target types. The repeatability reported in this figure is the point-to-point 3s variation over 10 repeats across 260 points across the wafer. For the thick lithography stack, the cDBO target yields good and uniform

repeatability across the wafer thanks to having higher stack sensitivity for both ADI and AEI cases. For the thin lithography however, the uniformity of the repeatability of the measurements is low at the ADI step as the stack sensitivity is lower. For the low contrast target, both top and bottom gratings are segmented, this trend is observed for both thicknesses. At the HM AEI step we observe more precise and more uniform repeatability measurements for both target types as the SS is improved compared to ADI. We believe that the improvement in SS is related to the increase in the volume of the top gratings.

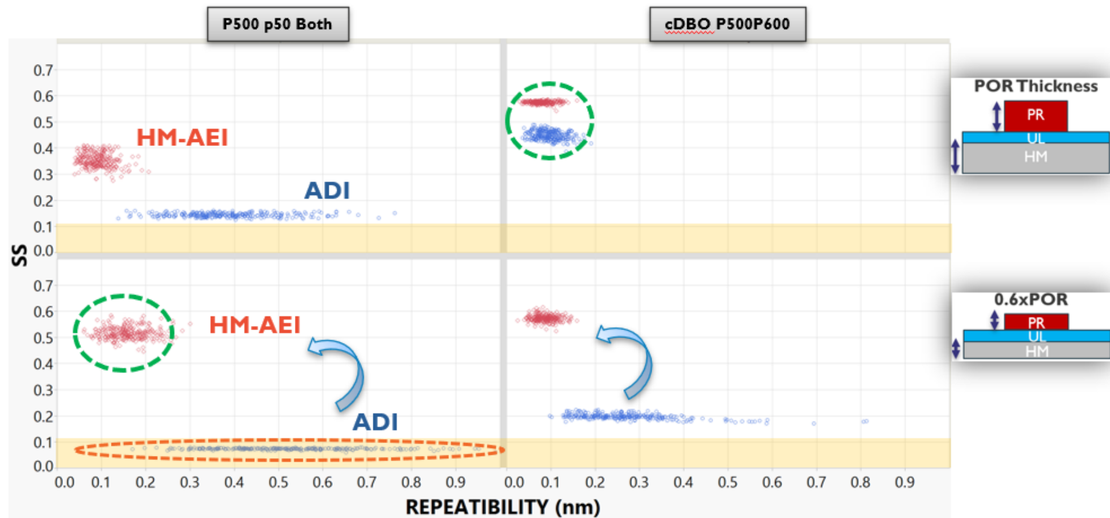
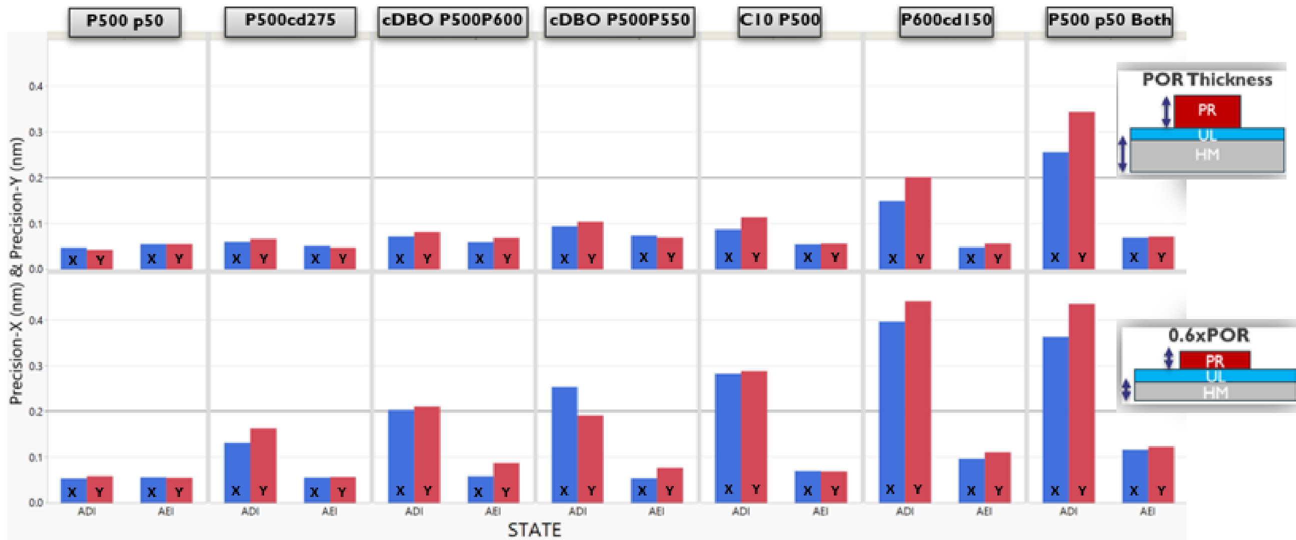


Figure 7. Repeatability depends on the stack sensitivity. Higher stack sensitivity reduces the metrology noise and provides more precise measurements. The precision of the measurements improved at the hard mask etch step with respect to the after-development measurements.

The dynamic reproducibility of the measurements is summarized in Fig 8. It is calculated as 3xRMS over 10 load/unload cycles. The bottom segmented µDBO target (p500 p50) demonstrated exceptional dynamic repeatability across all scenarios. This target has a good balance between the top and grating diffraction efficiency for the given stack, which results in good stack sensitivity. For the POR thickness, most targets have less than 0.2nm dynamic precision, which meets the precision requirements for high-end manufacturing. Only one target is above 0.2 0.2nm precision and improves after the HM etch step [7]. For the thin lithography stack, the dynamic precision improvement after the hard mask etch is more pronounced. We have four targets with dynamic precision above 0.2 nm, and they get below 0.1nm after the HM etch step. Up to 3 times improvement in precision can be observed on the two low-contrast targets.

These results indicate that overlay metrology at the hard mask etch step has clear advantages over overlay metrology after the development step. It is important to remember that Lam dry development and hard mask etch can be integrated into the same platform, speeding up the processing. Significant enhancements are mostly seen in the thin lithography stack, crucial for HNA EUV lithography. It eases the recipe optimization since it provides more robust wavelength regions and makes the low-contrast targets measurable. Also, the measurements become more stable over the wafer, which has low variation in the precision of the measurements at the HM etch step. Overall, dynamic precision improves. This enhancement is crucial as it enables us to utilize a greater number of targets and expands the range of target design possibilities. Also, since the HM AEI measurements require less illumination dose than the ADI measurements, it helps to reduce the measurement time.



Figfure 8. Summary of the dynamic reproducibility of the overlay measurements for both the ADI and AEI steps. One design that performs very well at both steps and overall improvement is observed at the AEI step for the rest of the designs, especially for the thin lithography stack.

4. CONCLUSION

In this study, we have shown that Lam dry resist could provide precise overlay measurements towards high NA EUV lithography with less than 0.2nm precision over a range of overlay target designs. Furthermore, the precision of the overlay measurements is improved at the hard mask etch overlay metrology step due to the increase in stack sensitivity. It also allows for more precise overlay measurements and flexibility in the target design. When we also consider its reworkable characteristics and inherent cost-saving advantages, integrated hard mask etch overlay metrology could be the preferred method over the after-development overlay metrology step.

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