Hotspot discovery and variability analysis for advanced EUV processes

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I. ABSTRACT

To maintain lithographic pitch scaling, extreme ultraviolet (EUV) processes have been adopted in high-volume manufacturing (HVM) for today's advanced logic and memory devices. Among various defect sources, stochastic patterning defects [1] are one of the most important yield detractors for EUV processes. In this work, we will limit our scope to patterning defects arising out of lithography. In the past, it has been shown that the patterning defect process window is often limited by stochastic hotspots [2]. These hotspots have very low failure probabilities in a well-optimized process, and hence their detection necessitates large area sensitive defect inspection, such as with a broadband plasma (BBP) optical defect inspection system. It has also been shown [2] that systematic issues in design can be exacerbated by stochastic variations. Hence, it is critical to discover these hotspots and study their variability with massive SEM metrology. Such analyses can uncover systematic trends, which can then be corrected and monitored. In this work, we discover hotspots using broadband plasma (BBP) optical inspection and study their variability using KLA's aiSIGHT™ pattern-centric defect and metrology software solution for automatic defect classification and SEM metrology measurements. We also demonstrate the need for fast and rigorous 3D probabilistic stochastic defect detection on design as a continuation of this work.

Keywords: *stochastic hotspots, broadband plasma, automatic defect classification, SEM metrology, hotspot prediction*

II. INTRODUCTION

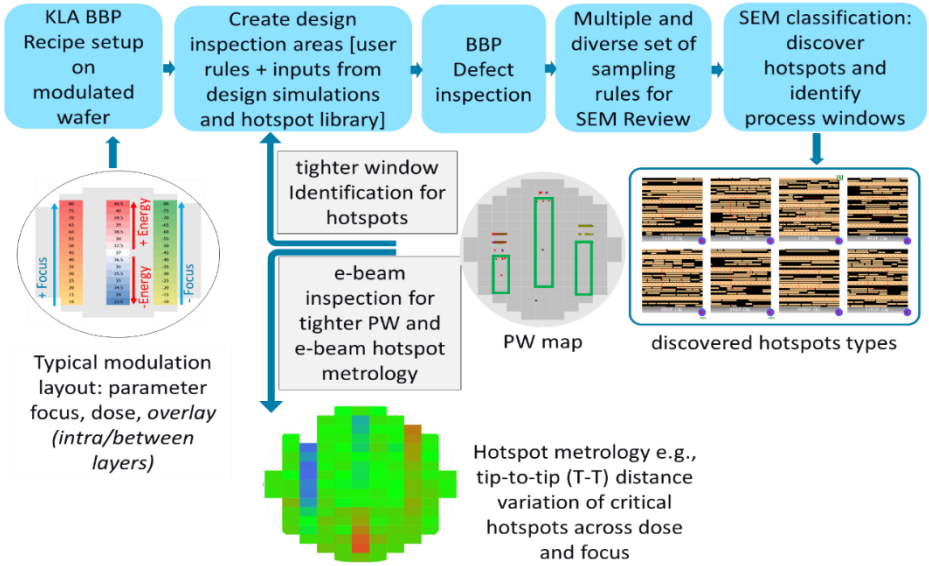

Figure 1: Process Window Discovery (PWD) and hotspot identification flow

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To discover weak patterns (also known as hotspots) and their process windows (PW) we use a large area, high sensitivity, optical defect inspection methodology developed using a broadband plasma defect inspection system. Such an inspection flow is shown in Figure 1 in its simplified form. We use a modulated wafer, typically with dose and focus modulations to set up the inspection. At this point, design inspection areas (also known as care areas) are incorporated from a general rule-based search on intent design and those from weak pattern models, design simulations or optical proximity corrections (OPC), if available. After a sensitive defect inspection on the modulated wafer, defects are sampled for SEM review using multiple sets of rules. SEM images are then classified and hotspots are identified along with their process window. A second-pass optical or e-beam inspection is often done for tighter identification of the process window upon refinement of care areas. Hotspot metrology for center-critical hotpots may also be done. One of the critical steps for faster time to results is automatic defect classification. In this paper, we have used the aiSIGHT pattern-centric defect and metrology software to accomplish this. The aiSIGHT (Anchor Integrated SEM Image Guided Hotspot Toolkit) software is tool agnostic – using SEM images from all manufacturers' e-beam inspection, review and metrology systems. Analysis can be done either with design (die-to-database – D2DB – solution for logic and logic-like layouts) or without design (as in the case of regular arrays). Figure 2 shows an example of using D2DB defect detection and classification. aiSIGHT can be integrated with Klarity® Defect for seamless defect analysis.

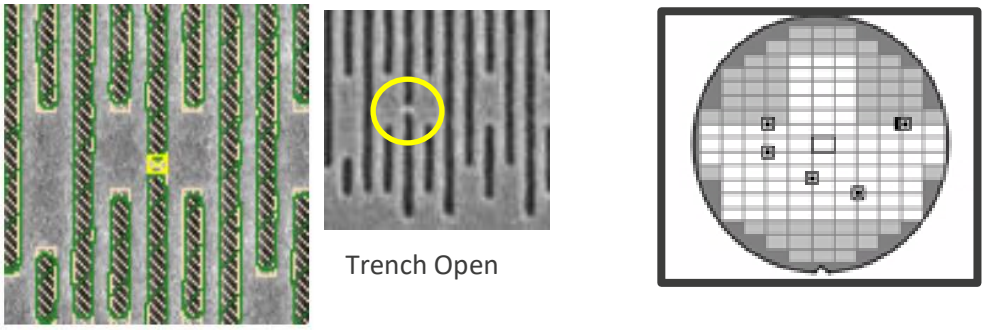

Figure 2: Example of die-to-database defect detection and classification on EUV Pitch 36nm logic-type layer

III. EXPERIMENT

In this paper, a pitch 28nm (P28) PNR (place and route) metal interconnect design on a BF (brightfield) low-n mask is exposed with single EUV exposure using spin-on MOR (metal oxide resist). We use a short loop stack and inspect with a 2935 broadband plasma (BBP) defect inspection system post etch to discover hotspots and PW on a FEM (focus exposure matrix) wafer, although it is preferred to have a PWD layout for better detection efficiency. There are different tip-to-tip (T-T) distances and biases designed for comparison purposes but in this work, we will only report results from P28 half-pitch bias and T-T design 20nm and 22nm. We also validate the process window with inspections on a CDU wafer. An example PNR design intent clip, the wafer stack and the FEM layout are shown in Figure 3 from left to right respectively.

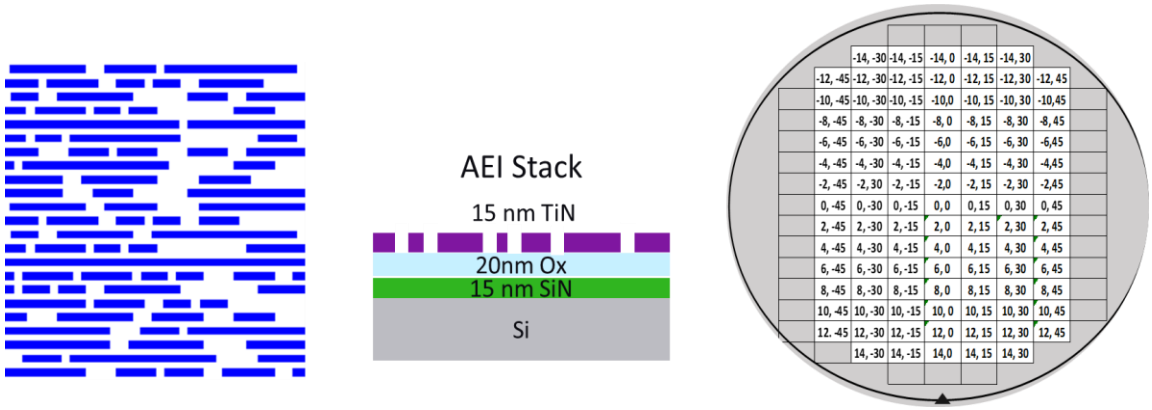

Figure 3: PNR design clip, short loop AEI stack and FEM exposure layout (offsets from nominal dose and focus are shown in mJ/cm^2 and nm respectively)

IV. RESULTS

Once the PWD methodology flow is executed, the defect process window can be obtained as a wafer map showing the existence and location of SEM verified hotspots. The wafer maps for each class of hotspots such as trench opens, tip-to-tip bridges, line end pullbacks, etc., can also be obtained. We can then identify overlapping defect-free process conditions across different classes. Figures 4a and 4b show a summary of these process windows for our experiment. We compare here PWs across three hotspot classes (namely trench opens, tip-to-tip horizontal bridging and hard-line end pullback) and across two tip-to-tip design rules (namely 20 and 22nm).

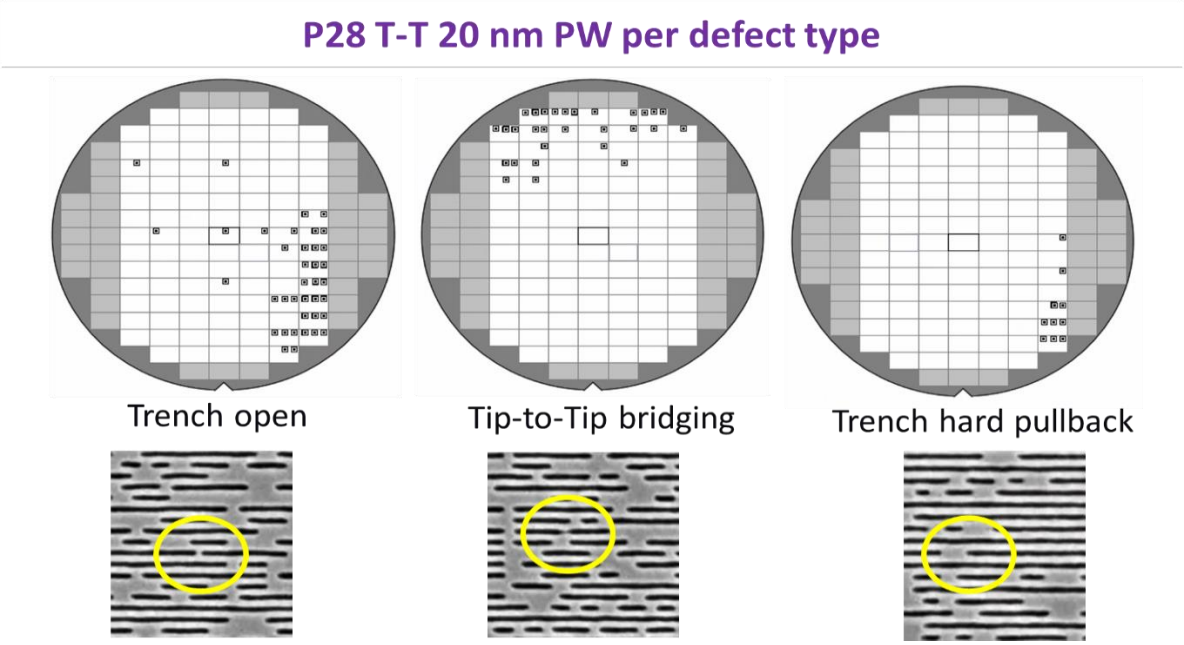

Figure 4a: PWD summary for the tip-to-tip 20nm design rule case: Defect PW map after SEM classification for three hotspot classes and an example SEM image for each

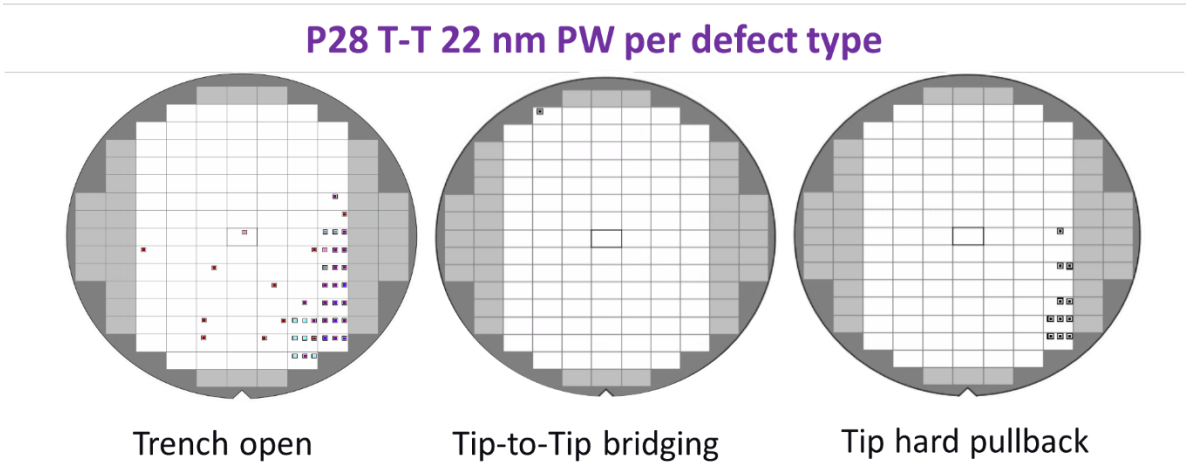

Figure 4b: PWD summary for the tip-to-tip 22nm design rule case: Defect PW map after SEM classification for three hotspot classes

From Figure 4 it can be seen that more aggressive tip-to-tip design rule leads to smaller windows (more failures at lower dose dies) for the tip-to-tip horizontal bridge class of hotspots. Trench open hotspots do not seem to have been impacted by the tip-to-tip design rule and are limiting the process window in a stochastic manner with more failure tendencies at higher dose and focus dies. Pullbacks, beyond LCDU (local CD uniformity), are mainly tiggered in high dose, high focus modulations. New center litho conditions (δdose= -2, δfocus = 0) could be used to have the least defectivity on both trench opens and tip-to-tip bridges. This is verified with BBP inspection of the 20nm tip-to-tip design rule on a CDU wafer exposed with these litho conditions. The defect map is shown in Figure 5.

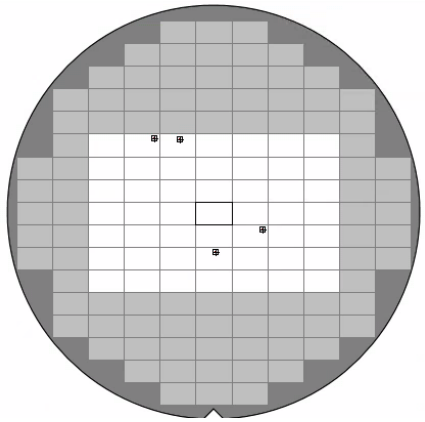

Figure 5: The CDU wafer exposed with dose and focus conditions obtained from FEM showed very few trench opens and no T-T bridges

Variations in trench CD with its LCDU and tip-to-tip CD with its LCDU through dose offsets from nominal are shown in Figure 6. With the current process, the T-T post etch CD is much larger than intended. Process and OPC optimizations are ongoing to reduce T-T CD closer to intent without affecting trench CD, followed by PWD confirmation.

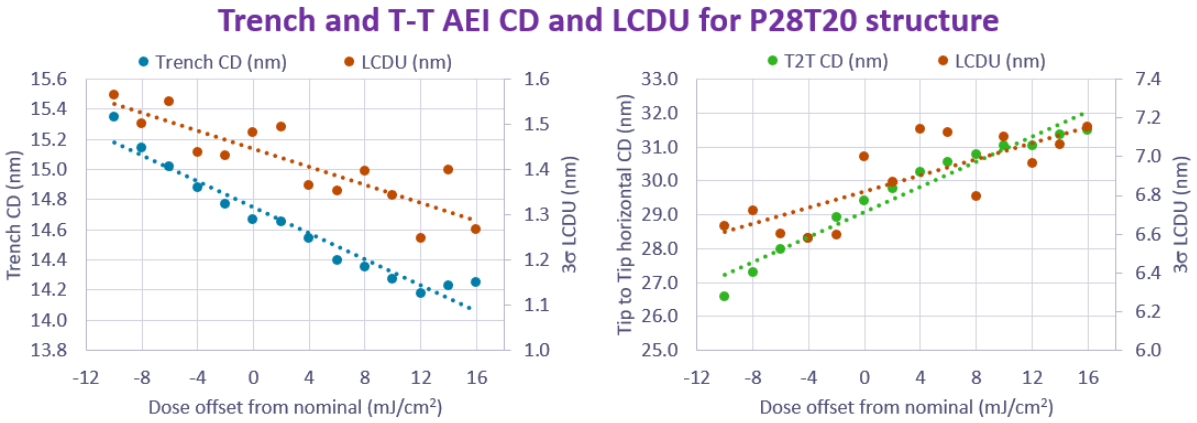

Figure 6: (Left) Trench CD and LCDU (3σ) with dose offsets from nominal; (Right) T-T CD and LCDU (3σ) with dose offsets from nominal

Next, we studied the process variation (PV) bands on a few PW-limiting hotspots from near nominal conditions. For this we collected SEM images on these hotspots on both modulated and CDU wafers, followed by contour extraction and stacking. The image collection and PV band measurement were done using KLA's e-beam metrology solution. The intent is to see the variation in PV bands at hotspot locations, and as such, determine if these variations are any indication of stochastic behaviour (e.g. hard fail). However, we found that at these levels of SEM sampling, we were not able to see any outlier behaviour. PV band widths also seemed unremarkable as compared to other features nearby in the FOV (field of view). Two examples are shown in Figure 7 for both modulated and CDU wafers. It would be fair to conclude that PV bands are not sufficient (at least with this level of SEM sampling) to show any obvious contour deviations from the target design, negating unique stochastic sensitivity.

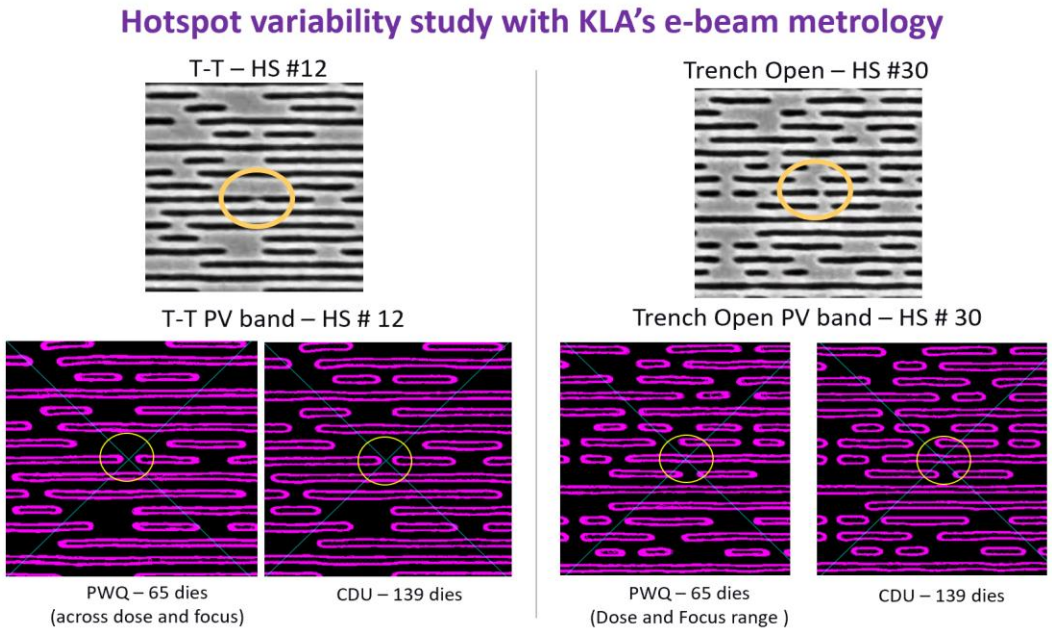

Figure 7: PV bands measured from KLA's e-beam metrology tool

Therefore, it becomes important to be able to predict these stochastic weak patterns from design simulations. These predictions serve as additional inputs to sensitive optical and e-beam inspections for hotspot discovery and monitoring applications. These predictions also help draw inferences about criticality (e.g. failure rate) of the hotspots empirically found by optical or e-beam inspections. To detect these stochastic hotspots from design simulations, a 2D model is not enough (such as those simulating ADI contours). A rigorous, physics-based, 3D resist model is required that takes stochastic variation of the resist profile into account. Also, the model should be highly accelerated to cover the full chip layout in a reasonable amount of time. For more details please refer to paper [3]. In our current study, the criticality of a limiting hotspot with defocus is shown in Figure 8. The model predictions on hotspot #30 as shown in Figure 7 (a semi-iso feature) are shown. The predictions are compared with a dense feature near the hotspot. From a computed LER (line edge roughness) point of view, both hotspot and dense features behave similarly with defocus. However, defect probability is very different with defocus, with the iso feature showing a higher probability of failing at slightly negative defocus.

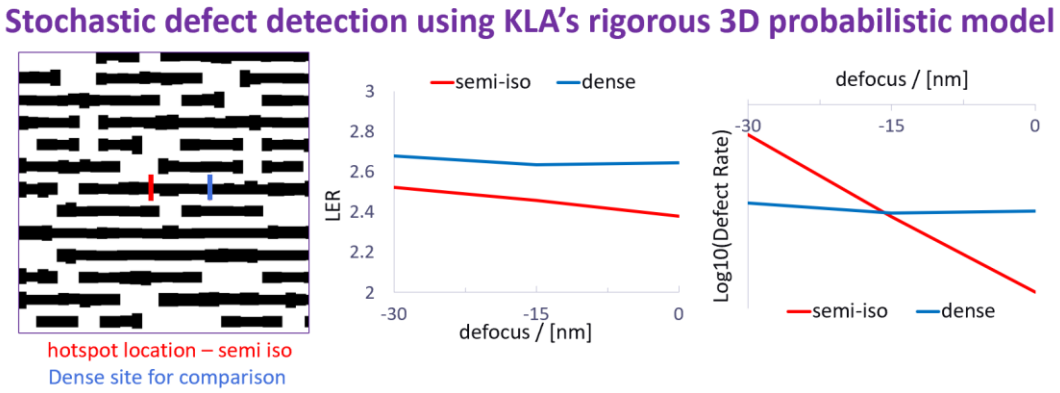

Figure 8: LER computed from 30k simulations does not show an obvious trend with defocus. However, the 3D model shows defect probability rapidly increases with increasing defocus on the semi-iso feature (flagged hotspot) showing higher sensitivity than the dense site.

V. SUMMARY

In this work, we use PWD flow to discover hotspots on a Pitch 28nm BF low-n PNR layer processed with single exposure EUV and spin on MOR. A tighter T-T design CD leads to a smaller T-T process window as expected. At near nominal conditions, PW is limited by stochastic hotspots. These hotspots do not easily show up in PV bands and may need very large SEM sampling to exhibit stochastic behaviour. Highly accelerated rigorous 3D probabilistic computational lithography can help verify these hotspots and predict their occurrence on full chip designs.

VI. REFERENCE

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