# Feature grouping to enable edge placement error-aware process control in multi-feature logic use case.

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### ABSTRACT

The grouping method assisted EPE-aware control method is being explored in a multi-feature dual layer Logic use case. EPE metric is estimated using angle resolved optical Scatterometry based overlay and electron beam-based metrology (large field of view SEM) for the reconstruction of edge-to-edge distance between the Metal and Via pattern. In the setup phase, EPE sensitivities to dose and focus have been derived using data from a FEM wafer. EPE-aware optimization, using scanner dose and overlay control sub-recipes, outperforms traditional optimization in simulations showing reduced EPE max per die. This improvement suggests a potential increase in device yield through the adoption of EPE-aware control strategies. To verify this performance improvement on wafers, an experiment is needed with minimal wafer to wafer and lot to lot variations which can be achieved by reducing time between lots and increasing the number of wafers measured.

Keywords: EPE, Grouping, Optimization, Overlay, Logic

## 1. INTRODUCTION

Over the latest technology nodes, traditional overlay (OVL) and critical dimension uniformity (CDU) metrics are used for monitoring and controlling the HVM on-product performance. Edge placement Error (EPE) is an additional KPI, which can potentially be used for budgeting, root causes analysis and yield improvement. EPE represents a distribution of the total error budget from different contributors (systematic, global, and local effects) [1]. It is well established that a substantial part of the EPE budget is attributed to the local variations and overlay contribution (Figure 1). Therefore, lithography solutions must effectively address these two critical aspects using optimization methods.

It has been shown that the EPE metric exhibits a stronger correlation with patterning defects compared to individual metrics [2]. Other research indicates that EPE has the potential to serve as an early predictor for yield [3]. Thus, EPE-aware process controller allows contributors from different layers to cross compensate to each other in spatial fingerprint, therefore, enabling the overall improvement of multilayer EPE [4,5].

Measuring EPE on a logic device is challenging due to the variety of features and large metrology load. There is a need to implement a categorization methodology such as grouping to classify features with similar EPE performance, based on their geometrical designs, optical behavior, and sensitivity to dose (and focus). With this method we can identify the most EPE critical features in a Logic design. This information is crucial to enable process controllers to be aware which fingerprints and specs are the most important in control and which fingerprints and specs are less important therefore allows trade-off.

In lithography processes, control loops are integral for enhancing (maximizing) product yield. Traditional optimization approaches address CD and overlay components independently whereas EPE-aware optimization considers all EPE components together. In this paper, we assess the performance of EPE-aware optimization in a cross-validation scenario and compare it to traditional optimization.

Optimization methods are introduced in Section 2. Wafer processing steps and metrology techniques are described in Section 3. In Section 4, the feature grouping method is investigated. Finally, the EPE setup and optimization results are discussed in Section 5.

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Figure 1 – EPE is composed by global and local errors.

## 2. OPTIMIZATION FLOW

In this paper, we aim to improve the product yield, as represented by EPE, through a multi-feature EPE-aware method that optimizes dose and overlay as illustrated in Figure 2.

Broadly speaking, as a first step, dose is optimized such that the uniformity of the dual-layer-based total CDU is maximized through cross-compensating the top-layer CD with the systematic fingerprint of the bottom layer. The total CDU metric encompasses the cumulative errors in global CDU, optical proximity correction (OPC), local CD, and placement errors as delineated in the EPE budget wheel.

Here, to predict the total CDU impact of dose actuation, it is required to determine the EPE sensitivities to dose of the critical features considered for optimization. Furthermore, we set constraints on CD per feature to account for CD process window limits for the dose optimization. Then, we use an EPE spec for the overlay optimization. The objective is then to optimize overlay such that the EPE spec is met as much as possible, which should in turn further improve the EPE performance. In other words, finding the optimum overlay setpoint to minimize EPE, as is illustrated in the right-most bar in Figure 2.

As a benchmark to the EPE-aware approach, in this paper, we consider the traditional optimization approach, where dose corrections are optimized to minimize top-layer CD uniformity and overlay corrections are optimized to minimize the overlay residuals. The high-level process flow for the traditional optimization approach and the EPE-aware optimization approach are illustrated in Figure 3 and Figure 4.



Figure 2 – Illustration of the EPE-aware sequential dose and overlay optimization approach [4].



Figure 4 – EPE-aware optimization uses e-beam metrology from both layers together with overlay metrology to improve EPE performance.

Top layer Patternin

metrolog

Global CD

Local CDU

&

placement

## 3. USE CASE DESCRIPTION

metrology

Overlay

metrology

Global CD

Local CDU

&

placement

EPE

The dual-layer use case investigated in this work includes a pitch 36nm semi-random design with about 150 unique features and pitch 40nm regular design with five vias on each metal line. GDS clip of these two targets are shown in Figure 5.



Figure 5 – GDS design of the targets of interest. (a) The semi-random design contains about 150 unique features. (b) The regular design consists of regularly spaced vias on top of metal lines.



A dual damascene like process flow adapted with a self-aligned Via process scheme was chosen as shown in Figure 6. The dual-layer patterning was decomposed into bottom (Metal) and top (Via) layers.

Figure 6 – Process flow showing a dual damascene like process flow adapted with a self-aligned Via process.

BEOL stack deposition was followed by the first layer M1 lithography exposure under an ASML EUV scanner. A positive tone lithography development (PTD) process was chosen to pattern the trenches. A resist on top of Spin-on-glass (SOG) and Spin-on-carbon (SOC) was first patterned. The resist patterns were consequently etched down into the SOG/SOC using a plasma-assisted etching technique in a Tokyo Electron Limited (TEL) equipment, and then transferred into TiN and SiN hard mask layers. The Via layer was then processed using a positive tone lithography development (PTD) process on EUV scanner. The stack consisted of a resist on top of SOG and SOC. The resist patterns were subsequently etched down into the SOG/SOC layers using a plasma-assisted etching technique to allow SEM metrology at this intermediate process step (SOC open). Finally, the patterns were transferred down into the bottom oxide layer to reach the Ru layer.

Large FoV SEM images were collected on both layers independently at the process steps indicated in 5(b) and 5(d). Feature contours were consequently extracted and superimposed to determine the total CDU which is based on the distance between contours of both layers as described in Figure 7. A combination of a semi-dense and dense SEM sampling scheme was selected. In addition, large FoV size with low pixel resolution enabled us to accurately capture the local effects such local CD uniformity and local placement errors.



Figure 7 – Total CDU is constructed by combining eBeam images from both layers.

Angle resolved optical Scatterometry based overlay technique was used to measure overlay. A dense sampling scheme was chosen for all measured fields to capture full overlay frequency range.

The overlay data is then combined with the total CDU data to obtain the full EPE performance as shown in Figure 8.



Figure 8 – EPE is constructed by combining eBeam and optical overlay metrology from both layers.

To set up EPE-aware controller, a total of five wafers (4 uniforms, 1 Focus Exposure Matrix (FEM)) were used to collect EPE data for dose sensitivity and fingerprint determination, cross validation simulation and to define process correction sub-recipes.

## 4. FEATURE GROUPING IN LOGIC

To reduce the number of features for optimization, we developed a grouping method, which combines features with similar behavior into "groups" that can be treated as a population of features with same properties. In our study, we propose a

novel grouping method based on simulated litho metrics. This method combines dimensionality reduction techniques, allowing us to reduce the feature space while preserving relevant information, and subsequent clustering to identify similar groups of features, based on their litho metrics behavior. Notably, our approach considers dose and focus as input parameters, enhancing the interpretability and efficiency of feature analysis. The outcome of grouping for semi-dense layout is illustrated in Figure 9, where features from a large design were grouped based on their lithographical performance. Each color indicates one group.



Figure 9 – Grouping strategy identifies the groups in the semi-random feature. Four groups were identified using the grouping method.

## 5. EXPERIMENTAL RESULTS

The results were acquired from three sets of wafers: (1) a FEM wafer to calculate EPE sensitivities to dose and focus, (2) four uniform wafers with no process corrections to measure EPE and calculate the control recipes, and (3) six wafers tor cross-validation. Based on grouping outcomes, we measured the suggested critical features' EPE performance and fingerprint to represent the overall EPE performance per design (regular, semi-random logic) from the 4 uniforms wafers. Multi-feature control method, which allows trade-off between fingerprints, was used to determine the optimum corrections in control. A k-fold cross-validation simulation is done for both traditional and EPE-aware controllers.

#### 5.1 EPE Sensitivity analysis

As preparation for the optimization work, we need to estimate the sensitivity of EPE and its components (local and global) to dose. Metrology collected from a FEM wafer was used to calculate the sensitivities of CD, LCDU, mean total CDU and std total CDU. Figure 10 shows the sensitivities of all the features. The local terms (LCDU and std total CDU) are insensitive to dose variations whereas the CD global terms can be described as linear functions of dose. Therefore, local terms exhibit significantly lower sensitivity as compared to global terms. Furthermore, as shown in Table 1, the sensitivities are different for each feature and the total CDU sensitivity can be approximated by CD/2 + PE.

| Sensitivity to dose [nm/%] |       |       |       |      |        |      |        |      |         |       |
|----------------------------|-------|-------|-------|------|--------|------|--------|------|---------|-------|
|                            | lso l |       | lso0  |      | Densel |      | Dense0 |      | Regular |       |
| CD                         | 0.20  |       | 0.22  |      | 0.18   |      | 0.21   |      | 0.11    |       |
| LCDU                       | -0.03 |       | 0.00  |      | -0.01  |      | -0.03  |      | -0.04   |       |
| PE                         | 0.00  |       | 0.00  |      | 0.02   |      | -0.03  |      | 0.00    |       |
| LPE                        | -0.02 |       | 0.01  |      | 0.04   |      | 0.01   |      | -0.01   |       |
|                            | Ν     | S     | Ν     | S    | Ν      | S    | Ν      | S    | Ν       | S     |
| mean(total CDU)            | -0.09 | 0.10  | -0.11 | 0.11 | -0.11  | 0.06 | -0.07  | 0.12 | -0.05   | 0.05  |
| std(total CDU)             | -0.01 | -0.01 | 0.00  | 0.00 | 0.01   | 0.00 | -0.01  | 0.01 | -0.01   | -0.01 |
| extreme(TOTAL<br>CDU)      | -0.12 | 0.13  | -0.11 | 0.09 | -0.06  | 0.06 | -0.09  | 0.09 | -0.09   | 0.09  |

Table 1 – Sensitivity of EPE components to dose for all the features in the experiment.



Figure 10 – Total CDU and CD sensitivity to dose of different features.

#### **5.2 EPE set up – fingerprints**

In the setup phase, four wafers without process corrections have been measured (both layers with SEM and overlay) to assess the EPE performances of each feature. Figure 11 shows the mean overlay (over four wafers) and the wafer-to-wafer variation. Figure 12 shows that the average total CDU fingerprints (average of 4 wafers) are different for each feature. Figure 13 shows the mean plus  $3\sigma$  of all the measurements (four wafers) per feature. The features with the highest values, iso0 north and iso1 south, are identified as the critical ones. Therefore, these features are used as the driving features in the EPE -aware optimization whereas the others are monitored to stay within bounds and specs.



Figure 11 – Measured overlay. Left: average over four wafers, right: wafer to wafer variation among four wafers.



Figure 12 – Total CDU per feature, average over four wafers (setup).

#### 5.3 Wafer to wafer variations

Figure 14 shows the wafer-to-wafer variation ( $3\sigma$  of the data after subtracting the mean wafer) per feature. We can see that different features are affected differently.

Figure 15 shows the comparison between the data of the setup wafers (four wafers) and the cross-validation wafers (six wafers). Ideally lot to lot differences should be minimized to optimize performance.



Figure 13 – Total CDU and overlay measured in the setup wafers. The largest values, iso0 north and iso1 south, are identified as critical and used as the driving features in the EPE-aware optimization.





Figure 15 – Delta EPE mean fingerprints difference for an example feature (dense 1 south).

#### 5.4 EPE-aware optimization simulation by self-correction and cross-validation

With the measured data from the setup wafers, we calculate dose and overlay corrections for Traditional and EPE-aware control according to the data flow shown in Figure 3 and Figure 4. In Figure 16, we can see the differences between the correction recipes of both methods (traditional and EPE-aware). The mean values (across wafer) remain similar, however the fingerprints are slightly different.



Figure 16 – Dose and overlay corrections for traditional and EPE-aware control.

In simulation results, as shown in Figure 17, the EPE-aware control method shows a performance improvement in comparison to the traditional optimization in terms of EPE (max per die): 0.6nm in setup (self-correction) and 0.3nm in cross-validation. This 0.3nm EPE reduction leads to a 2% Dies-in-spec increase. The performance per feature data shows that the features with high EPE numbers always improved (or are stable) when using EPE-aware optimization and the features with low EPE numbers are re-balanced and remained within the EPE spec (10nm).



Figure 17 – Performance comparison between setup and cross-validation simulations.

## 6. SUMMARY

In this paper we presented the methodology to enable EPE-aware process control set-up for a dual-layer, multi-feature Logic use-case. Starting with a grouping methodology to enable efficient metrology, which combines the multitude of features into a comprehensive number of groups, with optically similar EPE behavior through dose. We have shown by experimental validation that groups can exhibit different EPE behavior through dose and have different spatial wafer-scale EPE fingerprints. With these two pre-requisites, we have shown how to set up a process control recipe to optimize the EPE performance. Via cross-validation we have concluded that verification of such EPE-aware process control set-up can show sufficient EPE reduction, which must be validated with a large multi-wafer data set (signal to noise ratio) in which the inter-lot fingerprint variability and inherent intra-lot variability must be minimized. The needed number of wafers will be determined by the fingerprint stability (from 1 lot to the next) and by the intrinsic intra-lot variation.

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#### References

- J. Mulkens, M. Hanna, B. Slachter, W. Tel, M. Kubis, M. Maslow, C. Spence, V. Timoshkov, "Patterning control strategies for minimum edge placement error in logic devices", Proc. SPIE 10145 (2017)
- [2] R. Anunciado, J. Lee, E. Barzegar, S. van der Sanden, G. Schelcher, S. Schoofs, "Early defect detection for EUV self-aligned litho-etch litho-etch patterning with EPE", Proc. SPIE 12292, International Conference on Extreme Ultraviolet Lithography 2022, 122920J (2022)
- [3] C. E. Tabery, V. Rutigliani, S. Hastings, E. de Poortere, L. Wang, P. Leray, G. Schelcher, Y. Wang, "Voltage contrast edge placement estimation for Overlay, CD, and local uniformity metrology (Conference Presentation)", Proc. SPIE 10959, Metrology, Inspection, and Process Control for Microlithography XXXIII, 109591U (2019)
- [4] I. Kwak, N. Kim, I. Yim, J. Lee, S. Y. Lee, C. Hwang, P. Brandt, K. Lyakhova, M. Mueller, F. Kamalizadeh, A. Corradi, Yun-A Sung, T. Kim, S. Smith-Meerman, S. van der Sanden, Sung-Min Park, B. Boo, Hyok-Man Kwon, "EPE-aware process optimization for scanner dose and overlay in DRAM use case", Proceedings Volume 12496, Metrology, Inspection, and Process Control XXXVII; 124960N (2023) https://doi.org/10.1117/12.2658274
- [5] H. Dillen, W. Tel, J. Karssenberg, J. Mulkens, R. Anunciado, Y. Zhang, K. Nechaev, Z. Khalik, "The edge placement error characterization and optimization for advanced logic and DRAM nodes", Proc. SPIE 12496, Metrology, Inspection, and Process Control XXXVII, 124960O (30 April 2023); https://doi.org/10.1117/12.2658832