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Impact of Solder Voids on IGBT Thermal Behavior: A Multi-Methodological Approach

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Abstract: This study investigates the thermal behavior of Insulated Gate Bipolar Transistors (IGBTs) with a focus on the influence of solder voids within the device. Utilizing a combination of Finite Element Method (FEM) simulations, X-ray imaging, and SEM-EDX analysis, we accurately modeled the internal structure of IGBTs to assess the impact of void characteristics on thermal resistance. The findings reveal that the presence and characteristics of solder voids—particularly their size, number, and distribution—significantly affect the thermal resistance of IGBT devices. Experimental measurements validate the FEM model's accuracy, confirming that voids disrupt the heat flow path, which can lead to increased thermal resistance and potential device failure. Five regression models, including Gaussian process regression (GPR) and neural networks, were employed to predict the thermal resistance based on void characteristics, with the GPR models demonstrating superior performance. The optimal GPR RQ model consistently provided accurate predictions with an RMSE of 0.0050 and R^2 of 0.9728. Using the void percentage as the only input parameter for the regression models significantly impacted the prediction accuracy, showing the importance of the void extraction method. This study shows the necessity of minimizing solder voids and offers a robust methodological framework for a better prediction of the reliability of IGBTs.

Keywords: finite element method (FEM); Gaussian process regression (GPR); insulated gate bipolar transistors (IGBTs); machine learning; power electronics reliability; solder voids

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1. Introduction

IGBTs are standalone power electronic devices widely employed in marine, automotive, and green energy production and delivery systems [1–3]. IGBTs consist of various materials like silicon, copper, ceramic substances, soldering blends, and composite materials [4], leading to significant differences in expansion properties. The significant differences in expansion properties between these layers create complications. Consequently, IGBT assemblies often experience recurring thermal stress during normal operations and rapid testing, leading to fatigue-related deterioration.

Die-attach solder joint thermal fatigue is a common failure mechanism seen in IGBTs [5–7]. During temperature cycling, solder layers and bonding wires, having weaker material characteristics, are prone to breaking and separating. Studies [8–10] have shown that imperfections in the solder layers of IGBTs frequently begin at the periphery. As the deformation accumulates, fatigue or cracks develop within the solder layer [11]. The continuous formation and growth of microscopic defects due to temperature variations are largely considered the main causes of fatigue-related failures in solder alloys [12,13]. This fatigue failure in die-attach solder leads to increased thermal resistance between the junction and the case ($R_{th(j-c)}$), eventually triggering thermal runaway in IGBT chips [14,15]. This, in turn, affects the heat flow channels and heat transfer effectiveness of the device, intensifying

the rise in the junction temperature. Increased junction temperatures are the primary reason for IGBT module failures, making precise junction temperature measurements essential for tracking and assessing the modules' lifespan [16].

Present methods for estimating IGBT device temperatures include mathematical approximation techniques such as the Foster and Cauer models, alongside 3D finite element simulations [17]. Typical strategies for observing junction temperatures consist of optical methods, physical methods, temperature-dependent electrical parameter approaches [18], and thermal network model schemes [19].

However, the conventional thermal network model has limitations, notably its reliance on fixed parameter values and failure to account for the gradual deterioration of material heat transmission characteristics [20]. Without regular updates to thermal models, it becomes increasingly difficult to predict the device's thermal behavior accurately. This discrepancy between estimated temperatures and actual values, especially considering safety margins specified in datasheets, leads to inaccuracies in junction temperature prediction and potential device failures [21]. It is crucial to have accurate data on the maximum temperatures and temperature cycles over the device's lifetime to minimize thermomechanical stress and enhance device reliability.

Effect of Solder Voids on the Thermal Behavior of the IGBTs

Solder layer voids are an inevitable aspect of production that reduces the efficiency of the IGBT components' heat dissipation [22]. These voids cause a higher thermal impedance, hindering the transmission of heat from the chip. As the void fraction increases, the power semiconductor's heat discharge rate decreases, causing an increase in the junction temperature, which accelerates the IGBT's failure [23]. In addition, rising junction temperatures can cause bond wire wear, hastening other types of failures [24]. Localized hot spots and thermal runaways can develop as joint temperatures increase. It is important to note that the degradation of the IGBT component is a likely consequence of the voids present [24]. In fact, these voids can be categorized into three different types, as per common industry practices [14]: The first type is microscopic Kirkendall voids, which are typically found near the interface, arising from differing diffusion rates between the materials. The second type is small voids that form due to thermal cycling fatigue, while the third type is numerous voids generated during production. Studies have shown that the presence of both large and small voids can reduce the lifespan of IGBT packages [25,26]. Additionally, the reliability of solder joints is directly linked to the percentage, position, and dispersion of voids [27,28]. In [14], it has been found that the wear life of the solder layer is inversely proportional to the percentage of voids present. They also investigated the process-induced gaps in lead-free solder junctions subjected to thermal cycling using finite element modeling. They discovered that the fatigue lifespan was directly proportionate to the void volume percentage. Furthermore, the location of the voids can also impact their development and initiation. While voids do not necessarily compromise solder connections when located far from potential points of failure, research into the effects of gaps in solder joints typically focuses on thermomechanical fatigue.

Figure 1 displays X-ray images of both new and old IGBTs in a PV inverter that was deployed in actual residential PV systems. In certain instances, when analyzing chips, such as the IXTP, it may be observed that the voids tend to aggregate and coalesce toward the center of the chip. For the FGH40N60 case, it is observable that the smaller voids primarily migrate toward the edge of the chip or coalesce together to form larger voids. In this IGBT, the higher void percentage and the presence of gray areas in the center of the solder layer may be due to issues with the composition growth in the solder layer. The gray areas in the center of the solder layer may also indicate a problem with the soldering process or the quality of the solder itself.

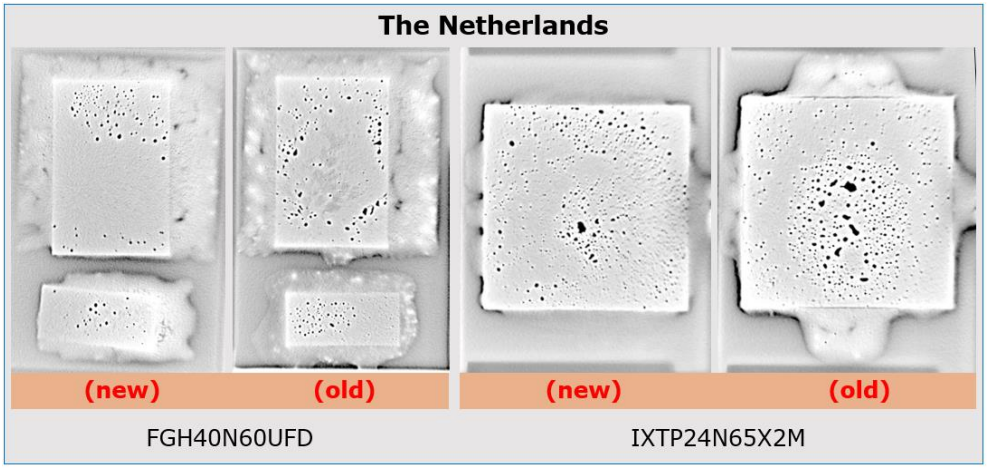


Figure 1. A comparison of the solder void patterns observed in new and old IGBTs taken from a commercial PV inverter installed in the Netherlands.

The observation of different types of void patterns in different cases highlights the complex nature of failure mechanisms in semiconductor devices. Overall, it is crucial to address the issue of voids in order to maintain the reliability and lifetime of IGBT components and solder joints.

A comprehensive understanding of the relevant mechanisms at play under these conditions is paramount, hence the need for a physics-of-failure approach to thoroughly investigate and comprehend the situation. The novelty of this work lies in its contribution to understanding the impact of solder defects on the IGBT's die surface temperature distribution. Previous studies have only partially explained the effect of cracks and voids on the thermal resistance and maximum junction temperature. This study takes a more comprehensive approach by characterizing the microstructure of the defects and assessing their relative importance in causing the R_{th} increase. Furthermore, the use of FEM and analytical expressions to model the temperature distribution provides a more accurate and reliable prediction of the thermal behavior of the IGBT. The integration of machine learning into the model for predicting the thermal resistance during the aging process of the solder layer further enhances the novelty of this work.

2. Three-Dimensional Finite Element Method (FEM) Model of IGBTs

The IGBT package encompasses the IGBT silicon chip, diode chip, lead-rich lead-tin solder, and copper substrate. The selected 700 V/40 A discrete IGBT (FGH40T70SHD) features one IGBT and one anti-parallel diode chip, denoted by Q and D, respectively. The package dimensions significantly influence the simulation accuracy, necessitating precise measurements. Initially, X-ray radiography is used to visualize the internal components of the IGBT, which can be distinguished by differences in the size, density, and composition. An FEI Quanta 200F FEG-SEM with a Thermo Fisher UltraDry silicon drift EDX detector and Pathfinder X-ray microanalysis software (version 2.0.2) is used to capture numerous cross-sections of the IGBT under study in different orientations [29]. By capturing primary electron (PE) and secondary electron (SE) images at low magnification and backscattered electron (BSE) images at high magnification, we will be able to gain a better understanding of the different interior components of the IGBT.

Figure 2 is a detailed representation of an IGBT device and its internal construction. The IGBT comprises several layers of different materials, such as a silicon chip, a Cu baseplate soldered using 88Pb-6Sn-6Ag, and an aluminum bond wire that is connected to the chip. Additionally, the device is protected by an epoxy molding compound (EMC) that contains a SiO_2 infill. Table 1, sourced from CES Edupack and MatWeb, provides further information on the characteristics of these materials.

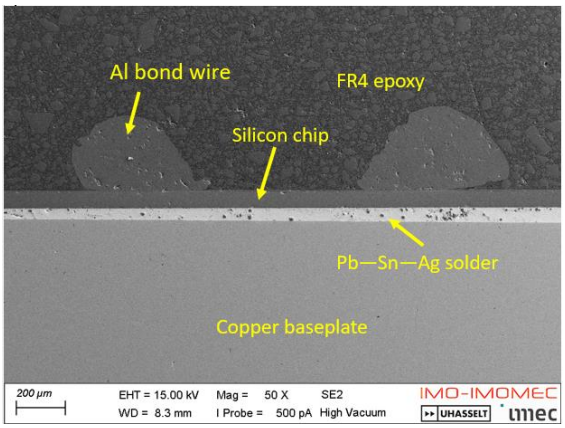


Figure 2. Cross-section of the IGBT being tested, showcasing the various material layers.

Table 1. Layer-by-layer breakdown of IGBT material's thermal and physical properties.

	Solder Pb-Rich	Silicon	Aluminum	Copper
Thermal conductivity [W/(m-K)]	60	131	210	398
Heat capacity [J/(kg-K)]	167	700	900	385
Density [kg/m^3]	8400	2329	2700	8930

The physical dimensions of the IGBT were extracted from both the X-ray images and the datasheet. The material information for each layer was also obtained and the thermal and mechanical parameters for these materials were sourced from established databases. Using this information, the IGBT's FEM model was accurately created in the COMSOL Multiphysics environment, as shown in Figure 3.

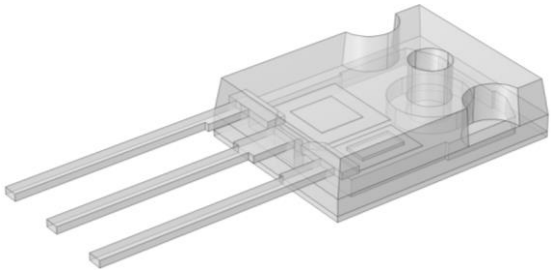


Figure 3. The completed geometry of the IGBT model implemented in the Finite Element Method (FEM) environment.

It is worth noting that the IGBT's various components, such as the dies, solder, and binding wires, have distinct coefficients of thermal expansion (CTEs). As a result, the device is subject to a significant amount of thermal stress, from which may arise challenges due to the differences in the CTEs among its material layers.

2.1. Solder Void Extraction

The methodology discussed here explains the steps required to extract the shape, size, and location of the voids from an X-ray image of an IGBT. The following is a detailed discussion of each step, as shown in Figure 4:

1. Black and white thresholding: The first step involves converting the grayscale X-ray image to a binary image by applying a threshold value between 30 and 150. This separates pixels into black and white, where white pixels indicate intensities above the threshold, representing potential void areas.

2. Cleaning small white areas: In the next step, the image is cleansed of small white areas. These areas can be noise or small defects that are not relevant to the analysis. Only the white pixels larger than 10 pixels are retained in the image. This step ensures the total void percentage remains constant, calculating the actual void area (act) as the ratio of white pixels to black pixels.
3. Inverse image: The color of the image is inverted from black and white to white and black. This is performed so that the voids will appear as black regions surrounded by white lines.
4. Void identification: In this step, a program is used to detect voids, extracting their size and location by identifying black regions outlined by white. The program replaces different-shaped voids with circles of an equivalent diameter and modifies the radius of these circles based on the actual void area ratio:

$$Radius_{new} = Radius_{old} \times \sqrt{\frac{act}{circ}} \quad (1)$$

5. Finally, it may be helpful to manually inspect the analysis results to verify the accuracy of the void identification, ensuring all the relevant features are captured.

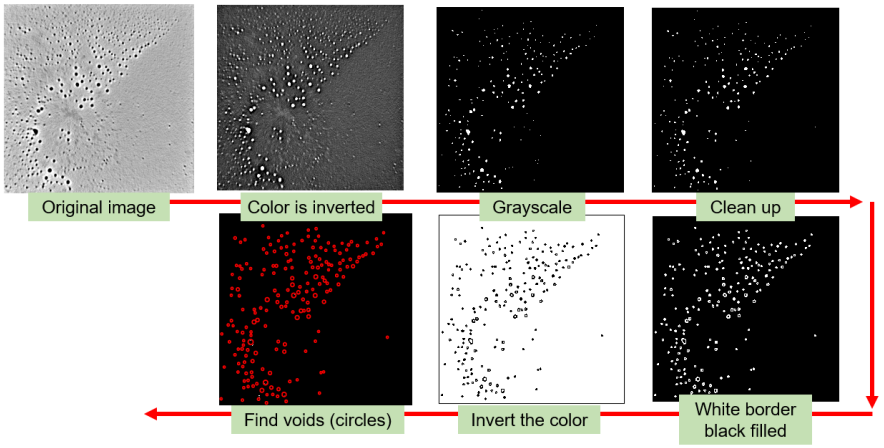


Figure 4. The void extraction procedure involved analyzing X-ray images of the solder layer to identify and extract voids using image processing techniques.

The above methodology can be automated using image processing software, such as MATLAB® (R2022a) or Python (v3.7), which have built-in functions for thresholding, image cleaning, and object identification. Here, a customized program is designed to fit the specific requirements of the IGBT analysis. Once the voids are identified and their size and location are extracted, the data can be used for further analysis, such as defect quantification and implementation in the FEM simulation.

2.2. FEM Simulation

Once the necessary materials and measurements are obtained for the internal elements of the IGBT, the outer packaging dimensions can be determined using their corresponding datasheets. This, in turn, allows for the creation of a 3D-CAD model of the examined IGBT device within the COMSOL Multiphysics® environment. The resulting model is presented in Figure 5, which also displays an RA-T2X-25E heat sink and a thermal pad serving as a thermal interface. To account for any solder voids, X-ray images of the IGBT under examination are used to incorporate these voids into the FEM model. These solder voids are considered hole-through, meaning they traverse the entire thickness of the solder layer.

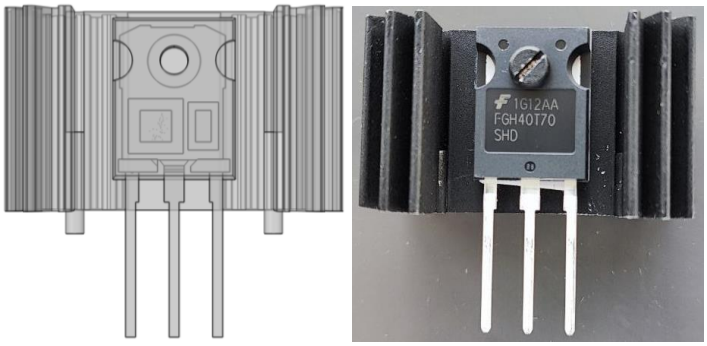


Figure 5. The modeled IGBT mounted on an RA-T2X-25E heat sink.

Heat transfer physics, encompassing conductive, convective, and radiative heat transfer, are also incorporated for each distinct material layer. The bond wires are omitted from the 3D model to streamline and expedite the FEM simulation, as well as to avoid issues with the meshing (the current mesh includes 116,520 domain elements). A previous study [30] demonstrated that including bond wires in the FEM model does not significantly affect the estimation of the junction temperature. The number of degrees of freedom (DOFs) amounts to 185,209 (plus 95,143 internal DOFs). The initial temperatures are set to match the ambient temperature (24 °C). Each FEM computation requires approximately 20 s to complete (utilizing an Intel® Core™ i7-9750H CPU and 16 GB RAM). The IGBT chip's temperature increases due to power dissipation while a uniform convective heat flux is applied to the baseplate's backside. Thermal insulation is incorporated into the remaining FEM domains/boundaries. The highest surface temperature of the chips is regarded as the junction temperature. The investigated IGBT features a copper baseplate and a Pb-Sn-Ag solder layer. Given the difficulty in determining the thermal and physical properties of this specific solder composition, a standard lead-rich Pb-Sn solder is used as the solder layer in this instance. The heat capacity (C_p) and thermal conductivity (κ_p) for silicon, the copper baseplate, solder layer, and aluminum are temperature-dependent.

2.3. Experimental Measurements

For this research, a 40 A/700 V discrete single IGBT mounted on a heat sink with natural convection is examined. A thermal pad with a thermal conductivity of 12.5 W/mK is used as the interface between the baseplate and the heat sink [9]. A DC-DC converter supplies a constant gate voltage of 15 V. A direct measurement of the IGBT's junction temperature (T_j) is impractical due to potential damage to the chip, so the collector–emitter voltage (V_{CE}) at a low current (100 mA) is used as the temperature-sensitive electrical parameter (TSEP) for estimating the T_j [8]. The sensing current, only 0.25% of the rated current, minimizes self-heating, ensuring it does not affect the V_{CE} calibration [9].

To establish a linear relationship between the V_{CE} and temperature, the IGBT is placed on a uniformly heated hot plate, adjusting the hot plate to set temperatures over extended periods. This method is repeated at various temperatures to define a linear V_{CE}-T_j curve, visualized in Figure 6. The calibration is conducted in a climate chamber, verifying the consistency at temperatures up to 70 °C. However, the V_{CE} cannot monitor the junction temperature during a high current flow; it is only measured during cooling or after the current is turned off [10]. In this study, the IGBT is subjected to currents of 5 A, 7.5 A, and 10 A, each for five minutes, to allow for the stabilization of the voltage and current. Here, the currents up to 10 A have been chosen for the experimental measurements rather than applying the IGBT's full rated current of 40 A. In practical applications (such as commercial PV inverters), such currents are generally lower to prolong the lifespan of these components, which are susceptible to failure under high thermal stress. These experiments are designed to mimic these real-world conditions. The voltage at each chip's end is recorded before the current shutoff, aiding in calculating the power dissipation (e.g., 8 W at 7.5 A).

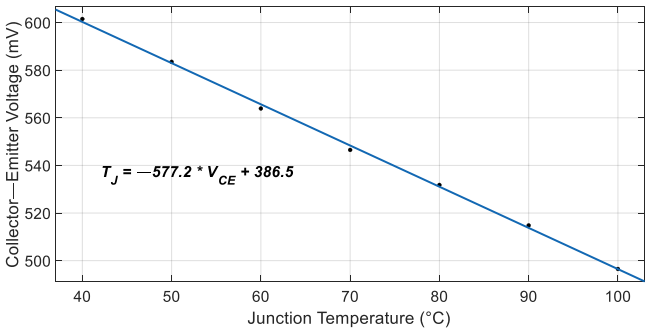


Figure 6. The calibrated V_{CE}-T_j curve for the IGBT under test.

Using the V_{CE}-T_j curve, an oscilloscope set to trigger mode captures the voltage drop across the IGBTs 200 µs after the current cutoff. The resulting junction temperature is then calculated from the V_{CE} waveform, presented in Figure 7. The junction temperature during the cooling phase is shown in Figure 8. Due to the delay in reaching electrical equilibrium and potential noise interference, the junction temperatures are rounded to the nearest value to ensure reliability, estimated at 52 °C, 62 °C, and 70 °C based on power losses. More precise temperatures at the time of the current cutoff are extrapolated from 200 µs to 0 s, fitting a second-order exponential curve to the data points [11]. The predicted junction temperature is within 1 °C of the corrected value. For high-current testing, two 70 A parallel-connected relays are used.

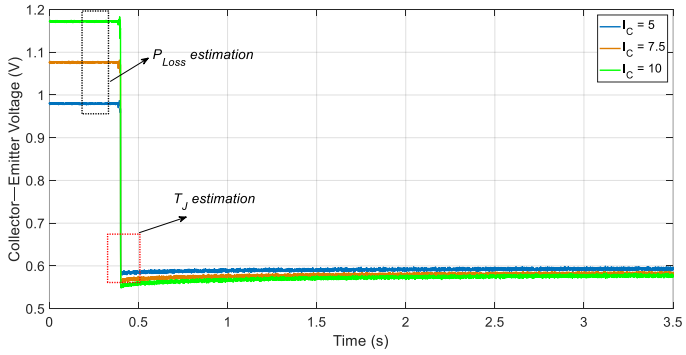


Figure 7. The V_{CE} waveform at the high current cutoff point.

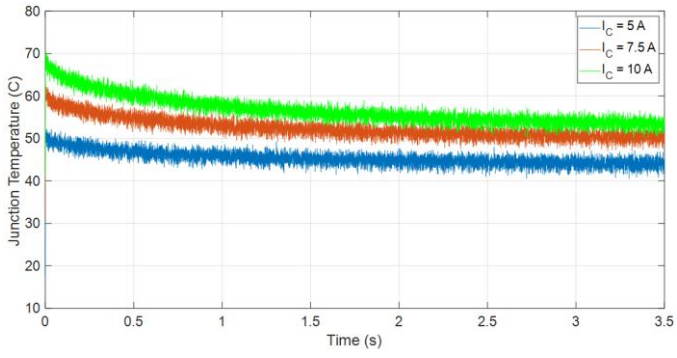


Figure 8. The measured junction temperature curve during the cooling phase.

The heat transfer coefficient value is determined by comparing the steady-state temperature points attained by applying various currents with the temperature anticipated from the FEM model. To find the heat transfer coefficient, an optimization algorithm using the Nelder–Mead method is employed, which minimizes the error between the actual

steady-state temperatures and the estimated temperatures from the FEM. The constraint range of the solver is set between 0 and 100 W/m^{2}K.

Additionally, power losses are applied based on the time-dependent experimental measurements over a 5 min period. The heat transfer coefficient is adjusted to match the estimated IGBT junction temperature with the measured junction temperature in practice. After 30 iterations, the optimal value of h is determined, as shown in Figure 9. The objective function is defined as follows:

$$obj = \min\left\{\sum\left(\left(T_{j\_IGBT} - T_{j\_EXP}\right)^2\right)\right\} \quad (2)$$

where T_{j_EXP} is the actual temperature measurement. By minimizing this function, the most appropriate heat transfer coefficient for the system is identified.

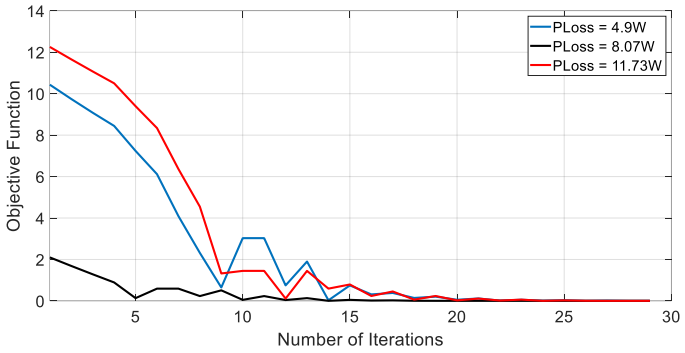


Figure 9. Nelder–Mead optimization's objective function versus the number of iterations, demonstrating the convergence of the optimization algorithm over time.

To determine the power loss, we need to multiply the collector–emitter voltage by the collector current just before the high current is cut off. After this step, we can obtain the heat transfer coefficient for the heatsink that is being used. This calculation is performed in terms of applied power losses, with an error of less than 1 °C in temperature estimation. The results are shown in Figure 10.

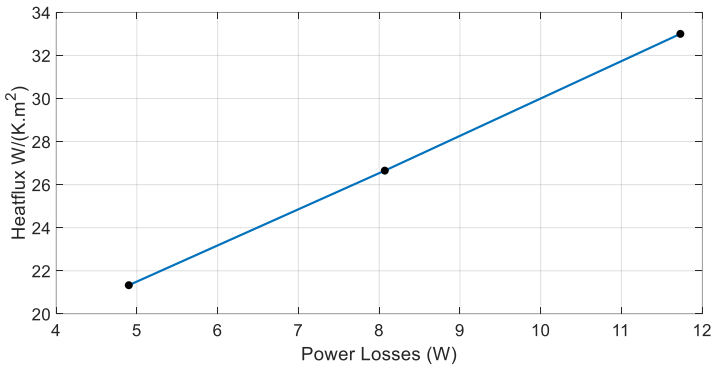


Figure 10. The heat transfer coefficient of the utilized heatsink plotted against the applied power dissipated.

It can be seen that the trend in Figure 10 is consistent with previous studies on this subject [31]. To obtain the chip heat flux in the FEM model, Equation (3) can be used:

$$H = \frac{P_{Loss}}{V_{chip}} \quad (3)$$

In this equation, the heat flux is denoted by H, the device's heating power consumption is symbolized by P_{Loss}, and the chip's area is represented by V_{chip}. The overall power, P_{Loss},

consists of the IGBT turn-off power usage, turn-on power usage, and operational losses. Nonetheless, given that the gate voltage is continuously applied at its rated value and the gate remains activated, only conduction losses are present. Additionally, other current values are employed to evaluate the suitability of the suggested FEM model, which is capable of delivering precise temperature estimations.

3. Effect of Voids on the Thermal Resistance and Gradient of the IGBT

This study's primary goal is to determine the correlation between solder voids and the thermal resistance from the junction to the case. Among the various stressors in power semiconductors, the temperature, particularly the junction temperature (shown in Figure 11), is considered the most critical factor that leads to wear-out failures in IGBTs. It is also required to represent the heat conduction path from the upper layer (junction) to the lowest layer (case).

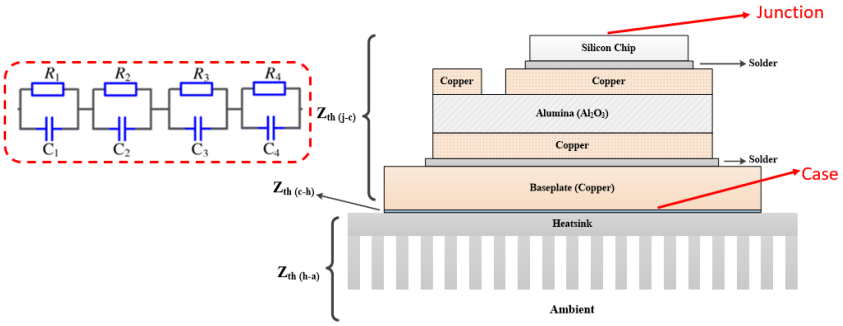


Figure 11. A cross-sectional view of the multilayer structure of a typical IGBT power module.

The thermal resistance (R_{th}) of an IGBT quantifies the device's ability to conduct heat away from its active area to either the backside case or a heat sink. By dividing the temperature difference between the junction and the case by the power dissipated, the thermal resistance can be obtained in the following manner [32]:

$$R_{th(j-c)} = \frac{T_j - T_c}{P_{loss}} \tag{4}$$

The presence of voids in the solder layer can alter this heat flow, potentially affecting the overall performance and reliability of the device. When solder fatigue occurs, it causes an increase in thermal resistance, which ultimately results in a higher junction temperature and on-state resistance [32]. In [33], it is indicated that a 20% increase in R_{th} is a sign of solder fatigue failure. In the case of IGBTs, this increase in thermal resistance indicates that the device has reached the end of its life. The device may continue to operate for a short period after the failure, but it is no longer reliable or safe to use. In this case, the FEM model has been validated with experimental measurements, indicating that the model is accurate and reliable. The initial voids in the solder layer have been removed, and the model is now considered as a reference case for further analysis. The location for measuring the case temperature (T_c) is beneath the center of the silicon chip at the backside of the IGBT. For further investigations, the case with a current of 7.5 A (junction temperature of 62 °C or power losses of 8.07 W) is considered. Two simulation cases were conducted to investigate the impact of voids in the solder layer on the thermal performance of the examined IGBT device. The first simulation case was conducted without any voids in the solder layer, while the second simulation case was conducted with initial voids in the solder layer. According to the FEM simulation, the case with the initial solder void has a thermal resistance of 0.47087 C/W, while after removing these initial voids from the solder layer, the FEM simulation gives us a thermal resistance of 0.46994 C/W. This result indicates an error of 0.19% after removing the initial solder voids, which is negligible. The FEM simulation results show that in the case without voids, the temperature at the junction of

the IGBT chip is uniform across the entire chip. However, by adding voids in the solder layer, some distortion in the uniformity of the temperature gradient of the silicon IGBT chip is observed. Specifically, the presence of voids causes the thermal gradient to be disrupted, and the highest temperature is observed around the largest voids. This effect is shown in Figure 12.

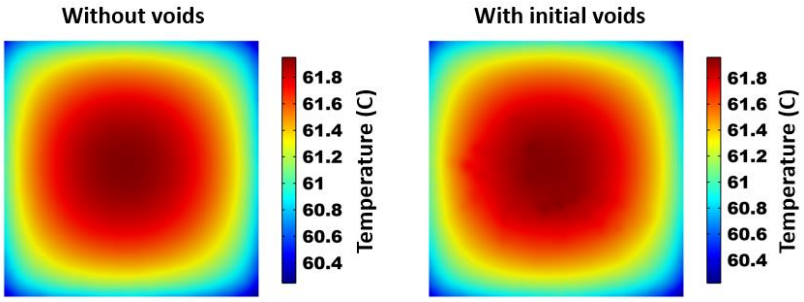


Figure 12. A comparison of the temperature distribution over the IGBT chip with and without solder voids.

3.1. Effect of a Single Void on the Thermal Resistance of the IGBT

To study the effect of voids on the behavior of the system, a single circle-shaped large void was introduced in the model. The radius of the void was 150 µm, and it was assumed that voids cannot appear in the edges to prevent meshing issues. To allow the void to move freely inside the model, a rectangular margin of 3.2 × 3.2 mm was considered as shown in Figure 13a.

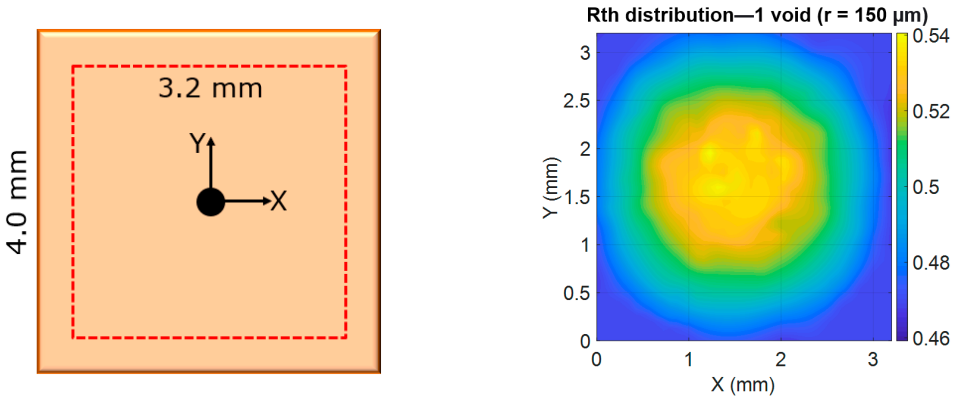


Figure 13. (**a**) A map indicating how voids can be placed across the solder layer; (**b**) the estimated junction-to-case thermal resistance based on the location of a single void with a radius of 150 µm.

The location of the void was varied to assess the impact on the junction temperature and thermal resistance between the junction and case. The results in Figure 13b show that the void's position significantly affects the thermal behavior of the IGBT. Specifically, the results indicate that when the void is placed in the center of the chip, the junction temperature is the highest. In the area around the center of the void, there are noticeable changes in the thermal resistance, particularly within the X range of 1–2 mm and the Y range of 1–2.5 mm. These areas show several peak thermal resistances, causing distortions in what would otherwise be a uniform thermal distribution. Interestingly, these distortions can become even more pronounced when dealing with a smaller circle radius. When the temperature fluctuation in the junction increases, it results in a higher level of viscoplastic strain [34]. This particular observation implies that the location of the void has an impact

on the flow and distribution of the heat within the device, ultimately causing alterations in the device's thermal behavior.

In the second case, the same single void was added, but the radius was increased to 200 µm. Figure 14 shows the temperature distribution for this particular case. When the radius of a circle-shaped void increases, the R_{th} distribution tends to become smoother and more uniform based on the void position. However, despite this smoothing effect, the highest temperature in the system is still typically found at the center of the chip.

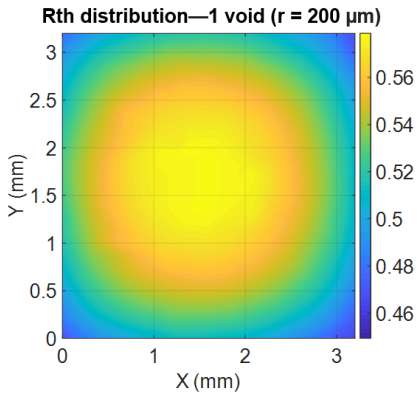


Figure 14. The estimated junction-to-case thermal resistance based on the location of a single void with a radius of 200 µm.

3.2. Effect of Multiple Voids on the Thermal Resistance of the IGBT

To further investigate the effect of voids on the thermal resistance of a solder layer, a second void (radius of 200 µm) was added to the FEM model. The aim was to explore the correlation between the size and position of the two voids and their impact on the thermal resistance R_{th} of the system. Figure 15a shows the effect of the first void's position on the thermal resistance and its distribution. The obtained results are well aligned with the previous cases. Figure 15b shows the distribution of the R_{th} based on the position of the second void. As can be seen, the result in this case is different than the case with a single void. After adding the second void, the temperature and thermal resistance have increased compared to the case with only one void. This indicates that the presence of multiple voids in the solder layer can have a different but significant impact on the IGBT's performance. This difference in thermal resistance is shown in Figure 15c.

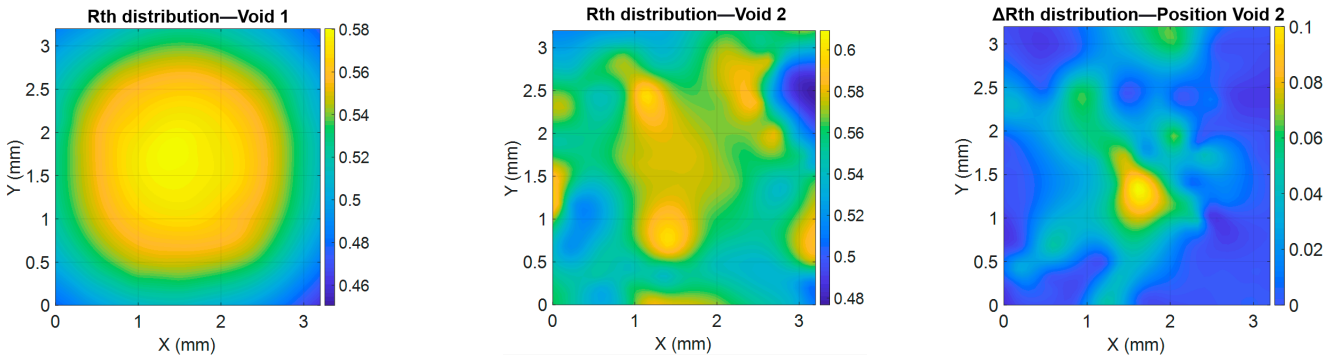


Figure 15. Thermal resistance distributions based on void positioning: (**a**) junction-to-case thermal resistance distribution with respect to void 1 (radius of 200 µm), (**b**) thermal resistance distribution with respect to void 2 (radius of 200 µm), and (**c**) increase in thermal resistance (ΔR_{th}) distribution after introducing void 2 with respect to its positioning.

Surprisingly, the results show that there is no correlation between the thermal resistance of these two cases. Specifically, the addition of a second void does not lead to a huge increase in the thermal resistance of the device (mainly the increase at the center). It can be seen that the presence of multiple voids may disrupt the heat flow path in a way that increases the overall thermal resistance of the device in some specific locations, such as the center of the chip.

In particular, increasing the number of voids can lead to an increase in the device's thermal resistance. To investigate this effect, FEM simulations were performed to estimate the junction temperature in cases with varying numbers of voids. The results of the simulations show that the thermal resistance increases with the number of voids. This finding suggests that the presence of voids disrupts the heat flow path in the device, reducing its thermal conductivity and increasing its overall thermal resistance. Interestingly, the simulations also show that the effect of the first two voids is much higher than the effect of the subsequent voids. The reduced impact of the subsequent voids may also be due to the cumulative effect of the voids already present in the device. As the number of voids increases, the cumulative effect of the voids on the device's thermal behavior may decrease, as the voids interact with each other and disrupt the heat flow path in a less efficient way.

To analyze the effect of small voids on the thermal resistance, we added ten circle-shaped voids of random sizes and locations in the solder layer. Of these ten voids, three were considered "big" with sizes ranging from 150 µm to 250 µm, while the remaining seven were considered "small" with sizes ranging from 10 µm to 50 µm. We compared the results of this case with the cases where only three big voids were present. Our findings show that the presence of small voids has no effect on the thermal resistance or temperature gradient. When comparing the case with 10 voids to the case with only 3 big voids, the maximum error percentage is only 0.0491%. This indicates that there is no significant change in the estimated thermal resistance, even with the addition of small voids.

3.3. Effect of Void Shapes on Thermal Behavior of the IGBT

In practice, the closest shape that can represent solder voids is the ellipse shape. In this study, the effect of voids with different shapes on the thermal resistance R_{th} has been investigated. The first step was to focus on studying the impact of ellipse-shaped void rotation on thermal resistance. Figure 16a shows the results of thermal resistance based on different rotations of a single large solder void.

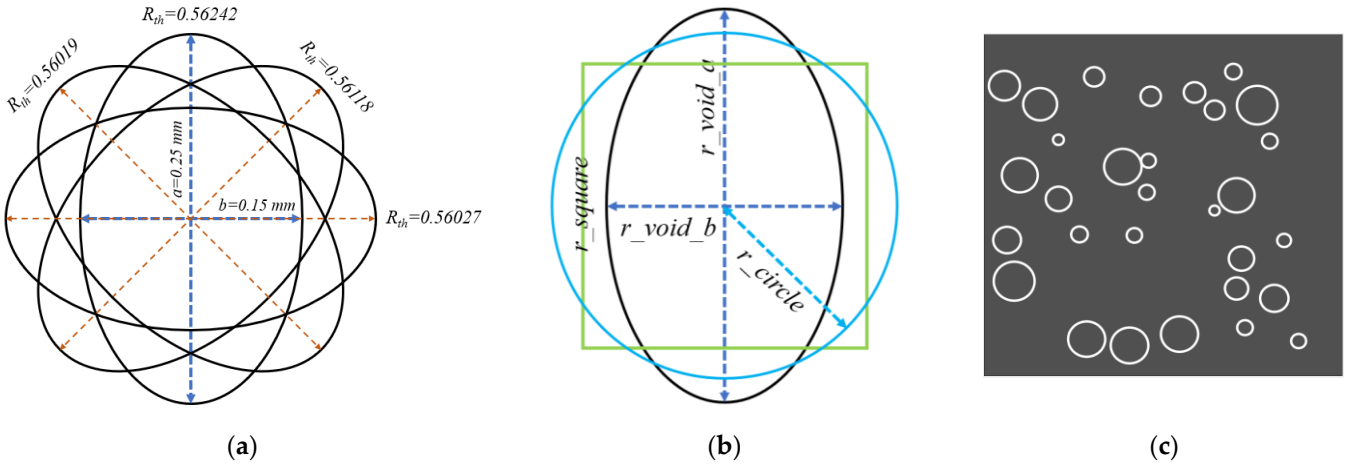


Figure 16. (**a**) The effect of the rotation of a single large ellipse-shaped void on the thermal resistance; (**b**) the equivalent void shapes considered in this study with the identical void area; and (**c**) the implementation of a circle packing algorithm on a square to achieve a desired total number of voids, terminated before completion.

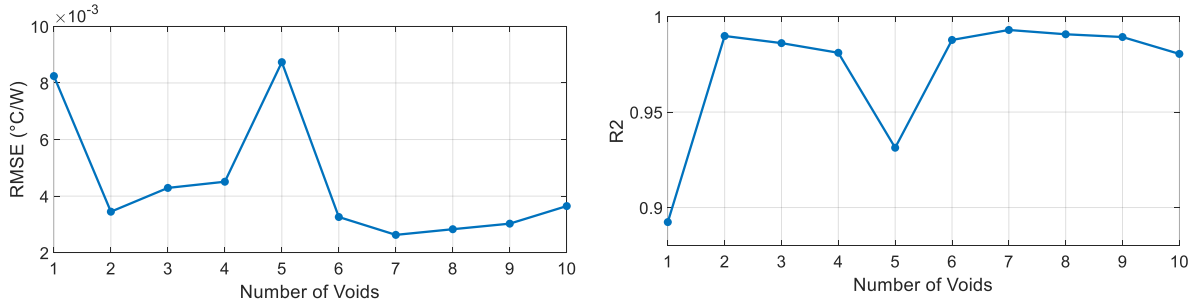
The results show that the rotation of the ellipse-shaped void does have an effect on the R_{th} value. A zero-degree rotation angle results in a thermal resistance of 0.56242 °C/W, while a +45° degree and −45° rotation angle result in a thermal resistance of 0.56118 and 0.56019 °C/W, respectively. These results imply that the void's orientation can cause changes in the heat flow path and distribution, which affect the thermal resistance of the device.

To accurately model the impact of solder voids on the thermal resistance of a system, it is important to analyze the shape of the voids. While circular or square voids may be easier to work with, it is important to determine whether the shape of the voids has a significant impact on the system's behavior. The selected void shapes are shown in Figure 16b.

To compare the impact of different void shapes, a simulation loop was run for 50 iterations, with the position of 10 randomly chosen voids being selected in each iteration. The size of the voids was also randomly selected. As a result, for each number of voids, we will have 50 different thermal resistances with a different position, size, and rotation of the voids. To generate a set of random circles of different sizes and positions within a square, an unconstrained circle packing method was employed [35]. The algorithm for circle packing was halted once the predefined number of circles within the square was reached rather than continuing until the entire square was filled. The main aim of this technique was to generate a cluster of circles randomly placed within the square, without any overlapping. The circle packing problem, which is demonstrated in Figure 16c, refers to the task of arranging a particular quantity of similar circles inside a container, without any overlap [36].

By using the unconstrained circle packing method to generate random circles within a square, the problem is being solved in a heuristic manner. This approach aims to find a feasible solution to the circle packing problem by trying different configurations of circles until a solution is found. Stopping the algorithm when the number of circles in the square reaches the predefined number can have implications for the resulting circle configuration. It is possible that stopping the algorithm early may lead to suboptimal solutions or patterns in the circle configuration. However, if the stopping condition is set appropriately, the method can still generate diverse and non-overlapping circle configurations that satisfy the goal of the circle packing problem. Upon halting the circle packing algorithm at a predetermined number of voids, the dimensions of the circle-shaped voids will be subject to random modification by a stochastic function. This process transforms the original circular voids into marginally smaller oval-shaped voids, thereby introducing an element of variability and irregularity into the packing configuration.

The error percentage (in terms of the RMSE and R^2) between the thermal resistance R_{th} for ellipse-shaped voids and R_{th} for circular or square voids was then calculated. It is important to ensure that the area of each void is the same, regardless of its shape. Figure 17 displays the difference between two cases, one with ellipse-shaped voids and the other with square-shaped voids.

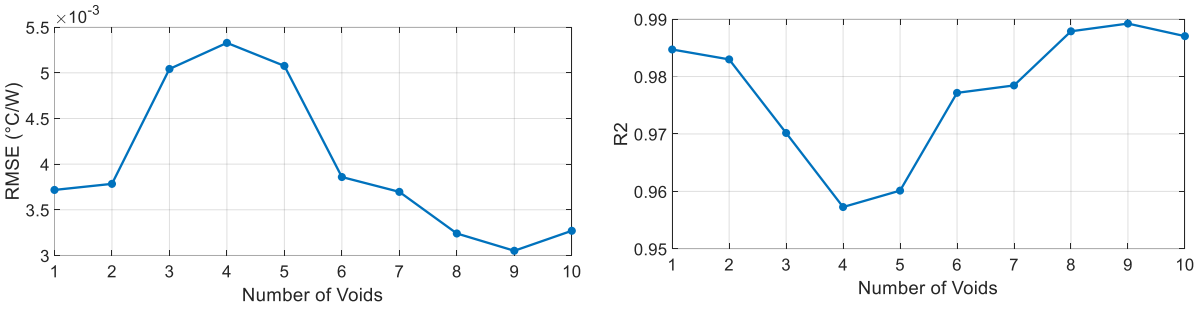


(**a**) (**b**)

Figure 17. A comparison of the RMSE (**a**) and R^2 (**b**) values for ellipse-shaped voids versus square-shaped voids based on the number of voids analyzed.

The results show that the error between the thermal resistance (R_{th}) values obtained for ellipse-shaped voids and square-shaped voids is relatively low. The R^2 value is almost equal to one when the number of voids is greater than two, indicating a strong correlation between the IGBT's thermal resistance with ellipse-shaped and square-shaped voids. However, when the number of voids is five, the error increases, suggesting that the impact of the void shape on thermal behavior may be more significant in certain configurations. The results reveal that the majority of the differences are less than 1%, indicating that there is almost no significant difference between these two cases in terms of thermal resistance.

This finding suggests that when it comes to predicting thermal resistance, using square-shaped voids instead of ellipse-shaped voids may not significantly impact the results. According to [37], the temperature predicted using square voids is being very careful and only differs by less than 1% from the temperature predicted using circular voids. This suggests that the shape of the voids has very little impact on the device temperature. Next, the results of the solder voids in an ellipse shape are compared with those in a circular shape. The error percentages are shown in Figure 18.



(**a**) (**b**)

Figure 18. A comparison of the RMSE (**a**) and R^2 (**b**) values for ellipse-shaped voids versus circle-shaped voids based on the number of voids analyzed.

When the results for ellipse-shaped voids are compared to those for circular voids, the error is quite low, indicating that there is no significant difference between the thermal behavior of the IGBT with ellipse-shaped and circular voids. This finding suggests that, for practical purposes, modeling voids as circles may be sufficient, without a significant loss of accuracy. Moreover, as the number of voids increases, the difference in the thermal behavior between the different void shapes decreases, suggesting that the impact of the void shape on thermal behavior is more significant in configurations with fewer voids.

3.4. Effect of Void Area Percentage on the Thermal Resistance of the IGBT

The next step involved analyzing the IGBT's thermal behavior based on the total solder void percentage. Void percentages of 1% up to 22.5% were considered in the simulation. The voids were randomly placed and sized within the solder layer, but the total void percentage was kept constant for each case. To reduce the effect of randomness in the void placement, the simulation was repeated 20 times for each void percentage, with different void sizes and locations. The thermal resistance from the junction to the case $R_{th(j-c)}$ was measured for each simulation case. Figure 19 illustrates the impact of the solder void area percentage on the IGBT's thermal resistance. As the void area percentage increases, the thermal resistance rises as well. However, the thermal resistances observed are scattered, with some being higher or lower than others. In a different scenario, we introduced a circular void beneath the center of the chip, allowing us to achieve the specified void percentages by adjusting the circle's size. The results show that a single large void has a more significant effect on the thermal resistance compared to multiple smaller voids distributed throughout the area. It can be concluded that the configuration of voids plays a crucial role in the thermal performance of a package. A single large void can considerably

raise the thermal resistance of an IGBT compared to multiple smaller voids with the same total void percentage [38,39].

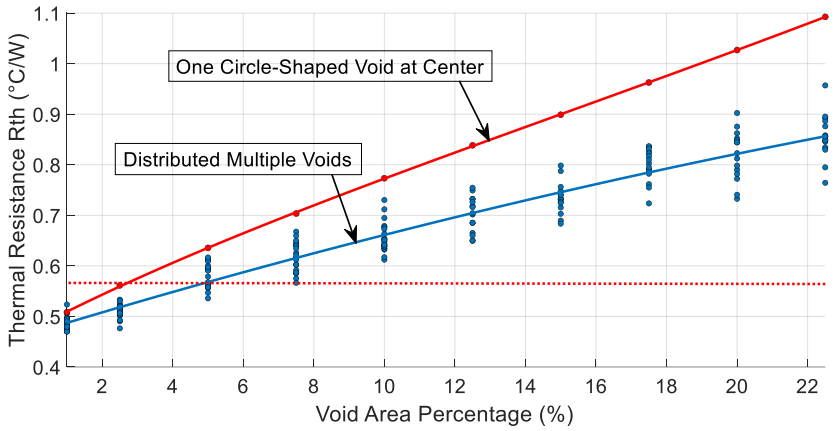


Figure 19. The increase in thermal resistance as a function of the total void area percentage in the solder layer. Excess thermal resistance is represented by the red dashed line, demonstrating a 20% increase from the initial value.

In the analysis, the red horizontal dashed line serves as a reference point where the thermal resistance R_{th} exceeds by 20%. When examining the impact of voids on R_{th}, we observe that with a 5% void, there are some cases where the R_{th} exceeds this limit, while in other cases it does not. However, with a 7.5% void, all 20 random cases show a 20% increase in the R_{th}.

Here, the effect of different void percentages on the IGBT's thermal resistance and transient thermal impedance curve is investigated. The results show that increasing the total void percentage in the solder layer of the device causes an increase in the thermal resistance, as shown in Figure 20. Moreover, the transient thermal impedance curve of the device is extracted for three different void percentages: 1%, 2.5%, and 5%. The results show that these curves have a shift by increasing the void percentage. This shift seems to have a linear correlation with the void percentage. This observation indicates that the thermal capacitance of the solder would also change by changing the void percentage.

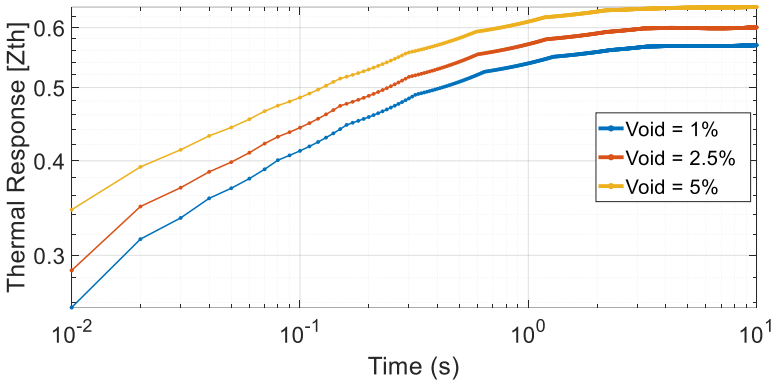


Figure 20. Effect of void area percentage on transient thermal impedance curve.

4. Advanced Regression Modeling for Thermal Resistance Estimation

The primary objective of this section is to determine the thermal resistance of the IGBT by examining the void characteristics, such as their percentage, size, position, and rotation. To achieve this, regression models are employed to establish a relationship between these void properties and the IGBT's thermal resistance, ultimately providing insight into the impact of voids on the device's thermal performance.

In this analysis, two scenarios are taken into account as shown in Figure 21: the first one utilizes the void percentages as input for the regression model, while the second scenario incorporates the void characteristics (such as the size, position, and rotation) as input for the regression models. This approach enables a precise estimation of the thermal resistance in IGBTs based on solder void patterns. Additionally, it facilitates the monitoring of thermal resistance changes should the initial void pattern experience alterations due to degradation.

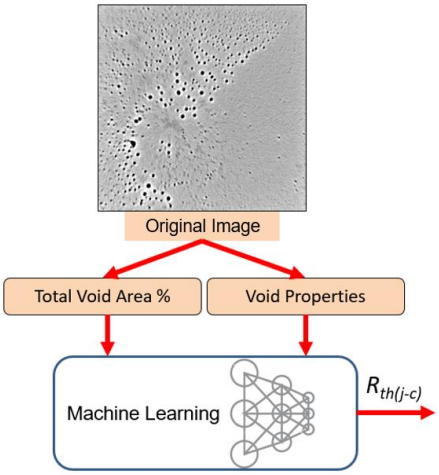


Figure 21. Two techniques for estimating the thermal resistance based on solder void patterns: using void properties such as the size and position as input to the advanced regression models and using the total void area percentage as an input to the regression models.

Before we start discussing the proposed method, it is crucial to give an overview of the regression models used in this study. In order to analyze the relationship between thermal resistance and the features extracted from X-ray images of IGBTs, we applied several regression models. These models are as follows:

1. Linear regression.
2. Support vector machine (SVM).
3. Tree regression (Fine-Tree).
4. Gaussian process regression (GPR).
5. Artificial neural networks (NNs).

These regression models have been trained and validated on the dataset to identify the best model for estimating the thermal resistance based on the features extracted from the X-ray images of IGBTs.

- **Linear Regression:**

Employing linear regression as a statistical technique allows for the forecasting of connections between a continuous outcome variable Y and multiple explanatory variables $X_1, X_2, \ldots, X_p$ [40]. The regression function is modeled as a linear combination of predictors, making it a simple and popular choice for many applications. One of the reasons for its popularity is the ease with which the model parameters can be interpreted.

The linear regression model can be specified in matrix form as:

$$y = X\beta + \varepsilon \tag{5}$$

where $y = [y_i]_{n\times 1}$ is an n-dimensional response vector, $X = \left(x_{ij}\right)_{n\times(p+1)}$ is an $(n \times p + 1)$ design matrix with the first column being a vector of 1 s, and $\varepsilon = [\varepsilon_i]_{n\times 1}$ is the error term.

While linear regression models have several advantages, such as ease of interpretation, they are highly sensitive to outliers, which can severely degrade the predictive accuracy of the resulting linear model [41].

- **Tree Regression:**

Examining and evaluating data patterns and processes can be effectively performed using tree regressions [42,43]. They provide multiple benefits, such as versatility in managing various response variable types and remaining stable under monotonic changes in the explanatory variables. The process of building trees is relatively uncomplicated, and interpreting them is accessible, even for those without expertise. A variable X is referred to as an ordered variable when its numerical values possess an inherent sequence. Otherwise, it is considered a categorical variable [44].

For any given node t, let us represent the collection of training data within t as $S(t)$ and the average value of Y within t as $\overline{y}_t$. Moreover, we can represent the "impurity" of node t with $\emptyset(t)$. To ascertain the optimal method for dividing nodes, AID employs a mathematical equation known as the sum of squared deviations: $\emptyset(t) = \sum_{i \in S(t)} (y_i - \overline{y}_t)^2$. This equation computes the cumulative impurities for every child node, selecting the split that results in the lowest sum of impurities. The smallest quantity of training samples needed for determining the output of each leaf node is referred to as the minimum leaf size (here, this is 4). While constructing a regression tree, it is crucial to balance both its simplicity and ability to predict. Typically, a detailed tree comprising numerous tiny leaves demonstrates high precision on the training data but might not achieve the same degree of precision on an independent test set [45].

- **Support Vector Machines (SVMs):**

The SVM was first introduced by Vapnik in 1995, initially designed to address classification problems but later expanded to handle regression issues as well [46]. The fundamental principles of SVMs stem from long-standing computational theories, such as hyperplane margins [47]. An SVM began as a linear classifier and eventually evolved to handle nonlinear issues, recognizing that most real-world problems are not linearly separable.

To put the SVM concept in simple terms, it involves finding the optimal hyperplane to separate two distinct classes. This separation is achieved by maximizing the margin between the hyperplane and the closest instance of each class, referred to as a support vector. The goal of the SVM learning method is to discover a linear function $f(x) = \beta x + b$, where $\beta \in R^p$ and $b \in R$, in order to classify a data point x as $+1\ if\ f(x) > 0$ and -1 otherwise. Introducing slack variables results in the development of the objective function, also referred to as the primal formula [48]:

$$\min(\frac{1}{2}||\beta||^2 + C\sum_{i=1}^{n} \xi_i) \tag{6}$$

with constraints:

$$(\beta x_i + b) \geq 1 - \xi_i, \quad \xi_i \geq 0 \tag{7}$$

In this case, the slack variable $\xi_i > 0$ represents the discrepancy between the ith instance and the necessary functional margin. The total of ξ_i can be considered an upper limit for empirical risk. Furthermore, the regularization constant $C > 0$ establishes the balance between $\frac{1}{2}||\beta||^2$ (the complexity component) and the sum of ξ_i.

The optimization problem with inequality constraints is altered using the Lagrange function, leading to a nonlinear regression function:

$$f(x) = \sum_{i=1}^{n} (\alpha_i - \alpha_i^*) \cdot G(x_i, x_j) + b \tag{8}$$

In this equation, $G(x_i,\ x_j)$ denotes the kernel function. The following kernel functions are frequently employed [49]:

(1) Linear kernel function:

$$G(x_i, x_j) = x_i^T x_j \tag{9}$$

(2) Polynomial kernel function:

$$G(x_i, x_j) = \left((x_i \cdot x_j) + 1\right)^q,\ q = \{2, 3, \ldots\} \tag{10}$$

(3) Gaussian kernel function:

$$G(x_i, x_j) = \exp\left(-||x_i - x_j||^2\right) \tag{11}$$

When dealing with data that are arranged in a linear manner, it is possible to divide them using a hyperplane, followed by the use of a linear kernel. In our research, we have utilized two types of nonlinear SVMs, which include the polynomial function and the radical basis function. The polynomial function is represented by the quadratic and cubic SVM, while the fine, medium, and coarse Gaussian SVMs represent the radical basis function [46].

- **Deep Neural Network (NN):**

Neural networks have been regarded as one of the most promising techniques in nonparametric statistics for several years, especially in multivariate statistical applications, such as pattern recognition and nonparametric regression. Recently, there have been several studies with a focus on deep learning, a branch of neural networks, where multilayer feedforward neural networks containing numerous hidden layers are employed for data examination (e.g., [50]). The success of deep learning has motivated researchers to investigate its theoretical properties, which has led to an increasing interest in the literature [51,52].

In our investigation, we concentrate on the fully connected layer, the most prevalent layer in neural networks, which performs a linear transformation of high-dimensional input signals into high-dimensional output signals using a dense matrix. When using neural networks to generate regression estimates, the initial step involves establishing an appropriate function space with a suitable activation function. The ReLU activation function is frequently utilized due to its effectiveness in nonlinear transformations [53]:

$$\sigma(x) = \max\{x, 0\} \tag{12}$$

The network structure, identified as (L, k), specifies the number of hidden layers and the neuron count in each layer, respectively. A typical network configuration might be expressed by [53]:

$$f(x) = \sum_{i=1}^{k_L} c_{1,i}^{(L)} f_j^{(L)}(x) + c_{1,0}^{(L)} \tag{13}$$

where $F(L,r)$ defines the neural network space with LL concealed layers and rr neurons in each layer, assuming fully connected feedforward architecture without any sparsity constraints [54]. The visual representation of this network as a directed acyclic graph is depicted in Figure 22.

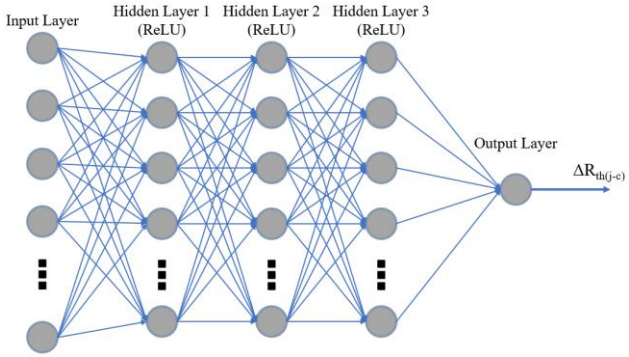


Figure 22. An illustration of a deep neural network architecture featuring up to three hidden layers.

To optimize the neural network's performance, particularly in minimizing the mean squared error (MSE), Bayesian optimization is employed. This method uses a guided search based on historical data to fine-tune hyperparameters such as the number of layers, size of the layers, and regularization strength, aiming to achieve the best possible model outcomes. This optimization method is indicated in [55].

In our specific study, we focus on optimizing the neural network through up to 60 iterations of hyperparameter adjustments. Additionally, we explore the impact of the number of neurons on performance by incorporating three neural network regressions with varying neuron counts, named narrow, medium, and wide, containing 10, 25, and 100 neurons, respectively. These modifications allow us to analyze the effects of the network structure on the thermal prediction performance of the models.

- **Gaussian Process Regression (GPR):**

Utilizing a nonparametric and probabilistic methodology, Gaussian process regression (GPR) serves as an effective instrument for performing regression analyses. GPR adeptly models intricate and nonlinear associations between input and output variables, offering both adaptability and comprehensibility. The foundation of GPR lies in representing the core function as a Gaussian process, which takes the form of a function distribution [56]. A Gaussian process is entirely defined by its mean and covariance functions, serving as a natural extension of the Gaussian distribution [57]. Here, the mean and covariance manifest as a vector and matrix, respectively. GPR models are grounded in the belief that prior observations furnish valuable insights about one another.

As a result, Gaussian process regression models can discern the predictive distribution associated with test input by leveraging the prior knowledge of functional dependency and data [58]. The nonlinear GPR models necessitate less training data and can incorporate new evidence as more data emerge. Additionally, these models usually possess a limited number of hyperparameters requiring optimization during training, reducing their susceptibility to overfitting [59].

In general terms, the GPR model is formulated by denoting the input and target variables as x and y, respectively. The initial phase in GPR modeling involves employing the subsequent general equation:

$$y_{L_i} = f\left(x_{L_i}\right) + \varepsilon_{L_i} \qquad i = 1, 2, \ldots, n \tag{14}$$

where $\varepsilon \sim N\left(0,\ \sigma_{noise}^2 I_n\right)$ represents the observation noise. The GPR model perceives f as a stochastic function, which can be characterized by its covariance and mean functions. This can be expressed as:

$$f\left(x_{L_i}\right) = GP\left(m(x),\ k\left(x, x'\right)\right) \tag{15}$$

The mean function $m(x)$ is often simplified to zero in practical computations.

The Gaussian conditioning rule helps to calculate the distribution of y_T given y_L, using kernel functions to define the covariance between inputs. This includes exponential, squared exponential, Matern, and rational quadratic functions, which are represented in the following form [57,60]:

Exponential GPR (GPR Exp):

$$k\left(x_i, x_j|\theta\right) = {\sigma_f}^2 \exp\left[-\frac{r}{\sigma_l}\right] \tag{16}$$

"r" represents the length of a line segment between the two points "x_i" and "x_j" in Euclidean space:

$$r = \sqrt{\left(x_i - x_j\right)^T \left(x_i - x_j\right)} \tag{17}$$

Squared exponential GPR (GPR SQ-Exp):

$$k(x_i, x_j|\theta) = {\sigma_f}^2 \exp\left[-\frac{1}{2}\frac{r^2}{{\sigma_l}^2}\right] \tag{18}$$

Matern 5/2 GPR (GPR Mat):

$$k(x_i, x_j|\theta) = {\sigma_f}^2 \left(1 + \frac{\sqrt{5}r}{\sigma_l} + \frac{5r^2}{3{\sigma_l}^2}\right) \exp\left[-\frac{\sqrt{5}r}{\sigma_l}\right] \tag{19}$$

Rational quadratic GPR (GPR RQ):

$$k(x_i, x_j|\theta) = {\sigma_f}^2 \left(1 + \frac{r^2}{2\alpha{\sigma_l}^2}\right)^{-\alpha} \tag{20}$$

The Gaussian-scale mixture parameter, denoted by α, is always a positive value.

This study opted for the Matern 5/2 kernel over the Matern 3/2 kernel due to its proven better performance in past studies [61,62]. All the GPR models, encompassing squared exponential, exponential, Matern 5/2, and rational quadratic kernels, showed superior results compared to multiple linear regression models [63].

4.1. Using Void Size/Position/Orientation as the Input to Different Regression Models

In the first step of generating synthetic X-ray images with solder voids, random voids are introduced with the following characteristics:

1. Random X-Y positions: The voids are placed at random positions within the image, ensuring a diverse set of spatial arrangements representative of real-world scenarios.
2. Random sizes (a and b): The dimensions of the ellipse-shaped voids, represented by the major axis (a) and minor axis (b), are randomly assigned within a specified range to create voids of varying sizes.
3. Random rotation angle (0–180): The voids are rotated by a random angle between 0 and 180 degrees to introduce additional variability in the orientation of the voids, mimicking the different orientations that may be encountered in actual IGBTs.

By incorporating these random factors, a diverse and representative dataset of synthetic solder voids can be generated, simulating various solder void patterns that may be found in real-world IGBTs. This study involves the application of 12 different regression models to predict thermal resistance in a case with 10 randomly generated solder voids. Here, a total of 1000 void patterns have been generated, encompassing cases with 1 void up to 10 voids randomly distributed within the solder layer. Thus, we can describe an FEM simulation where 10 randomly generated ellipse-shaped voids are added to a solder layer 1000 times to create a dataset. The process then involves removing the voids one by one to obtain a dataset for the number of voids ranging from 1 to 10. It means, for instance, the position, size, and rotation of the first void remain fixed in each of the ten cases.

In the first regression modeling scenario, a separate regression block is selected for each number of voids present in the solder layer, as shown in Figure 23. This means that for up to 10 voids, 10 different regression models are required. The appropriate regression block is then selected based on the number of voids present in the solder layer. This approach allows for the development of customized regression models that can account for the specific number of voids present in the solder layer. By using separate regression models for each number of voids, the accuracy and effectiveness of the modeling process can be improved. As mentioned before, a circle packing method is used to randomly generate non-overlapping ellipse-shaped voids in the solder layer. In this scenario, 80% of the input data are randomly selected to be used as the training data, while the remaining 20% are used as the testing/validation data. This is a common split ratio used in many applications. The reason behind this split is explained in [64], based on empirical evidence. The dataset for the experiment includes 10 voids, and for each void, there are five characteristics,

which include the position (x,y), size (a,b), and rotation (rot). The last row in the dataset is dedicated to thermal resistance junction-to-case ($R_{th(j-c)}$). Therefore, considering the total number of voids as 10, the size of the input data becomes 1000 × 151.

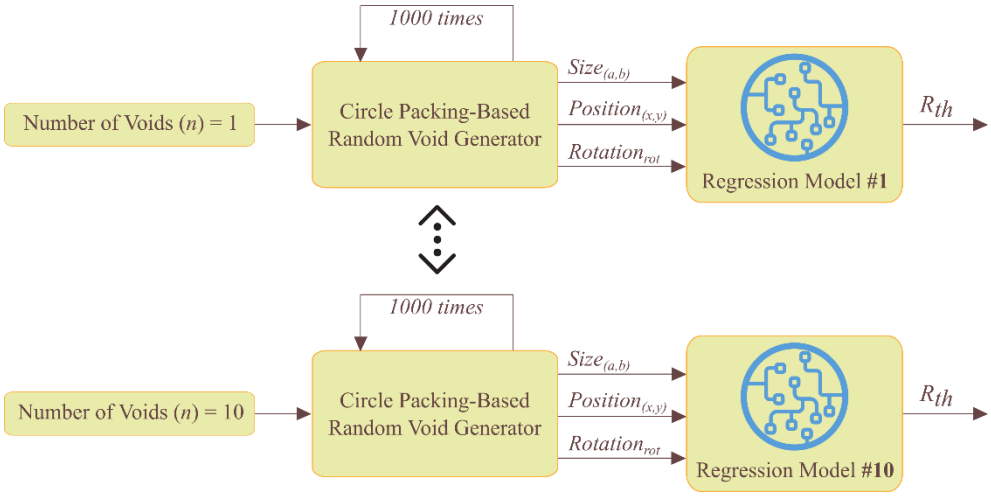


Figure 23. Proposed method for estimating thermal resistance using separate regression blocks for each number of voids.

The regression performance for both training and testing in the case with one single void is shown in Figure 24. As can be seen, the linear models (linear regression and SVM-Linear) applied in this study also could not provide a good prediction for the thermal resistance. The SVM models, in general, could not provide a good fit on the data. This finding suggests that linear models may not be appropriate choices for predicting thermal resistance in cases also with multiple voids. The findings also indicate that the accuracy of the regression models varies greatly depending on the number of neurons in the neural network. In this case, the higher number of neurons in the first layer does not necessarily lead to a better prediction.

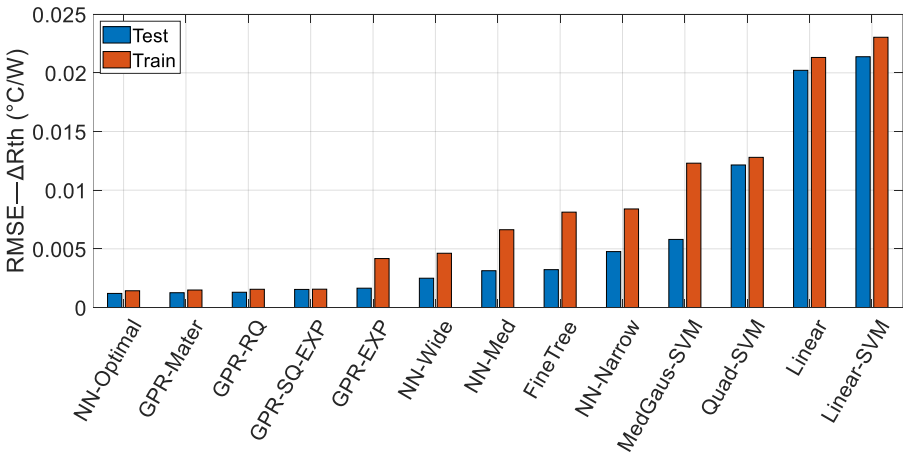


Figure 24. Comparison of RMSE values for predicted thermal resistance test data with a single void in solder layer using different regression models.

The optimal neural network is also obtained by hyperparameter optimization (Figure 25). In this case, the optimal number of hidden layers is one with 106 neurons. However, the optimal regularization strength (λ) is not equal to zero, which has a significant effect on the accuracy of the neural network model (for the narrow, medium, and wide neural networks, the parameter λ is zero). Regularizers have been identified as

necessary for the fine-tuning of neural networks, as stated in [65]. They play a critical role in improving the prediction performance of the models and can lead to significant improvements in their accuracy. A regularization strength of $\leq$0.01 has been found to be more beneficial for the learning process of neural networks [66]. Here, the optimal value of λ is 6.4054×10^{-5}. Although the optimal neural network could provide accurate predictions (testing RMSE = 0.00515 and R^2 = 0.964), the GPR regression models, in particular, seem to be the most appropriate option for predicting thermal resistance, as they consistently provide accurate predictions. In this case (no. voids = 1), the GPR Matern has the best prediction performance with the RMSE = 0.0050 and R^2 = 0.9728. Figure 26 displays the QQ-plot of the testing/training performance for GPR Matern and the optimal neural network. Despite the weak training performance of the neural network, the testing performance is found to be acceptable.

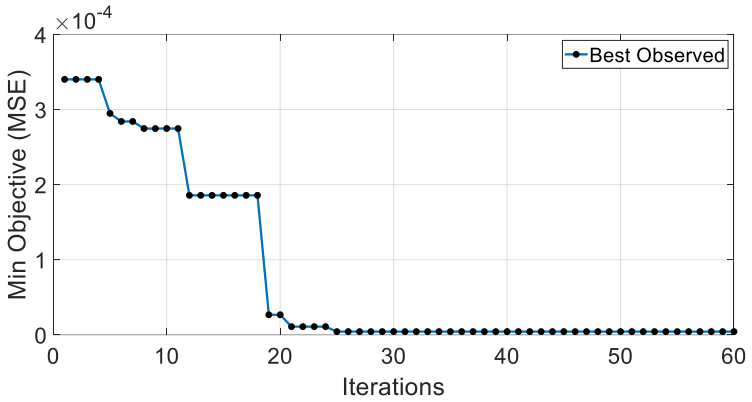


Figure 25. The minimum objective function achieved by optimizing the hyperparameters of the optimal neural network.

We extend our analysis to include 10 voids in the solder layer, using regression models to predict the thermal resistance. Figure 27 depicts the RMSE values obtained for the estimated thermal resistance in the case of 10 large voids in the solder layer using various regression models. Surprisingly, linear models show better performance in comparison to the previous cases with fewer voids. Similarly, the tree and SVM regression models also demonstrate improved performance at a higher number of voids. The GPR models maintain their position at the top of the performance list, indicating their effectiveness in predicting thermal resistance. Based on our analysis, the GPR RQ model is found to be the best regression model in this case, and it outperforms the other regression models in predicting thermal resistance. Meanwhile, Figure 28 shows the predicted response versus the actual response for the GPR RQ model, as well as the error percentage over the test data using the same model. The results indicate that, with a few exceptional outliers, the GPR RQ model exhibits near-perfect accuracy in predicting thermal resistance.

The optimal neural network, in this case, performs similarly to the narrow neural network with a low layer size. This result suggests that the optimal neural network architecture for 10 voids might not require a large number of nodes in the hidden layers and that simpler models could be sufficient for effective prediction.

To investigate the performance of the GPR regression models on the prediction results with varying numbers of voids (ranging from 1 to 10), we apply these models to different cases. Figure 29 depicts the prediction error obtained from four GPR kernel models for thermal resistance prediction, presented in relation to the number of voids. In cases where multiple voids are present, the RMSE remains almost constant around 0.006 °C/W.

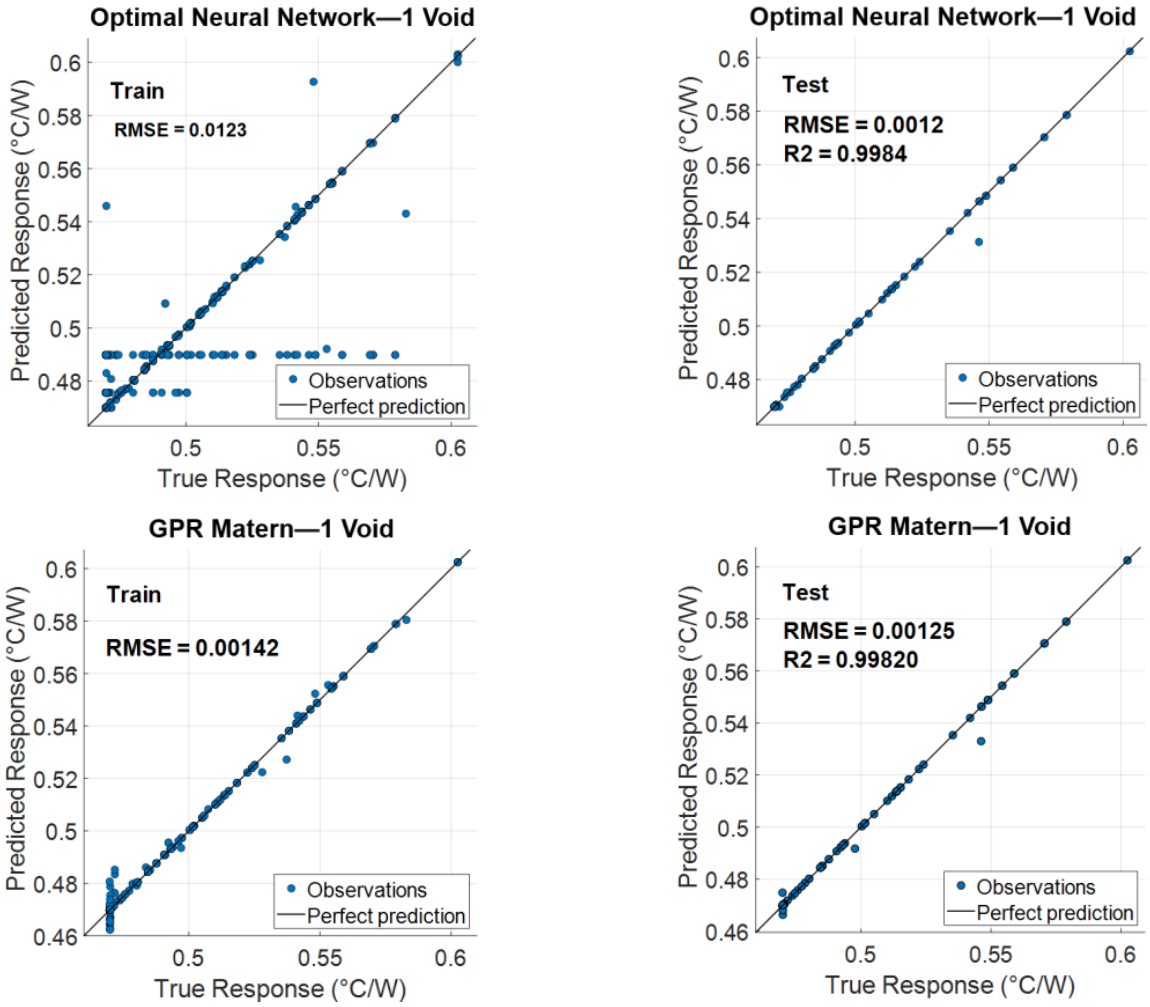


Figure 26. A comparison of the real versus predicted values for the optimal neural network and GPR Matern models, depicted in scatter plots over the training and testing datasets. The black inclined line denotes the ideal prediction.

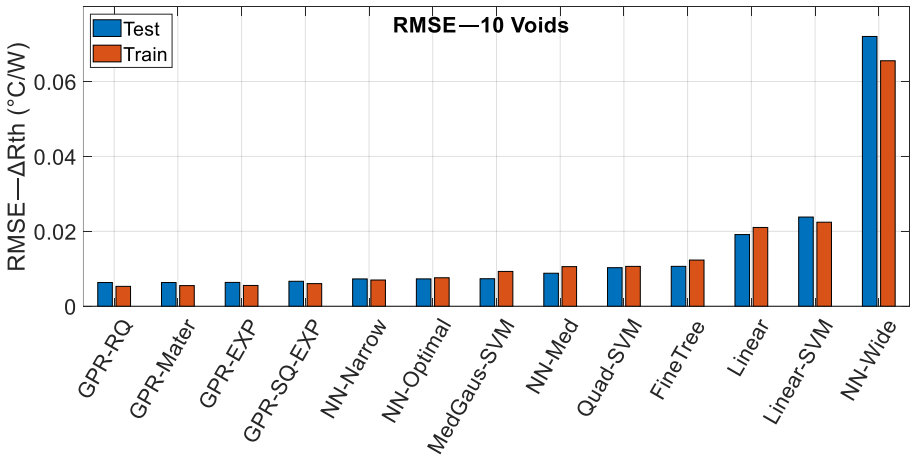
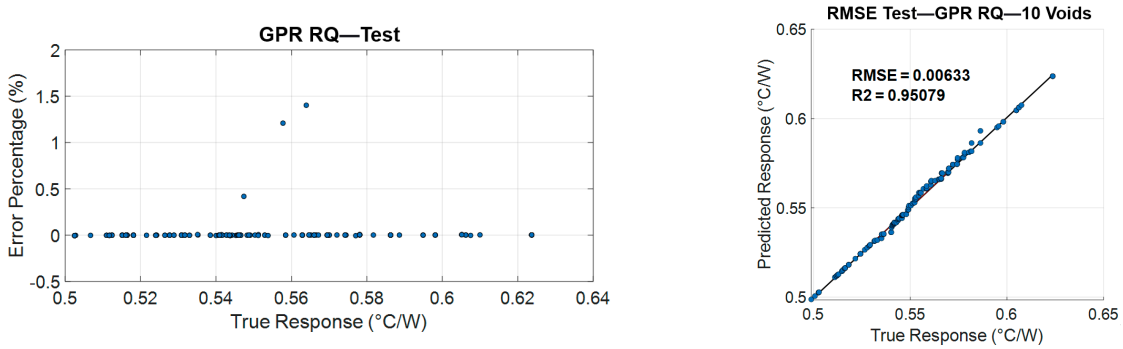
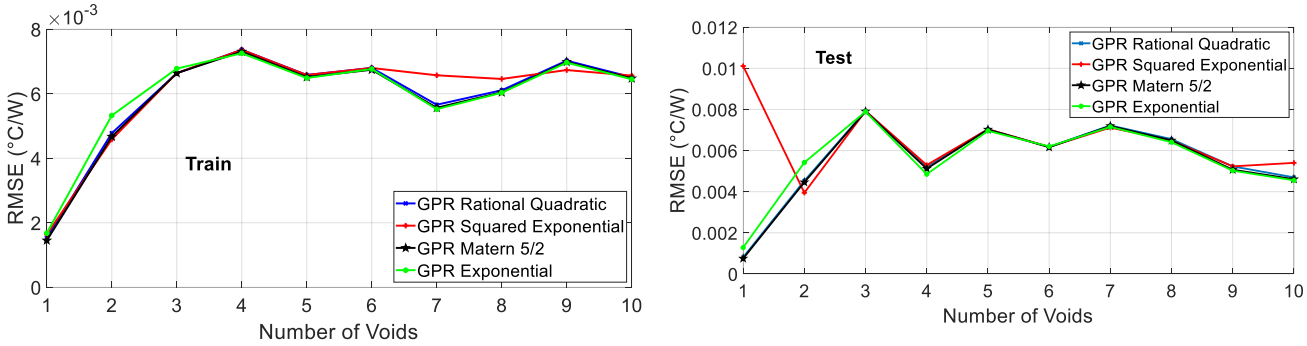


Figure 27. Comparison of RMSE values for predicted thermal resistance test data with 10 large voids in solder layer using different regression models.



(**a**) (**b**)

Figure 28. Error percentage of GPR RQ regression model (**a**), and its relative QQplot against true response (**b**).



(**a**) (**b**)

Figure 29. RMSE comparison of four GPR kernel models for thermal resistance prediction in terms of the number of voids (Train data: (**a**), test data: (**b**)).

Interestingly, the GPR SQ-Exp model shows poor results compared to the other three GPR models in the case of a single void. However, in the multiple voids scenario (as shown in Figure 29), the GPR SQ-Exp model demonstrates similar results to the other three GPR models. The columns from the input dataset are randomly picked by a random function in MATLAB while keeping the ratio of 80–20% constant for each iteration. An example is shown in Figure 30. This finding suggests that the random selection of 80–20% for training and testing datasets can have an impact on the regression model's performance. To address this, we repeat the random selection process 50 times and plot the box plot of the RMSE for the four GPR regression models, as shown in Figure 31.

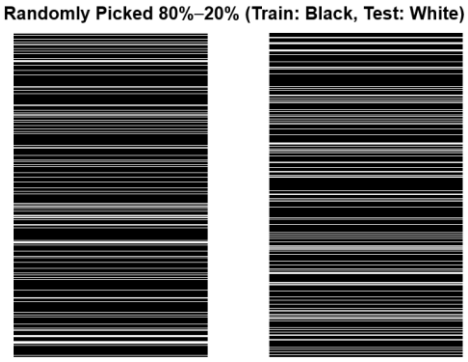
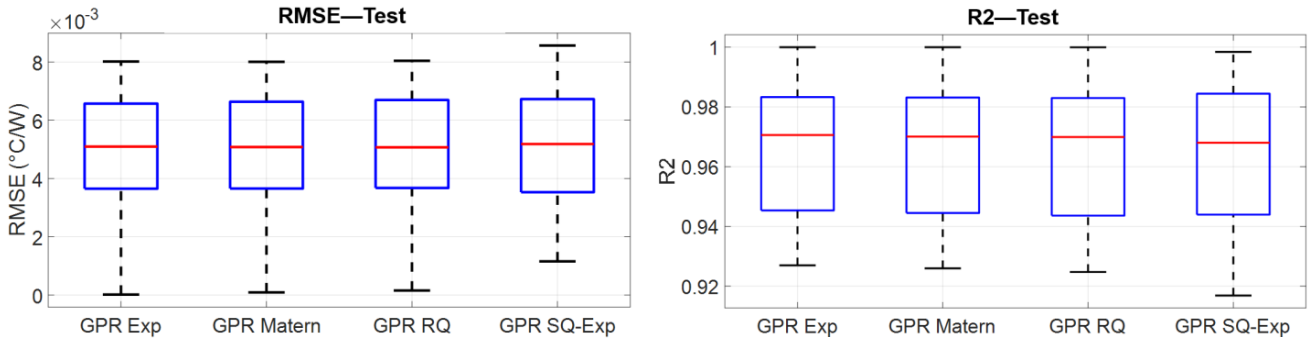


Figure 30. An illustration of the 80–20% random sampling technique on the input dataset.



(**a**) (**b**)

Figure 31. Model goodness-of-fit comparison for four GPR kernels and sensitivity analysis to the order of input data (RMSE: (**a**), and R^2: (**b**)).

The box plots reveal that the GPR SQ-Exp has the worst prediction performance among the GPR models considered. However, this slightly higher error does not necessarily imply that this kernel is unsuitable for regression modeling of thermal resistance estimation. On the contrary, it remains one of the best choices for this task, as demonstrated by its performance relative to the other GPR models. Therefore, it is important to consider the specific requirements of each scenario and carefully evaluate the trade-offs between model complexity, prediction accuracy, and computational resources when selecting an appropriate kernel for GPR regression modeling.

4.2. Utilizing Void Characteristics for Regression Models through Zero-Padding Method

Zero-padding is a technique used to fill up matrix arrays with zero values. In this method, additional zeros are added to the beginning or end of an existing array to achieve a specific size or shape. This technique is commonly used in signal processing, image processing, and data analysis applications [67]. In data analysis, zero-padding is often used to ensure that datasets are the same size or shape. Zero-padding can be used to add zeros to the shorter column so that the two columns have the same length, enabling comparison and analysis.

In the case of 10 voids, the input dataset contains 150 elements, whereas for the case of a single void, there are only 5 elements. In order to ensure that each column of the input dataset has the same number of elements, a zero-padding method is used to fill up the blank columns with zeros. For instance, when there is only one void, the remaining 145 elements are padded with zeros at the end of the column to make the total number of elements 150. This approach ensures that the input dataset is consistent. By using the zero-padding method to ensure that each column of the input dataset has the same number of elements, we can train a single regression model block that can be used for all cases, regardless of the number of voids. This approach is advantageous as it eliminates the need to train several regression models on a large dataset with varying numbers of voids, simplifying the modeling process and reducing the computational complexity. Figure 32 shows the proposed approach based on the zero-padding method.

Figure 33 shows the results for ellipse-shaped voids with a zero-padding method. To ensure the consistency and accuracy of our regression models, we repeat the training process 10 times with randomly picked 20% test data and 80% train data. We apply the randomly picked data to the different regression models while taking into account the zero-padding method to ensure that each column of the input dataset had the same number of elements. This approach allows us to validate the performance of the regression models across multiple iterations, providing a more robust assessment of the accuracy and effectiveness of the models.

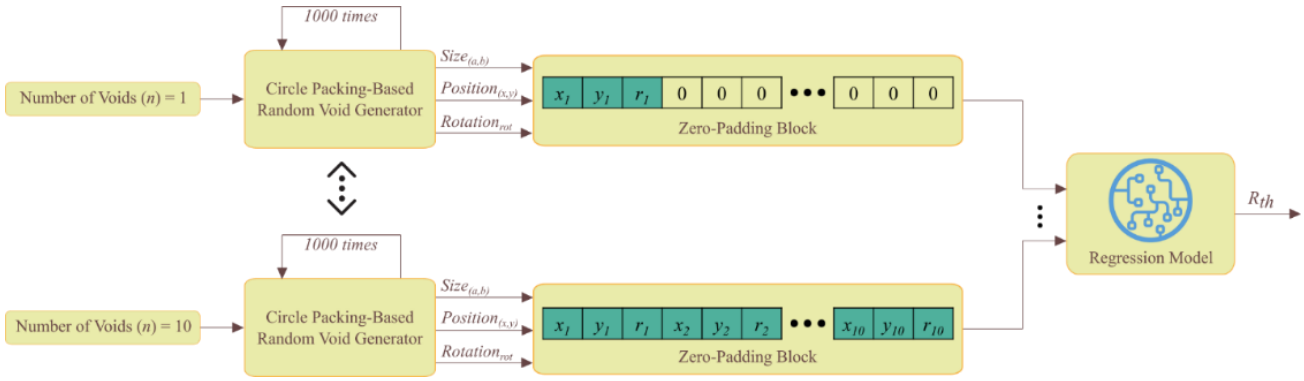
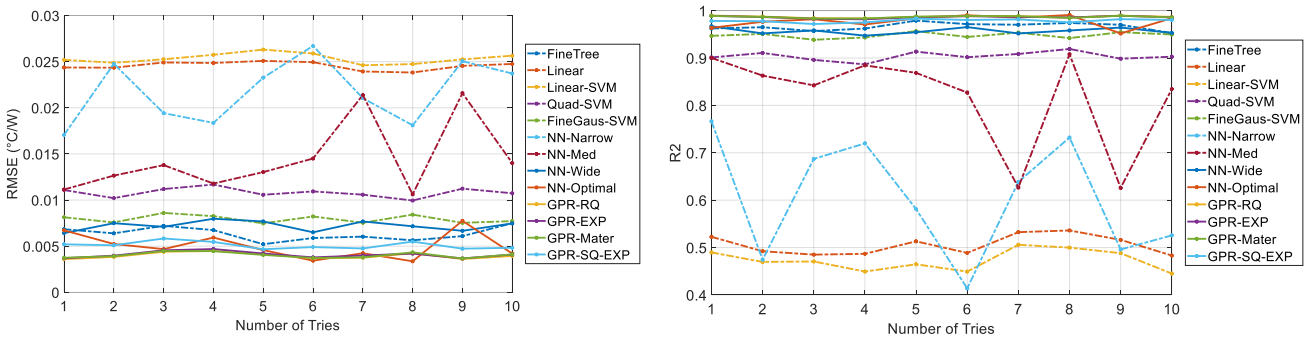


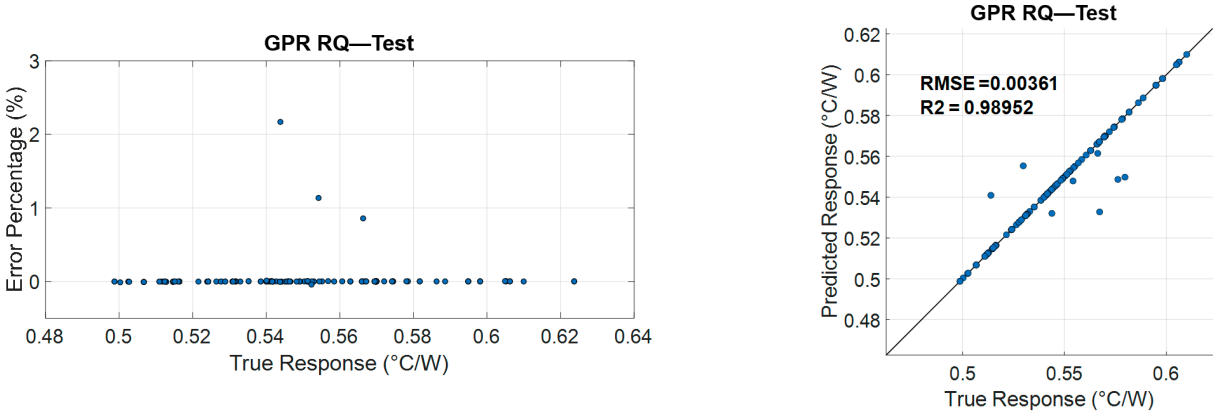
Figure 32. Proposed method for estimating thermal resistance using zero-padding method and one unit regression block for all numbers of voids.



(**a**) (**b**)

Figure 33. Comparison of RMSE (**a**) and R^2 (**b**) values for regression models with zero-padding method applied to multiple ellipse-shaped voids (up to 10 voids).

The error percentage between the predicted thermal resistance values and actual values obtained from the FEM simulations for the best-performing regression model, GPR RQ, is presented in Figure 34. The error percentage plot in Figure 34 indicates that, except for a few outliers with an error percentage of around 1 or 2%, most of the data points have almost a zero-percent difference with the true response. This suggests that the GPR RQ regression model has an impressive accuracy for estimating the thermal resistance and can ideally predict these values.



(**a**) (**b**)

Figure 34. Error percentage of GPR RQ regression model (**a**) and its relative QQplot against true response (**b**) (up to 10 voids with the zero-padding method).

Our analysis shows that a single regression model can be used for all numbers of voids, simplifying the modeling process. The results indicate that non-optimized neural networks, particularly narrow and medium neural networks, are highly dependent on the input data, whereas the other regression models show more consistent performance across different input data. Linear regression and linear SVM regression do not perform well in general, while tree regression provides better predictions than the wide neural network. The selected SVM regressions are not optimal choices compared to the GPR and optimal neural network regressions. The GPR regressions alongside the optimal neural network demonstrate the best performance overall and are the recommended choice for this case. However, among the GPR kernels, the GPR SQ-Exp kernel has the worst performance.

Our findings suggest that the use of the zero-padding method and a single unified regression block can potentially reduce the accuracy of the prediction, as expected. However, in the case of GPR models and optimal neural networks, the decrease in accuracy is negligible, and the models are still able to provide highly accurate results. This indicates that the use of a single regression model and zero-padding method can be a viable approach for simplifying the modeling process without sacrificing the accuracy of the predictions, particularly when GPR models are used.

4.3. Using Void Characteristics for Regression Models: Scaling up to 50 Voids

In our next step, we increase the number of voids up to 50 to better capture the effect of smaller voids on the thermal resistance junction-to-case. However, to avoid increasing the number of inputs to the regression model significantly, we model circle-shaped voids instead of ellipse-shaped voids. Although this simplification may introduce some errors in the simulations, our previous analysis showed that there is little difference between the predictions of circle-shaped and ellipse-shaped voids when the number of voids is high. Therefore, we expect the use of circle-shaped voids to have minimal impact on the accuracy of our predictions. The total number of data points in this analysis is 3000. Similar to the previous case, we conduct 10 simulations with randomly generated voids in the solder layer, and for each case, we apply the different regression models that were used in our previous analysis. This approach allows us to evaluate the performance of the regression models across multiple scenarios and provide a more robust assessment of their effectiveness in predicting the thermal resistance junction-to-case based on the void percentage. Figure 35 displays the RMSE values calculated for the testing data using different regression models across the 10 simulations with randomly generated voids in the solder layer.

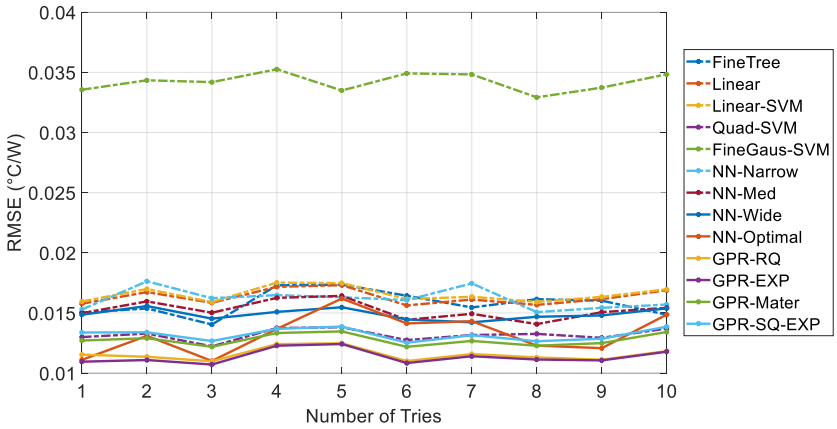


Figure 35. The RMSE values for the testing data across 10 simulations with randomly generated voids in the solder layer using different regression models.

The results shown in Figure 35 highlight the limitations of the Fine-Gaussian SVM in modeling this regression problem, as it produces worse results than even the linear regression model. Similarly, other SVM models also fail to provide accurate predictions,

except for the quadratic SVM, which outperforms the tree regression and single-layer neural networks in this particular case. The GPR RQ and GPR-Exp models are found to be the best prediction methods for this scenario. However, the optimal neural network model shows a high degree of variability in performance, and at certain points, it performs worse than the GPR kernels. Overall, the GPR Matern model performs slightly better than the GPR SQ-Exp model and ranks third among the best regression models in this analysis.

4.4. Using Void Area Percentage as Input to the Regression Models

Our next step in simplifying the prediction framework is to estimate the thermal resistance junction-to-case solely based on the solder void percentage. This means that the input to the regression model is only the void percentage, and the output is the thermal resistance. The proposed thermal resistance prediction framework is depicted in Figure 36. To calculate the void percentage, we can determine the total area of the circle-shaped voids and divide it by the total area of the solder layer under the IGBT chip, which is 4×4 mm. To calculate the void percentage for the regression model, we will use the same dataset as in the previous case with random voids, where up to 50 voids were randomly generated. Thus, we will have a total of 3000 data points in the input dataset, each consisting of the void characteristics and the corresponding thermal resistance junction-to-case. We then calculate the solder void area percentage for the 3000 given void patterns and apply various regression models to the problem. To ensure robustness in our estimated error, we repeat the simulation process 10 times, randomly selecting 80–20% of the input data for training and testing purposes.

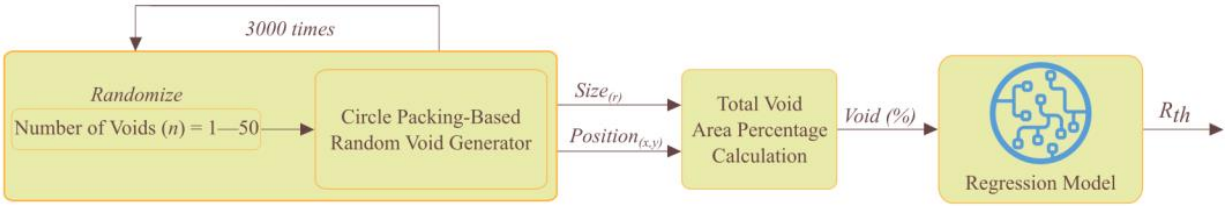
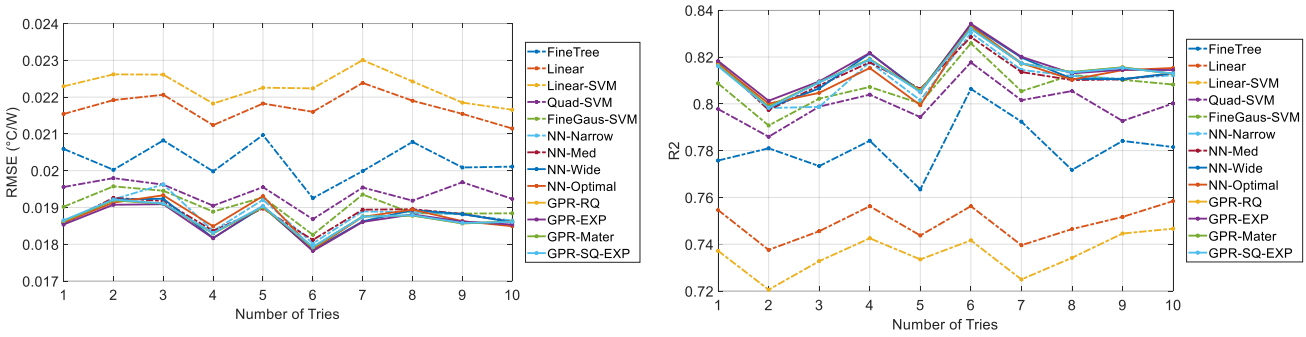


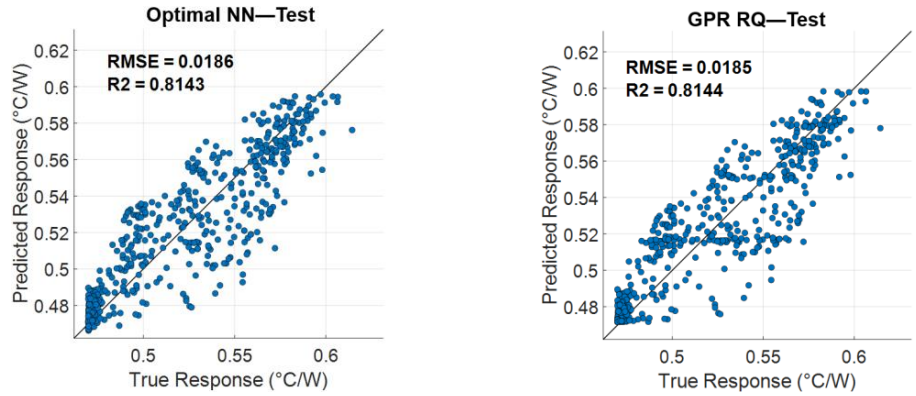
Figure 36. The proposed method for estimating thermal resistance using the void area percentage as input and a single unit regression block.

The results obtained from the regression models using the void percentage as input are displayed in Figure 37, which shows the RMSE and R^2 estimates. It can be observed that the linear regression models perform poorly in predicting thermal resistance. The tree regression model also could not provide accurate predictions in this scenario. Surprisingly, all the regression models show a significant increase in the prediction error when the void percentage is used as the input parameter. Also, the SVM-based regression models could not achieve acceptable accuracy. Interestingly, the remaining regression models, including the one-layer neural networks (ranging from narrow to wide), optimal neural network, and GPR models, all provide the same level of accuracy in predicting thermal resistance. The sensitivity of the neural network on the layer size is comparatively lower in this case. This low accuracy in prediction suggests that using only the void percentage as input may not be the best option compared to using more detailed void characteristics as input to the regression models. Figure 38 presents a scatter plot that compares the predicted and actual values, utilizing both the optimal neural network and GPR RQ regression (as the best-performing regression model). The results imply that the characteristics of individual voids and their locations within the solder layer are crucial factors affecting thermal resistance. Therefore, it is necessary to consider such characteristics in order to achieve a more accurate prediction of thermal resistance.



(**a**) (**b**)

Figure 37. Comparing RMSE (**a**) and R^2 (**b**) values of regression models using void area % as input (up to 50 circle-shaped voids).



(**a**) (**b**)

Figure 38. A scatter plot of the predicted and actual values using an optimal neural network (**a**) and GPR RQ regression (**b**).

5. Conclusions

In conclusion, this study thoroughly examined the role of solder voids in influencing the thermal behavior of IGBT devices, utilizing experimental measurements, advanced image processing techniques, and Finite Element Method (FEM) simulations. The results demonstrated that void characteristics—particularly the size, position, and quantity—significantly impact thermal resistance, highlighting the critical need for minimizing these voids to enhance device reliability and performance.

This study showed that the optimal neural network model achieved an impressive testing RMSE of 0.00515 and an R^2 of 0.964, validating the model's accuracy in predicting thermal resistance. The regression analyses revealed that Gaussian process regression (GPR) models exhibit exceptional predictive accuracy, with the GPR RQ model standing out for its robust performance across various scenarios, achieving an RMSE of 0.0050 and an R^2 of 0.9728 in cases with single and multiple voids. The precision of this model in complex scenarios reflected its ability to handle the nonlinear relationships between thermal resistance and void characteristics. In more detailed experiments involving up to 50 voids, the GPR models still provided high accuracy, with the GPR Matern model showing great performance across different void configurations. Specifically, the GPR Matern model showed superior adaptability, managing an RMSE as low as 0.006 °C/W in multi-void scenarios.

Additionally, the simulations revealed that even minor changes in the void characteristics—such as a shift from single to multiple voids—can significantly impact the thermal resistance. For instance, adding a second large void could lead to an increase in thermal resistance by approximately 20%, underscoring the critical influence of void

distribution within the solder layer. It was also found that small voids (less than 50 µm) have negligible effects on thermal resistance, highlighting the greater significance of larger voids in thermal behavior.

Furthermore, this study highlighted the limitations of relying only on the void percentage as a predictor, which significantly increased the prediction errors across all the models. This shows the importance of adding detailed void characteristics in the models to obtain precise predictions of thermal resistance. Applying zero-padding in regression models to the datasets containing different numbers of voids could give us high levels of predictive accuracy, showing the applicability of this approach to simplify the regression modeling.

This detailed study significantly enhances our knowledge of how void characteristics influence the thermal resistance of IGBT devices and refines the methods used for predicting their reliability and operational efficiency. Future research should consider incorporating these predictive models into actual monitoring systems, which could improve early failure detection and extend the lifespan of IGBTs. Additionally, the exploration of alternative solder materials and novel manufacturing techniques may offer effective strategies to decrease the occurrence of voids, thereby improving thermal management and overall performance of IGBT modules.

Author Contributions: Conceptualization, O.A., W.D.C. and M.D.; methodology, O.A.; software, O.A.; validation, O.A. and M.D.; formal analysis, O.A.; investigation, O.A.; resources, W.D.C. and M.D.; data curation, O.A.; writing—original draft preparation, O.A.; writing—review and editing, W.D.C. and M.D.; visualization, O.A.; supervision, W.D.C. and M.D.; project administration, M.D.; funding acquisition, M.D. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data supporting this study are included within the article.

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Conflicts of Interest: The authors declare no conflicts of interest.

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