Solving the Annealing of Mo Interconnects for Next-Gen Integrated Circuits

Ivan Erofeev, Antony Winata Hartanto, Khakimjon Saidov, Zainul Aabdin, Antoine Pacco, Harold Philipsen, Weng Weei Tjiu, Hui Kim Hui, Frank Holsteyns, and Utkur Mirsaidov*

Recent surge in demand for computational power combined with strict constraints on energy consumption requires persistent increase in the density of transistors and memory cells in integrated circuits. Metal interconnects in their current form struggle to follow the size downscaling due to materials limitations at the nanoscale, causing severe performance losses. Next-generation interconnects need new materials, and molybdenum (Mo) is considered the best choice, offering low resistivity, good scalability, and barrierless integration at a low cost. However, it requires annealing at temperatures far exceeding the currently accepted limit. In this work, the challenges of high-temperature annealing of patterned Mo nanowires are looked into, and a new approach is presented to overcome them. It is demonstrated that while a conventional annealing process improves the average grain size, it can also reduce the cross-section area, thus increasing the resistivity. Using high-resolution transmission electron microscopy (TEM) with in situ heating, the evolution of structural features in real time is directly observed. Using insights from these experiments, a cyclic pulsed annealing method is developed, and it is shown that the desired grain structure is achieved in only a few seconds, without forming the surface grooves. These findings can radically facilitate Mo integration, boosting the efficiency of future integrated circuits.

1. Introduction

Moore's law of device scaling has been guiding semiconductor technology development toward higher computational power and lower energy consumption for the past 60 years.[1] This required a steady reduction in the size and increase in the density of all elements in integrated circuits (ICs).[2–4] While the recent advances with new gate-all-around designs ensure further downscaling of transistors for at least a few generations,[5] metal interconnects that link individual transistors have become the real bottleneck. Similarly, the ever-growing size of NAND flash memory stacks sets a higher plank for the performance of metal interconnects than what current technology can reach. At the scale of tens of nanometers, where the metal width d and the average grain size D become comparable to the electron mean free path λ, the electron scattering off the surface and reflections at the grain boundaries (GBs) substantially increase the effective metal resistivity. The surface and GB contributions follow the Fuchs-Sondheimer (FS) and Mayadas-Shatzkes (MS) scalings, respectively[6,7]: $\rho_S \sim \rho_0 \frac{\lambda}{d}(1-p)$ and $\rho_{GB} \sim \rho_0 \frac{\lambda}{D}(\frac{R}{1-R})$. Here, ρ_0 is the bulk resistivity, p is the surface specularity (i.e., the fraction of electrons keeping their parallel momentum upon reflection from the metal surface), and R is the probability of an electron reflection from a GB. It follows, that metals with short λ are less susceptible to these

I. Erofeev, A. W. Hartanto, K. Saidov, U. Mirsaidov
Centre for BioImaging Sciences
Department of Biological Sciences
National University of Singapore
Singapore 117557, Singapore
E-mail: mirsaidov@nus.edu.sg

I. Erofeev, A. W. Hartanto, K. Saidov, U. Mirsaidov
Centre for Advanced 2D Materials
National University of Singapore
Singapore 117546, Singapore

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.202400035

K. Saidov, U. Mirsaidov
Department of Physics
National University of Singapore
Singapore 117551, Singapore

Z. Aabdin, W. W. Tjiu, H. K. Hui
Institute of Materials Research and Engineering (IMRE)
Agency for Science
Technology and Research (A*STAR)
Singapore 138634, Singapore

A. Pacco, H. Philipsen, F. Holsteyns
imec
Kapeldreef 75, Leuven B-3001, Belgium

U. Mirsaidov
Department of Materials Science and Engineering
National University of Singapore
Singapore 117575, Singapore

effects and can perform better at the nanoscale, even if their ρ_0 is higher. Copper (Cu) has been used as an interconnect metal for decades due to its very low $\rho_0 = 1.68\,\mu\Omega\,cm$, but its relatively long $\lambda = 39.9\,nm$ makes the downscaling of Cu interconnects to $d < 20\,nm$ challenging.[8,9] Moreover, the need for a barrier layer to prevent Cu diffusion into the surrounding dielectric under electric and thermal load reduces the effective conductor width by another 3–4 nm on each side,[10–12] which leads to an even more drastic increase in the line resistance. Hence, an ideal metal for nanoscale wiring should feature a low $\rho_0\lambda$ value and not need a barrier layer for maximum conductive cross-section.[13,14] The most promising candidate that fits the above requirements is molybdenum (Mo). It has $\rho_0 = 5.34\,\mu\Omega\,cm$ and $\lambda = 11.2\,nm$,[15] does not diffuse into dielectrics,[16,17] and can be patterned using direct metal etch, a simpler and cheaper approach compared to the damascene process currently used for Cu.[18–21] In addition, it is much cheaper than its main competitor – similarly performing ruthenium (Ru) with $\rho_0 = 7.8\,\mu\Omega\,cm$ and $\lambda = 6.59\,nm$[14] (currently ≈65 USD/kg for Mo versus over 14 000 USD/kg for Ru [22]). The key integration challenge for Mo lies in its high melting temperature of 2623 °C,[23] which suggests that achieving coarse grain structure to reduce ρ_{GB} will require annealing at temperatures well beyond the currently accepted limit of ≈500 °C.[24] Although this limit can be potentially increased in the new backside power delivery architecture,[25,26] or by using unconventional annealing methods such as a laser beam,[27,28] annealing of Mo nanowires at temperatures this high has not been widely explored.

Interconnect wires have been previously studied on the examples of Al and Cu[8,9,29–31] at the scales relevant for the corresponding technology generations. These studies show that achieving a so-called bamboo grain structure, so that all GBs go across the wire axis and take the entire cross-section, is critical for the performance. More recent studies address the resistivity of cobalt,[32] ruthenium,[33] and tungsten[34] nanowires as a function of their width and the effect of annealing, but they do not provide any nanoscale details about the structure evolution or the resistivity dependence on the grain size. For Mo metallization, studies so far have mostly been focused on thin films[35,36] rather than nanowires because the films are easy to manufacture and have standard procedures to characterize their structure and electrical resistivity. However, because of the morphology difference, thin film results are not directly applicable to nanowires in integrated circuits. In quasi-2D polycrystalline films, the GB migration during annealing is largely unconstrained in two planar dimensions: if a GB motion stops in one direction, it can continue in the other. This is because GBs are arranged in a network, and each geometry variation generates a long-range equilibrium perturbation.[37] Of course, there is a pinning effect from surface grooves,[38,39] but it poses only a minor obstacle. In contrast, quasi-1D nanowires are limited by the surface in two dimensions, so GBs can only rearrange locally. Because of the energy minimization criterion, they tend to turn perpendicular to the wire axis, forming the bamboo structure. This makes GBs disconnected from each other on a larger scale, so once a local equilibrium is achieved, there is little drive for further migration. Provided that the initial average grain size in a nanowire is very small, the maximum grain size after annealing cannot be much bigger than the nanowire width. For this reason, polycrystalline films have larger grains when subjected to

similar annealing conditions. On the other hand, film annealing has to be done separately for each metal layer, while using post-patterning annealing enables processing the entire stack at once, potentially saving hours of fabrication time.

Hence, the major open questions regarding nanowires are: i) how does the crystal structure change during annealing?; ii) how much can the mean grain size be improved and how much will it reduce the resistivity; iii) what are the optimal annealing temperature and duration?

Here, we describe how the grain structure of patterned Mo nanowires evolves during different annealing scenarios. First, we show how conventional nanowire annealing affects the grain structure and resistivity over time and identify the key issue of this process: formation of GB grooves, which reduce the nanowire cross-section and thus increase the resistance, negating the positive annealing effect. Using high-resolution transmission electron microscopy (HRTEM) with in situ heating, we track the evolution of individual grains and structural features during the annealing at different temperatures at the atomic scale. We focus on the dynamic changes in surface diffusion and GB motion with the temperature increase and identify the respective time scales that govern the interplay between these processes. Based on these insights, we present the cyclic pulsed annealing approach, which allowed us to achieve the bamboo grain structure and high surface smoothness in just a few seconds while not forming any GB grooves.

2. Results and Discussion

The nanowires used in this work are patterned in large arrays from a Mo film, with each wire being 40 nm in height and 32 nm in width, as shown in the schematics in **Figure 1A**. A typical annealing profile with a dwell temperature of 800 °C is shown in Figure 1B, where four key states are marked with Roman numerals I-IV: before the annealing, after 0.5, 1, and 2 h. The corresponding top-view TEM images of the nanowires in Figure 1C show a steady increase in the grain size, as well as the formation of deep GB grooves at the later stage of annealing. The histograms in Figure 1D show grain size distribution for these four states obtained through automated grain recognition in TEM images. Without annealing, the distribution features a single peak at 13 nm and the average grain size is 13.6 nm, while the maximum is ≈34 nm. This is consistent with the previously reported scaling of average grain size with the film thickness.[36] After 30 min of annealing at 800 °C, a second peak in the grain size distribution appears ≈23 nm size, increasing the average grain size to 18.3 nm. After 1 h of annealing, the number of small grains below 15 nm is significantly reduced, and the average grain size increases to 23.8 nm, while the maximum grain size remains below 40 nm. After 2 h of annealing, the size distribution is nearly normal, with a mean value of 31.2 nm. There are only a few grains below 15 nm in size, and the maximum size increased beyond 50 nm. Finally, the measured resistivities of nanowires are compared in Figure 1E: the resistivity gradually reduces from the initial 20.6 to 15.9 $\mu\Omega\,cm$, that is, by 22%, during the first hour but then increases to 28.3 $\mu\Omega\,cm$ during the second hour of annealing. The first three data points fit well to the FS-MS theoretical scaling[6,7] with specularity $p = 0$ and GB reflection coefficient $R = 0.65$, but the final point deviates from this scaling
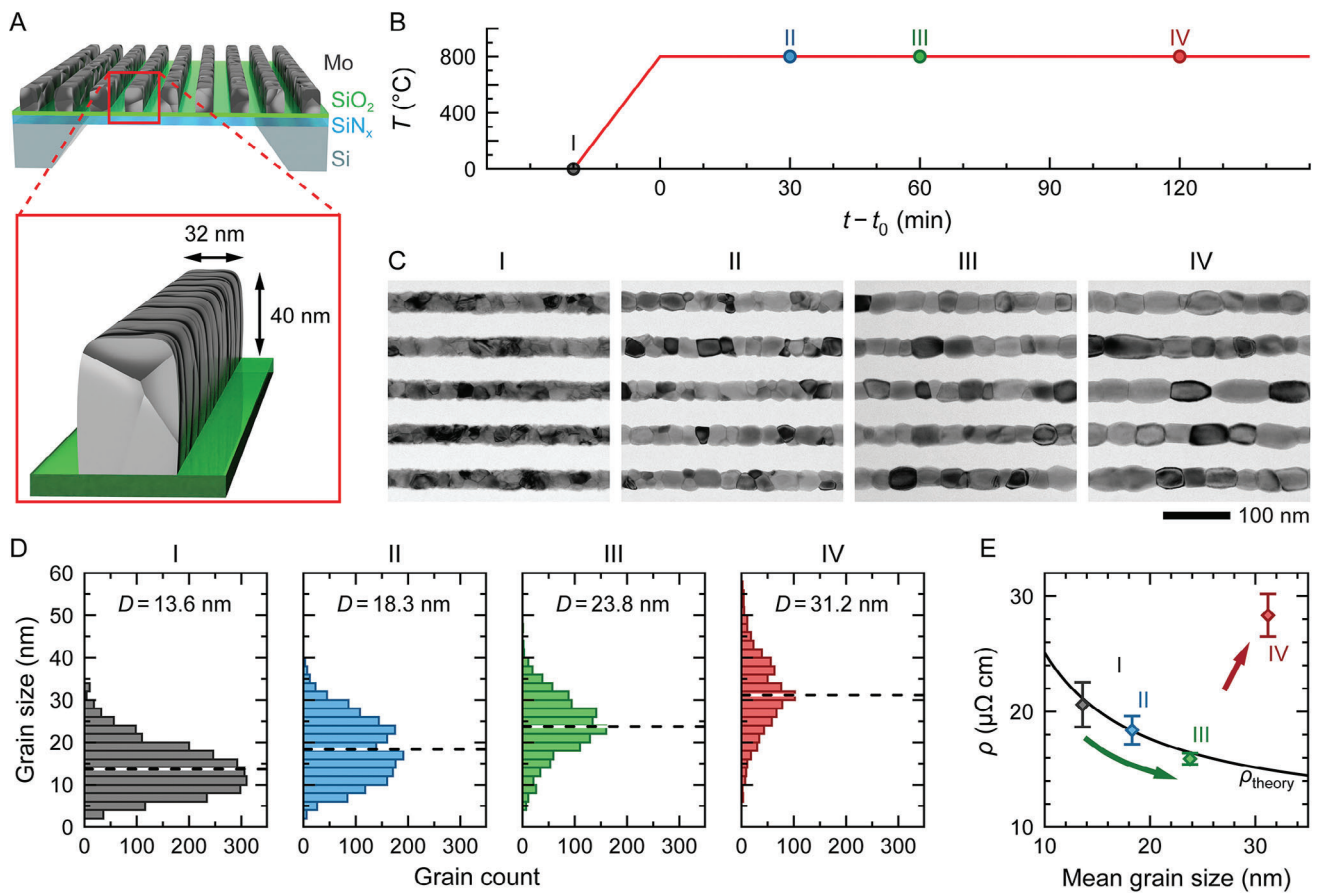
**ADVANCED
SCIENCE NEWS**

www.advancedsciencenews.com

**ADVANCED
ELECTRONIC
MATERIALS**

www.advelectronicmat.de

Figure 1. Furnace-annealed Mo nanowires. A) Schematics of Mo nanowires patterned over a SiO_2/SiN_x film on a Si wafer. B) A typical annealing profile with the dwell temperature of 800 °C, four key conditions are marked with Roman numerals. C) Top-view TEM images of nanowires at the four conditions of (B). D) The corresponding grain size distributions. Here, linear grain size is calculated as the square root of the projected grain area. The mean value D is indicated by the dashed line. E) The corresponding measured resistivity. Theoretical values (black curve) are calculated using the combined FS–MS model using known nanowire geometry and the average grain sizes from (D), with fitted model parameters $p = 0$ and $R = 0.65$.

significantly. This demonstrates that the inverse relation between the average grain size and the resistivity holds as long as the wire cross-section is preserved. And though the NWs after 2 h of annealing feature superior average grain size, deep GB grooves heavily deteriorate its resistivity by forming bottlenecks that reduce the effective wire cross-section.

To better understand the observed transformations in the grain structure, we tracked the evolution of structural features down to the atomic scale in real time during in situ annealing of nanowires inside a TEM. We were mainly interested in the relative time scales of atomic surface diffusion, GB motion, and groove formation at the relevant process temperatures, which would help us identify the optimal annealing conditions. **Figure 2A** shows a series of STEM (scanning TEM) images of a growing Mo grain under stepwise in situ heating: we applied heating profiles with 1-min ramps and a dwell time of 30 s, with the dwell temperature gradually increasing by 50 °C up to 1000 °C (Video S1, Supporting Information). After 30 s at 1000 °C, the initial atomic-scale roughness smoothens out significantly (Figure 2B), and the GBs almost reach their equilibrium (i.e., stable) positions. At the same time, the GB grooves are still negligibly small. Only after another 30 s do they start increasing

and become prominent by 600 s of the total dwell time at 1000 °C. Similar dynamics can be observed in Figure 2C: the surface is still rough after 800 °C but becomes atomically smooth after 30 s at 1000 °C. After that, instead of waiting longer at 1000 °C, we increased the temperature to 1200 °C and saw little changes on the surface but a noticeable deepening of the groove. Note that the bottom groove formed before annealing and remained stable throughout the entire experiment. Figure 2D shows frames from a TEM video of an in situ heating experiment with the temperature raised from 1000 to 1100 °C (Videos S2 and S3, Supporting Information). Here, a small grain is consumed by its bigger neighbors, forming a bump at the GB, which takes ≈75 s to dissimilate fully due to surface diffusion. The final structure also features noticeable grooves, similar to those predicted by Mullins' theory.[38]

These findings are summarized in the schematics in Figure 2E and can be explained as follows. In this nanowire system, both surface smoothening and groove formation rates are governed by the surface diffusion of metal atoms, while the groove depth depends on the GB energy.[38,40] The GB migration rate is also proportional to its energy and the diffusion of metal atoms at the GB. As the GB energy is usually lower than the surface
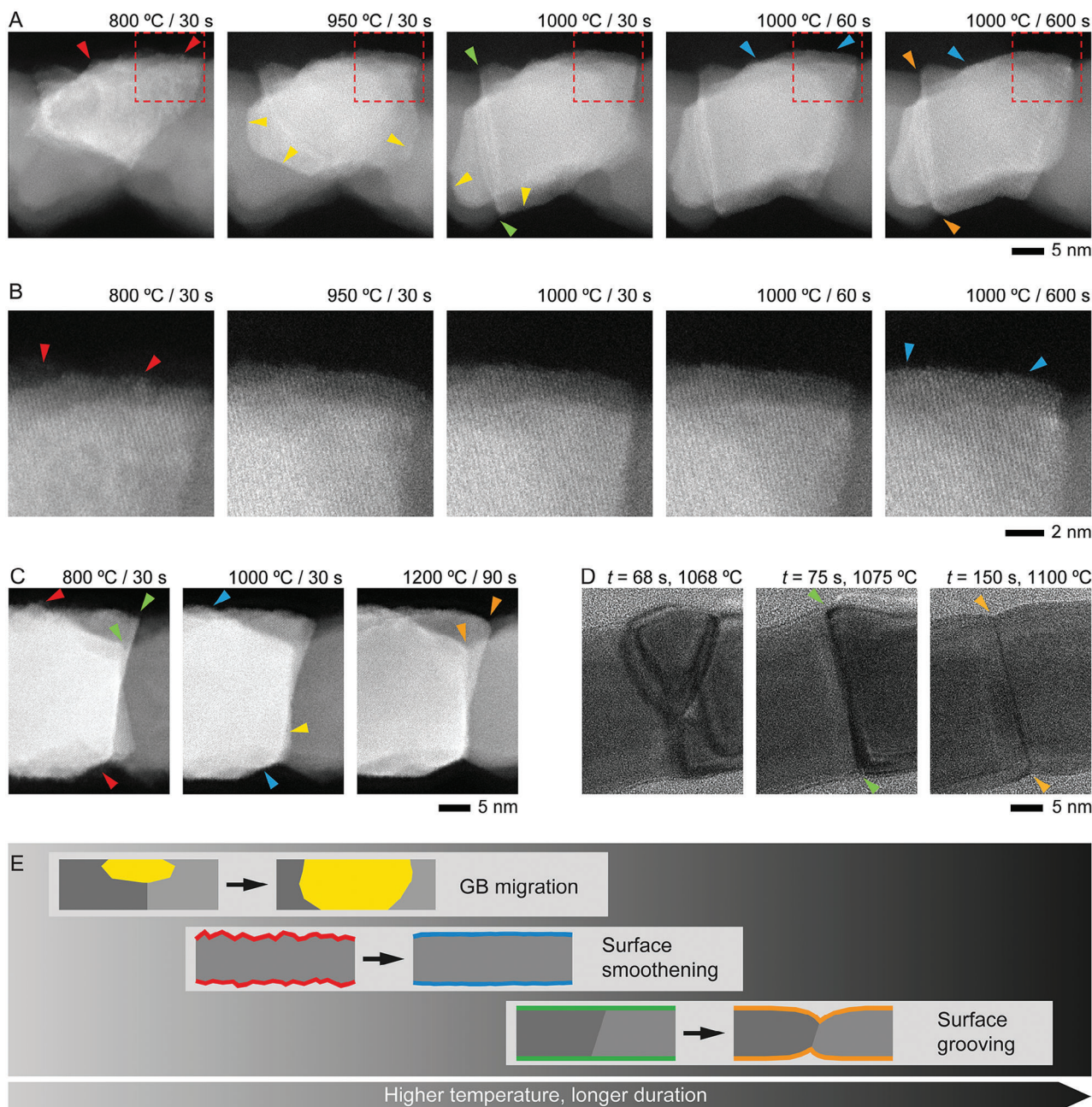
2400035 (3 of 7)

**ADVANCED
SCIENCE NEWS**

www.advancedsciencenews.com

**ADVANCED
ELECTRONIC
MATERIALS**

www.advelectronicmat.de

Figure 2. Evolution of structural features during annealing. A) Series of STEM images of a single grain during a stepwise temperature increase (see Methods, in situ annealing, also Video S1, Supporting Information). Images are labeled by the top temperature and the total annealing time at this temperature. Red arrows point at the examples of surface roughness, blue arrows mark the same areas smoothened. Green arrows mark smooth surface triple junction, while orange arrows show the grooves formed. Yellow arrows show moving GBs. B) Magnified images from the dashed red squares in (A). C) Series of STEM images of a quasi-static GB demonstrating the evolution of surface roughness and grooves. D) Series of TEM images showing the consumption of a smaller grain by its two bigger neighboring grains, followed by the surface smoothening and groove formation during overheating from 1000 to 1100 °C at 1 °C s^{-1} that started at t = 0 s (Videos S2 and S3, Supporting Information). E) Schematics showing the observed time scales of the considered phenomena during in situ annealing.

energy, and since atoms only need to rearrange locally, the GB motion can be activated at a lower temperature. High-energy or high-curvature boundaries start moving first due to a larger driving force, and as the temperature rises, the overall GB mobility increases rapidly. On the other hand, surface diffusion activates at a higher temperature, and it can take longer to reach an equilibrium surface geometry, especially if GBs keep moving.[41] During slow conventional annealing (Figure 1B), the grain growth and surface smoothening/grooving proceed simultaneously. Even though the grooves are noticeable after 60 min

**ADVANCED
SCIENCE NEWS**

www.advancedsciencenews.com

**ADVANCED
ELECTRONIC
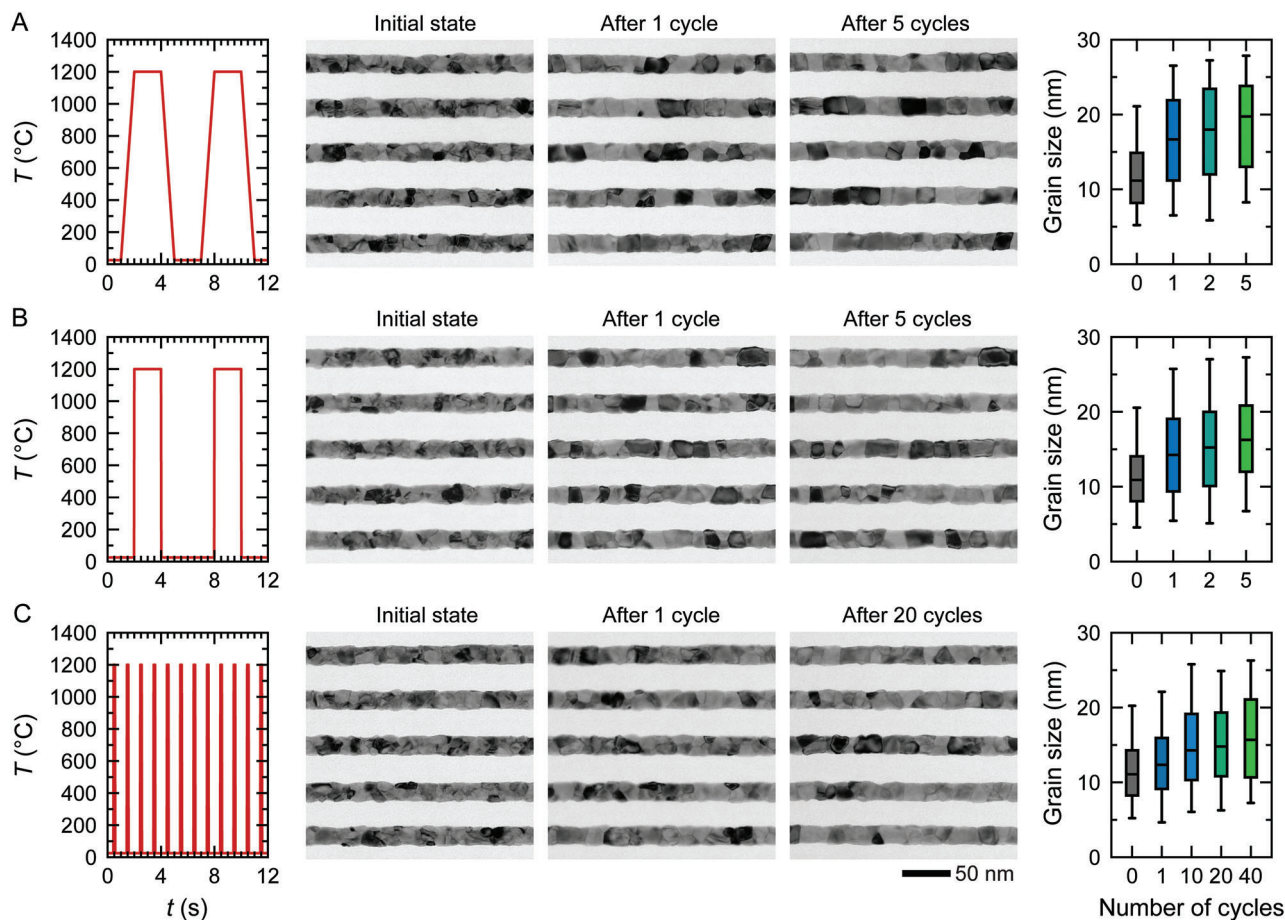MATERIALS**
Open Access

www.advelectronicmat.de

Figure 3. Fast annealing of Mo nanowires and the effect of thermal cycling. A) Profiles with 2 s dwell time at 1200 °C and 1-s ramps. Time between the pulses is arbitrary, as it does not affect the annealing efficiency. TEM images show the grain structure in the same area before annealing, after one cycle, and after multiple annealing cycles. Grain size statistics are calculated for a square area with ten nanowires and represented with a box plot. The box spans from the 25th to the 75th percentile, the middle line marks the median value, and the whiskers correspond to the 5th and 95th percentile values. B) Same for the profiles with 2-s dwell time at 1200 °C and short 20-ms ramps. C) Same for the profiles with only 0.1 s of dwell time at 1200 °C and short 20-ms ramps.

of annealing, they don't seem to restrict the GB motion, and Figure 2D illustrates that a groove having only several atoms in depth just follows its GB as it settles down. We argue that the gradual GB motion is what keeps grooves relatively shallow for the first 60 min during the conventional annealing. Consequently, as the GBs approach their equilibrium configuration, grooves grow deeper to establish a minimum total surface energy for each grain, eventually leading to the effective reduction of the nanowire cross-section observed after 2 h.

Seeing that a higher temperature leads to a faster GB evolution while keeping the surface grooves small, it becomes obvious that increasing the process temperature and ramping rates can drastically improve the annealing efficiency while also reducing the annealing duration, which is crucial for integration. Our tests have shown that 1 h at 800 °C can be substituted with a few minutes at 1000 °C (Video S4, Supporting Information) or a few seconds at 1200 °C. **Figure 3A** shows a fast annealing profile with a 2-s dwell time at 1200 °C and 1-s ramps, along with TEM images and grain size distributions of Mo nanowires before annealing and after applying this profile multiple times in cycles. Despite the short dwell time, we see a dramatic improve-

ment in the grain structure already after one cycle: it features a bamboo pattern, the average grain size reaches ≈20 nm, and the cross-section is very uniform. Repeating this annealing cycle five times leads to further improvements, though the improvement due to each consecutive cycle is smaller than the previous. The final grain structure is largely similar to the result of annealing at 800 °C for 30 min, but the surface grooves are much less prominent here (see Figure S1, Supporting Information for edge roughness comparison), which should positively affect the resistivity. According to our observations, the amount of idle time between the pulses does not affect the annealing efficiency, so it can be adjusted freely.

To test the effect of the ramping rate, we implemented another profile with a 2-s dwell at 1200 °C but faster temperature ramps of only 20 ms (Figure 3B). As before, already the first cycle enhanced the surface smoothness and reduced the number of small grains almost as effectively as with slower ramps. Even though the average grain size increased slightly less, the evolution of the grain size distribution over five cycles is very similar, suggesting that the temperature ramps can be kept as short as possible. We then tested if the same result could be achieved when the thermal

**ADVANCED
SCIENCE NEWS**

www.advancedsciencenews.com

**ADVANCED
ELECTRONIC
MATERIALS**
Open Access

www.advelectronicmat.de

exposure is split into even shorter pulses, using a profile with only 0.1 s dwell time at 1200 °C (Figure 3C). This time, one cycle led to only marginal structure improvement, but after about 20 cycles, the average grain size is as after one 2-s profile in Figure 3B, which validates that this approach is similarly efficient. Shorter pulses can be used when the time-averaged thermal load needs to be minimized, and if implemented to only heat the top surface, this approach can provide means to effectively anneal Mo and other high-melting-point metals while keeping other IC components at a lower temperature.

3. Conclusion

We demonstrated that the nanowire resistivity can be reduced by over 20% by post-patterning annealing and correlated this to the increase in the mean grain size, in agreement with the theory. Over-annealing is shown to induce deep surface grooves, thus reducing the effective cross-section area of nanowires and drastically degrading their electrical performance. By analyzing the behavior of Mo nanowires during the annealing at the atomic scale with high-resolution in situ TEM, we devised a cyclic fast annealing method and demonstrated its high efficiency. Potentially, this approach can improve the grain structure faster and further than the conventional annealing method while avoiding the formation of deep GB grooves. A large-scale implementation of this method can be realized, for example, by using a sweeping laser beam,[27,28,42] and our simulations show that selective heating of metal nanostructures on a substrate is indeed possible (Section S2, Supporting Information). Additionally, as both Si and SiO_2 are transparent for infrared radiation, it should be possible to anneal the entire interconnect network at once with an IR laser, accelerating the manufacturing process. Overall, we believe that this work provides new insight into nanoscale details of high-temperature processing of Mo interconnects, which will facilitate their integration into new generations of high-performance computers.

4. Experimental Section

Fabrication of Mo nanowires: The process is described in detail in one of the other papers,[43] with the only difference that in this work, no pre-annealing was done, that is, the metal grain structure is defined by the deposition and patterning steps only.

Furnace Annealing: A glass tube furnace was used with gold coating pumped down for several hours with a turbopump to reach the base pressure of 3×10^{-6} mbar. The furnace was baked before each annealing experiment for 20 min at 800 °C to release possible contamination from its walls. The ramping up and down times were set to 20 min (ramping rate 39 °C min^{-1}), with a dwell temperature of 800 °C and a dwell time of 30, 60, and 120 min.

Resistivity Measurement: Metal electrode pads were deposited on top of the nanowires using a photoresist mask and lift-off method. Each pair of metal pads connects 50 to 500 Mo nanowires with 30 μm length (Figure S3, Supporting Information). Various metals (Au, Cu, Al, and Cr) were tested, and we selected Al for the pads as it features low resistivity, a protective passivation layer, and its electrochemical potential is lower than that of Mo. A custom-built probe with four tungsten (W) wires connected to a Keithley 2450 source measure unit (Keithley Instruments, Cleveland, OH, USA) was used to determine the resistance at five different temperatures between −196 °C (liquid N_2 boiling point) and 200 °C. The effective total cross-section was derived using the TCR (thermal coefficient of resistivity) method[36,44,45] and used to calculate the resistivity at 20 °C.

TEM Imaging: TEM imaging was done using a JEOL 2010F transmission electron microscope (JEOL Ltd., Tokyo, Japan) equipped with a Gatan OneView camera (Gatan Inc., Pleasanton, CA, USA) at 200 kV, and using a Thermo Fisher Titan S/TEM (Thermo Fisher Scientific Ltd., Hillsboro, OR, USA) equipped with a Gatan K2 IS camera at 300 kV.

In Situ Annealing: In situ annealing was performed using single-tilt Wildfire holders (DENSsolutions, Delft, the Netherlands) for JEOL and Thermo Fisher microscopes. Large free-standing SiN_x windows were etched in the wafer with Mo nanowires and used to transfer Mo nanowires onto the heating chips (Figure S4, Supporting Information). For fast annealing profiles, a custom power source was implemented using a Keithley 6430 SMU controlled by homemade software written in LabView. in situ TEM imaging was done at 10 frames per second with an electron flux of <100 e$^-$ Å^{-2} s^{-1}.

In situ STEM image series in Figure 2A–C and Video S1 (Supporting Information) were acquired as follows. After taking the first STEM image of NWs, a short annealing was performed with 1-min up and down ramps and 30-s dwell at 600 °C. Then the NWs were allowed to cool down to room temperature, and another STEM image of the same grain was captured. This way, STEM images of a series of annealing profiles were recorded, with the dwell temperature increased by 50 °C each time. When the temperature reached 1000 °C, the dwell times instead of the temperature were increased, first by 30 s, then by 60 s, and so on. The time label on the images means the total dwell time at the highest dwell temperature. In Video S1 (Supporting Information), the images corresponding to dwell temperatures up to 1000 °C are labeled only by the highest dwell temperature, as the dwell time is fixed at 30 s. The time label appears from the second frame at 1000 °C and means the total dwell time at 1000 °C. To get more details while keeping the image distortion due to sample drift low, for each final image, 10–20 STEM images taken with short exposure times were aligned and summed.

Image Segmentation and Grain Size Statistics: A machine learning algorithm from the Python[46] TensorFlow[47] library trained on about a hundred TEM images of Mo nanowires and films was used to detect GBs. The resulting segmentation was revised manually to avoid any possible errors. To build each of the histograms in Figure 1D, five square TEM images with ten nanowires (four times the size of any image in Figure 1C) were analyzed, so they contain statistics over the same area. The linear grain size was calculated as the square root of the projected grain area, which is a viable approximation for nanowires where most grains have a shape close to a rectangular prism. Grain size distributions in Figure 3 are represented with box plots. Each box spans from the 25th to the 75th percentile, the middle line marks the median value, and the whiskers correspond to the 5th and 95th percentile values.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

[1] G. E. Moore, *2003 IEEE Int. Solid-State Circuits Conf.*, IEEE, Piscataway, NJ **2003**.

[2] A. Mocuta, P. Weckx, S. Demuynck, D. Radisic, Y. Oniki, J. Ryckaert, *2018 IEEE Symp. on VLSI Technology*, IEEE, Piscataway, NJ **2018**, 147.

[3] A. Razavieh, P. Zeitzoff, E. J. Nowak, *IEEE Trans. Nanotechnol.* **2019**, *18*, 999.

[4] A. Spessot, B. Parvais, A. Rawat, K. Miyaguchi, P. Weckx, D. Jang, J. Ryckaert, *2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symp. (BCICTS)*, IEEE, Piscataway, NJ **2020**, pp 1–8.

[5] C.-T. Tu, Y.-C. Liu, Y.-R. Chen, B.-W. Huang, C.-Y. Cheng, C. W. Liu, *2023 Int. VLSI Symp. on Technology, Systems and Applications (VLSI-TSA/VLSI-DAT)*, IEEE, Piscataway, New Jersey, USA **2023**, p. 1.

[6] E. H. Sondheimer, *Advances in Physics* **1952**, *1*, 1.

[7] A. F. Mayadas, M. Shatzkes, *Phys. Rev. B* **1970**, *1*, 1382.

[8] W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, M. Engelhardt, *J. Appl. Phys.* **2005**, *97*, 023706.

[9] A. Pyzyna, R. Bruce, M. Lofaro, H. Tsai, C. Witt, L. Gignac, M. Brink, M. Guillorn, G. Fritz, H. Miyazoe, D. Klaus, E. Joseph, K. P. Rodbell, C. Lavoie, D.-G. Park, *2015 Symp. on VLSI Technology (VLSI Technology)*, IEEE, Piscataway, NJ **2015**, pp T120-T121.

[10] C.-K. Hu, L. Gignac, R. Rosenberg, *Microelectron. Reliabil.* **2006**, *46*, 213.

[11] C. Witt, K. B. Yeap, A. Leśniewska, D. Wan, N. Jordan, I. Ciofi, C. Wu, Z. Tokei, *IEEE Int. Interconnect Technology Conf. (IITC)*, IEEE, Piscataway, NJ **2018**, pp 54–56.

[12] H. Xu, Z.-J. Hu, X.-P. Qu, H. Wan, S.-S. Yan, M. Li, S.-M. Chen, Y.-H. Zhao, J. Zhang, M. R. Baklanov, *Appl. Surf. Sci.* **2019**, *498*, 143887.

[13] D. Gall, *IEEE Int. Interconnect Technology Conf. (IITC)*, IEEE, Piscataway, NJ **2018**.

[14] D. Gall, *J. Appl. Phys.* **2020**, *127*, 050901.

[15] D. Gall, *J. Appl. Phys.* **2016**, *119*, 085101.

[16] D. Choi, *Nanosci. Nanotechnol. Lett.* **2018**, *10*, 1310.

[17] D. Tierno, K. Croes, A. Ajaykumar, S. Ramesh, G. Van den Bosch, M. I. Rosmeulen, *IEEE Int. Reliability Physics Symp. (IRPS)*, IEEE, Piscataway, NJ **2021**, pp 1–6.

[18] D. S. Fischl, D. W. Hess, *J. Vacuum Sci. Technol. B: Microelectron. Proc. Phenom.* **1988**, *6*, 1577.

[19] D. C. Edelstein, *IEEE International Electron Devices Meeting (IEDM)*, IEEE, Piscataway, NJ **2017**.

[20] A. Fischer, A. Routzahn, T. Lill, *ECS Meeting Abstracts 2020, MA2020-02 (14)*, 1380, https://iopscience.iop.org/article/10.1149/MA2020-02141380mtgabs/meta.

[21] S. Decoster, E. Camerotto, G. Murdoch, S. Kundu, Q. T. Le, Z. Tőkei, G. Jurczak, F. Lazzarino, *J. Vacuum Sci. Technol. B* **2022**, *40*, 032802.

[22] *Daily Metal Prices*, https://www.dailymetalprice.com/metalprice charts.php.

[23] A. G. Worthing, *Phys. Rev.* **1925**, *25*, 846.

[24] C. Fenouillet-Beranger, B. Previtali, P. Batude, F. Nemouchi, M. Cassé, X. Garros, L. Tosti, N. Rambal, D. Lafond, H. Dansas, L. Pasini, L. Brunet, F. Deprat, M. Grégoire, M. Mellier, M. Vinet, *Solid-State Electron.* **2015**, *113*, 2.

[25] S. S. T. Nibhanupudi, D. Prasad, S. Das, O. Zografos, A. Robinson, A. Gupta, A. Spessot, P. Debacker, D. Verkest, J. Ryckaert, G. Hellings, J. Myers, B. Cline, J. P. Kulkarni, *IEEE Trans. Electron Dev.* **2022**, *69*, 4453.

[26] A. Jourdain, M. Stucchi, G. V.d. Plas, G. Beyer, E. Beyne, *2022 IEEE 72nd Electronic Components and Technology Conf. (ECTC)*, IEEE, Piscataway, NJ **2022**, pp 1531–1538.

[27] N. Jourdan, F. Roze, T. Tabata, S. Lariviere, A. Contino, F. Mazzamuto, T. Zsolt, *2020 IEEE Int. Interconnect Technology Conf. (IITC)*, IEEE, Piscataway, NJ **2020**, pp 163–165.

[28] L. Lu, N. Jourdan, R. Daubriac, T. Tabata, F. Roze, L. Thuries, F. Cristiano, Z. Tokei, *IEEE International Interconnect Technology Conf. (IITC) and IEEE Materials for Advanced Metallization Conf. (MAM) (IITC/MAM)*, IEEE, Piscataway, NJ **2023**, pp 1–3.

[29] S. H. Kang, C. Kim, J. W. Morris, F. Y. Génin, *J. Appl. Phys.* **1996**, *79*, 8330.

[30] D. N. Lee, H. J. Lee, *J. Electron. Mater.* **2003**, *32*, 1012.

[31] C.-C. Yang, T. Spooner, P. McLaughlin, C. K. Hu, H. Huang, Y. Mignot, M. Ali, G. Lian, R. Quon, T. Standaert, D. Edelstein, *IEEE International Interconnect Technology Conf. (IITC)*, IEEE, Piscataway, NJ **2017**, pp 1–3.

[32] E. Yoo, J. H. Moon, Y. S. Jeon, Y. Kim, J.-P. Ahn, Y. K. Kim, *Mater. Characterizat.* **2020**, *166*, 110451.

[33] J. H. Moon, S. Kim, T. Kim, Y. S. Jeon, Y. Kim, J.-P. Ahn, Y. K. Kim, *J. Mater. Sci. Technol.* **2022**, *105*, 17.

[34] J. Gao, J. Luo, H. Geng, K. Cui, Z. Zhao, L. Liu, *Materials* **2020**, *13*, 3749.

[35] D. Rafaja, H. Köstenbauer, U. Mühle, C. Löffler, G. Schreiber, M. Kathrein, J. Winkler, *Thin Solid Films* **2013**, *528*, 42.

[36] V. Founta, J.-P. Soulié, K. Sankaran, K. Vanstreels, K. Opsomer, P. Morin, P. Lagrain, A. Franquet, D. Vanhaeren, T. Conard, J. Meersschaut, C. Detavernier, J. Van de Vondel, I. De Wolf, G. Pourtois, Z. Tőkei, J. Swerts, C. Adelmann, *Materialia* **2022**, *24*, 101511.

[37] K. Saidov, I. Erofeev, H. Yan, Z. Aabdin, U. Mirsaidov, *Phys. Rev. Mater.* **2023**, *7*, 063402.

[38] W. W. Mullins, *J. Appl. Phys.* **1957**, *28*, 333.

[39] M. J. Rost, D. A. Quist, J. W. M. Frenken, G. Grains, *Phys. Rev. Lett.* **2003**, *91*, 026101.

[40] A. Ramasubramaniam, V. B. Shenoy, *Acta Materialia* **2005**, *53*, 2943.

[41] L. Klinger, E. Rabkin, *Interface Sci.* **2001**, *9*, 55.

[42] C. S. Hau-Riege, C. V. Thompson, *Appl. Phys. Lett.* **1999**, *75*, 1464.

[43] K. Saidov, I. Erofeev, Z. Aabdin, A. Pacco, H. Philipsen, A. W. Hartanto, Y. Chen, H. Yan, W. W. Tjiu, F. Holsteyns, U. Mirsaidov, *Adv. Funct. Mater.* **2024**, *34*, 2310838.

[44] J. J. Plombon, E. Andideh, V. M. Dubin, J. Maiz, *Appl. Phys. Lett.* **2006**, *89*, 113124.

[45] E. Milosevic, V. Kamineni, X. Zhang, H. Dixit, M. V. Raymond, H. Huang, R. Southwick, C. Janicki, N. Lanzillo, D. Gall, *IEEE International Interconnect Technology Conference (IITC)*, IEEE, Piscataway, NJ **2018**.

[46] G. van Rossum, F. L. Drake, *Python 3 Reference Manual*, CreateSpace, South Carolina, USA **2009**.

[47] *Tensorflow*, https://github.com/tensorflow