Novel Cross-Point Architecture utilizing Distributed Diode Selector for Read Margin Amplification

Taras Ravsher[1,2*], Andrea Fantini[2], Kruti Trivedi[2], Nouredine Rassoul[2], Harold Dekkers[2], Attilio Belmonte[2], Jan Van Houdt[1,2], Valeri Afanas'ev[1,2], Kurt Wostyn[2], Sebastien Couet[2], Gouri Sankar Kar[2]

[1]KU Leuven, Celestijnenlaan 200D, 3001 Leuven, Belgium; [2]IMEC, Kapeldreef 75, 3001 Leuven, Belgium; *taras.ravsher@imec.be

***Abstract*—While cross-point array architecture provides ultimate area efficiency for low-cost memory solutions, it also faces some challenges. On top of the complexity associated with co-integration of a selector device (e.g., a diode) with a resistive memory element (ME), the resulting 1D1R cell suffers from the read margin (RM) degradation due to the voltage redistribution between the two sub-components. The present work provides a detailed investigation of this issue and proposes a novel cross-point architecture to alleviate it. It features a distributed Schottky diode (i.e., spanning the full length of the access line) which simultaneously constitutes an embedded MeSFET, thus providing a tunable connection between the neighboring cells to directly control the voltage across the selected ME. Operation of such an array is discussed, with simulation results confirming effective RM amplification without additional footprint penalty. Finally, the concept is validated experimentally by fabricating InGaZnO-based MeSFET, demonstrating good rectification.**

Keywords—Cross-point arrays, Distributed Schottky diodes, MeSFETs, Oxide semiconductors, Read margin.

I. Introduction

In order to enable a high-density cross-point memory array, a suitable two-terminal selector device is necessary. In case of memory element (ME) supporting unipolar operation, such as phase-change memory (PCM) or voltage-controlled magnetic anisotropy (VCMA) magnetic memory, the role of a selector can be played by a simple diode [1]. Especially relevant in this context are Schottky diodes based on amorphous oxide semiconductors thanks to their compatibility with back-end-of-line (BEOL) integration. For example, we have previously demonstrated a high-performance unipolar Schottky diode based on amorphous InGaZnO (a-IGZO) [2].

The resulting 1 diode – 1 resistive ME (1D1R) cell can be easily integrated into a cross-point array (**Fig. 1a**). **Fig. 1b** shows the measured I-V characteristics of our Pt/IGZO/Mo Schottky diode, with ultra-low reverse leakage and steep sub-threshold slope (with ideality factor n=1.25). However, even with an ideal diode, the 1D1R cell has some limitations. Of particular interest for this work is the degradation of the effective read margin (RM), discussed below.

This work is structured as follows. Section II discusses the origin of the RM degradation in 1D1R cell and possible mitigation strategies, focusing on the RM amplification in a simplified 3-terminal 1D2R cell. Then, in Section III a novel array configuration will be introduced, describing the possibility of integrating such a cell in a compact cross-point structure with a bit cell area of $4F^2$. Next, Section IV will demonstrate the operation of such an array by means of TCAD simulations, specifically focusing on the role of MeSFET-based tunable lateral connections. Finally, Section V will confirm the feasibility of the proposed idea by experimentally demonstrating MeSFET functionality in a Pt/a-IGZO device, which, in turn, was used to calibrate the TCAD model.

II. Read Margin Degradation & Gain Cell

A. Analysis of 1D1R cell

Consider the 1D1R cell in **Fig. 2a**, consisting of a Schottky diode and a resistive ME that can switch between low-resistance (LRS) and high-resistance state (HRS). For the sake of example, assume R_{LRS}=100k and R_{HRS}=200k, translating into a read margin (RM) of 100%. Here, RM is defined as

$$RM_0 = (R_{HRS} - R_{LRS})/R_{LRS} \quad (1)$$

The problem of RM degradation arises when trying to read the combined 1D1R cell, due to the unavoidable voltage redistribution between series-connected diode and resistor. This is illustrated with a graphical biasing point analysis in **Fig. 2b**. Suppose the 1D1R cell is biased with a constant voltage V_{Read} (0.8V in this example). In LRS state this would correspond to a Read current (I_{Read}) of I_{LRS}=2μA. One would expect that in HRS state I_{Read} must be half this value due to doubling of R_{ME}. However, this is not the case, because the decrease in I_{Read} also implies a decrease in current through the diode (I_D), thus inherently leading to a slight decrease in voltage drop across it (V_D). Given that a total voltage across 1D1R is constant, the decreased V_D must be compensated with a corresponding increase in voltage across ME (V_{ME}), as highlighted in **Fig. 2c**. As a result, the drop in I_{Read} in HRS is smaller than the change in ME resistance (I_{HRS}=1.1μA instead of 1.0μA). One can define an *effective* RM of 1D1R as

$$RM = (V/I_{HRS} - V/I_{LRS}) / (V/I_{LRS}) = (I_{LRS} - I_{HRS}) / I_{HRS} \quad (2)$$

Hence, in this case the effective RM is only 82% (compared to the original RM_0 = 100%). The amount of this voltage redistribution, and hence the degree of RM degradation, is determined by the steepness of the diode characteristics (i.e., n), with pronounced deterioration of RM with increasing n. It is important to emphasize that even for an ideal diode (n=1), the RM degradation is inherently present in a 2-terminal 1D1R cell, because of the voltage redistribution between the two series-connected components.

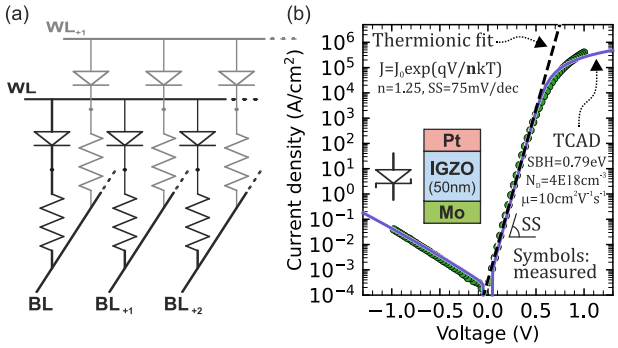

Figure 1. (a) Classical 1D1R cross-point array with unipolar ME and diode selector. (b) Measured I-V characteristics of Pt/IGZO/Mo Schottky diode.

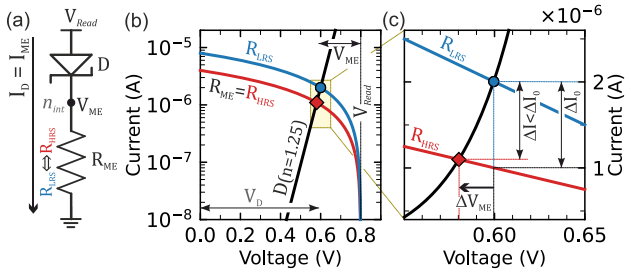

Figure 2. (a) Schematic of a 1D1R cell and (b) bias point analysis for different R_{ME} values with (c) focused view of the highlighted region.

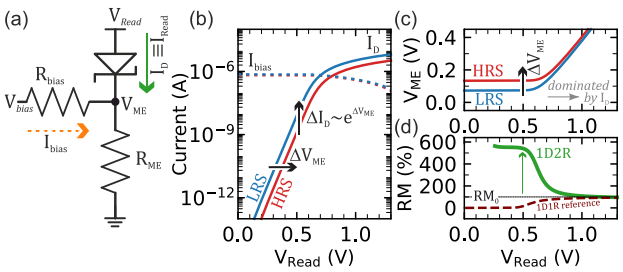

Figure 3. (a) Proposed 3-terminal gain cell, where V_{ME} is controlled directly via a biasing resistor R_{bias}. (b) I_D is exponentially dependent on V_{ME}, which in the limit of $I_D \ll I_{bias}$ itself is independent of I_D and proportional to R_{ME}, as shown in (c). (d) This results in RM amplification above RM_0 (=100%).

B. *3-terminal 1D2R gain cell*

One way to circumvent this issue is by directly controlling the voltage at the internal node between the diode and ME (n_{int}) by means of an external biasing resistor R_{bias} (see **Fig. 3a**). By choosing the resistance and bias values appropriately, one can maintain V_{ME} almost independent of the diode current I_D, as shown in **Fig. 3b,c**. Instead, V_{ME} will be determined by the ratio of the voltage divider between R_{ME} and R_{bias}:

$$V_{ME} \approx R_{ME}/(R_{ME} + R_{bias})*V_{bias} \qquad (3)$$

Assuming $R_{bias} \gg R_{ME}$, Eq. (3) can be approximated by $V_{ME} \approx (R_{ME}/R_{bias})*V_{bias}$. Meaning that V_{ME} is proportional to R_{ME}. In turn, V_{ME} directly controls the voltage across the diode ($V_D = V_{Read} - V_{int}$). Therefore, the value of I_D will depend *exponentially* on the value of R_{ME}. Hence, by taking I_D as the Read current we arrive at the possibility of not only preserving, but even *amplifying* RM beyond its original value. In the example in **Fig. 3d**, the effective RM > 500% could be achieved. It is worth mentioning that the above approximations are strictly valid in the limit of $I_D \ll I_{bias}$. While the analysis becomes more complicated for $I_D \gtrsim I_{bias}$, some RM amplification can be expected in this case as well.

III. Distributed Diode Architecture

At first glance the above-described 3-terminal 1D2R cell seems to be incompatible with dense cross-point array structure. However, as will be shown in this section, it is possible to implement such a biasing scheme with only minor modifications and still preserving the $4F^2$ footprint.

A. *Concept and biasing scheme*

This can be achieved by embedding the semiconductor layer along with the top Schottky contact into the word line (WL) stack, while leaving the bottom Ohmic contacts within individual ME pillars, as illustrated in **Fig. 4a**. We will refer to this structure as a *distributed diode* [3], since the active region of a diode is shared among all the cells along the WL. This arrangement allows for a connection between the neighboring cells along the WL.

Note, the resistance (R_{lat}) of this connection is not fixed, but instead can be modulated by the WL voltage (V_{WL}). Essentially, each segment of this line can be viewed as a metal-semiconductor (MeSFET) transistor, with Schottky electrode acting as a gate. Now, with an appropriate biasing scheme these connections can be used to directly control the V_{ME} through the neighboring cells. Consider the equivalent circuit of the region of interest around the selected cell (along WL direction) shown in **Fig. 4b**. In the proposed scheme, during Read operation, voltage V_{Read} is applied to the selected WL, while the selected bit line (BL) is grounded. Unlike in a typical cross-point V/2 scheme, the unselected BLs (BL^{uns}) are supplied with the same bias as the WL (i.e., V_{Read}). This ensures three things: (i) the selected diode receives full forward bias to access the corresponding cell; (ii) the unselected diodes can be assumed to be (approximately) zero-biased; (iii) there is a non-zero current flow from the nearest neighboring cells into the selected ME through the lateral channel resistors R_{lat}. The combination of these lateral paths can be considered as a lumped resistance R_{bias}. In analogy with **Fig. 3**, this ensures the possibility of RM amplification.

The introduction of such lateral connections may be counter-intuitive, since it appears to create additional leakage paths, that are meant to be contained by the selector device in the first place. However, thanks to the tunability of MeSFET channels, the proposed scheme ensures complete control over these currents.

B. *Critical design considerations*

1) *Disturb to the neighboring cells*

A possible concern one may point to in the proposed operating scheme is the fact that V_{ME} biasing requires passing current through the neighboring unselected cells, potentially disturbing the stored state. To avoid this issue, it is imperative that the (reverse) current through the neighboring cell is sufficiently small. During the Read operation this is achieved automatically, since normal I_{Read} must normally satisfy the same requirement. Moreover, the current through individual neighboring cell is at most $I_{ME}/2$. During the Write operation (which requires larger V_{WL} and V_{BLuns} voltages) one may suspect this current to rise uncontrollably. However, this is not the case since increased $V(BL^{uns})$ will be accompanied with a comparable rise in voltage across the selected ME, hence keeping overall voltage drop across R_{lat}, and hence the biasing current, almost constant.

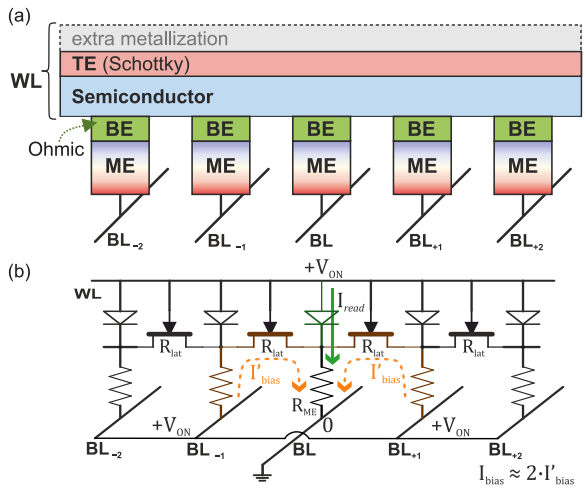

Figure 4. (a) Distributed diode structure and (b) its equivalent circuit. Semiconductor layer and Schottky electrode are embedded within WL.

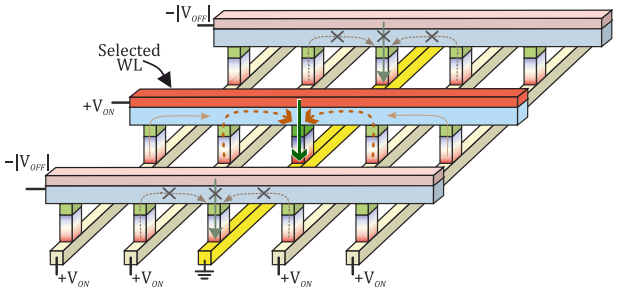

Figure 5. Modified cross-point architecture, showing the proposed biasing scheme. MeSFET channels are active only within the selected WL, while the unselected ones are turned OFF.

2) Interference from the state of the neighboring cells

The magnitude of biasing current (I_{bias}) is determined by the combined resistance of R_{lat} and the value of R_{ME} of the nearest neighbors. Ideally, I_{bias} should not depend on the state of any of the ME cell. This can be achieved by selecting a sufficiently large R_{lat} >> R_{HRS}, so that I_{bias} is dominated entirely by R_{lat}, irrespective of R_{ME} values.

3) Sufficient I_{bias} for RM amplification

At the same time, R_{lat} should not be too large to allow for a sufficient lateral current through MeSFET (I_{lat}) needed to achieve RM amplification. These two requirements limit the range of desired R_{lat} values (i.e., MeSFET strength), that must be chosen in accordance with the target R_{ME} resistance.

4) Lateral selectivity for leakage suppressing

Within a selected WL the lateral current is exploited to achieve RM amplification. However, it is critical to be able to suppress these currents for all the unselected WLs (see **Fig. 5**) to avoid disturbing the cells along the selected BL during Write. This is achieved by dynamically tuning the value of MeSFET resistance R_{lat}, by modulating the depletion region of the Schottky junction via WL voltage (V_{WL}) [4].

IV. TCAD SIMULATION & ARRAY-LEVEL OPERATION

A. Single MeSFET analysis

This selectivity is illustrated with a TCAD simulation of a simplified MeSFET structure in **Fig. 6**. It shows that current through the lateral channel I_{lat} can be tuned in a wide range, depending on the applied gate voltage. At the same time, this device also acts as a diode selector with good rectification. Note, this TCAD model was calibrated to an experimentally measured MeSFET device (discussed in Section V). Now, by choosing the appropriate biases, it is possible to enable sufficient lateral inter-ME conduction within the selected WL, while suppressing the leakage through the unselected ones.

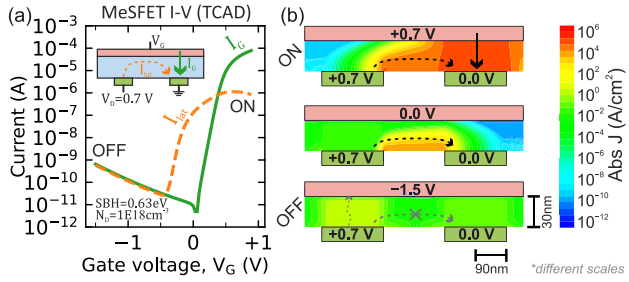

Figure 6. MeSFET as an in-line selector device. (a) Simulated I-V characteristics. (b) Snapshots of current density in different regimes.

B. Distributed diode structure

This is illustrated with an extended TCAD model that inludes multiple ME connections (11 in total) to emulate the behavior of a string of cells along the WL direction. Also here, calibrated model parameters are used. **Figs. 7a-c** show the snapshots of current density distribution under various biasing conditions. **Fig. 7a** and **Fig. 7b** represent the selected WL during Write and Read operation, respectively. Importantly, we include a series resistors to simalate R_{ME}. All the unselected R_{ME}'s are set to 100k, while the selected R_{ME} varies between 100k (LRS) and 200k (HRS) to assess the effective RM. **Fig. 7d** shows the V_{WL} dependence of the Read current (sensed through the WL) I_{WL} for different R_{ME}, with the extracted RM shown in **Fig. 7e**. A clear RM amplification at target V_{Read} is confirmed. **Fig. 7d** also verifies that I_{BL}^{uns} saturates at a fixed value, preventing disturb to the unselected cells during Write operation, as discussed in Section III.B.1. Furthermore, it is independent of R_{ME}.

Fig. 7c models the situation in the unselected WLs. Here, a worst-case scenario is assumed, in which all the unselected BLs are biased with V_{Write}=+1.5V. It confirms effective suppression of I_{lat}, as evidenced from **Fig. 7f**. However, due to strong reverse bias across the unselected cells, their reverse leakage component becomes more pronounced.

C. Array operation and scaling

To further confirm the above conclusions, we perform a simulation on a small array (5x5) to visualize the current flow in a realistic scenario (**Fig. 8**). It clearly shows that only the selected WL is active, while all the others are turned OFF. It also illustrates the dominant role of the nearest neighboring BLs in providing the I_{bias}. This is expected, since the unselected diodes along the selected WL are effectively zero-biased, with negligible votage drop between MEs further from the selected one, as is visible in **Fig. 7a,b**. These observations are important in terms of target non-linearity specifications.

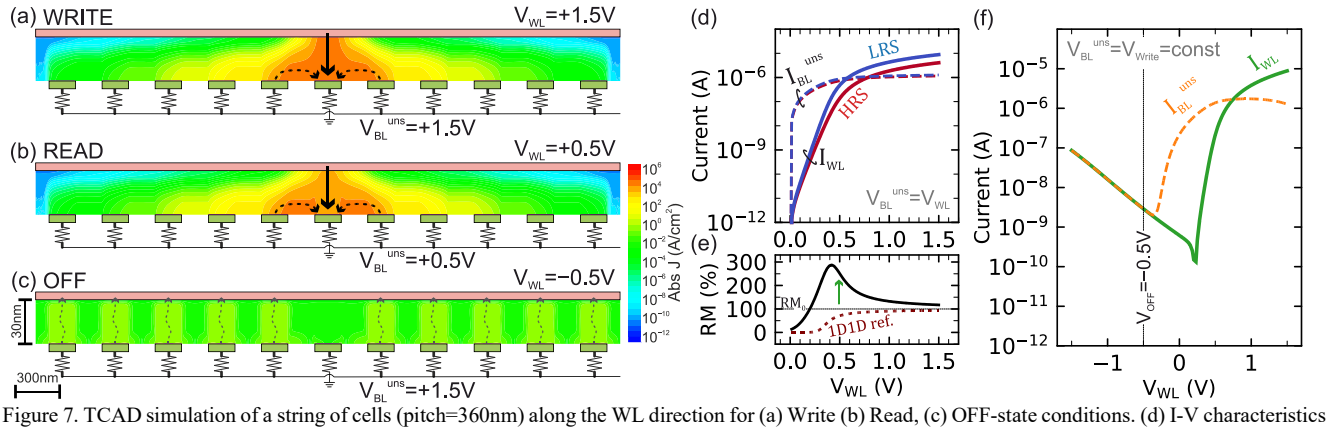

Figure 7. TCAD simulation of a string of cells (pitch=360nm) along the WL direction for (a) Write (b) Read, (c) OFF-state conditions. (d) I-V characteristics within the selected WL for different R_{ME} and (e) extracted effective RM, showing amplification above RM_0 and 1D1R reference. (f) OFF-state selectivity.

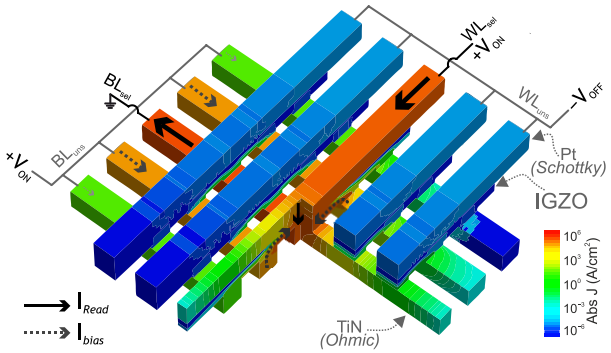

Figure 8. Array-level TCAD simulation illustrating the current flow during operation. Only the selected WL is active, with biasing current composed primarily of nearest-neighbor BL contributions.

Specifically, for the lateral channel it is sufficient to achieve non-linearity factor in the order of the width of the array, N (~10^3 for Mbit array), since only the nearest-neighbors along the selected BL contribute to the leakage current. Instead, it is more important to control the reverse leakage of the unselected diodes, since they constitute most of the array and their contribution scales as ~N^2 [1].

Another consideration is the need to provide some non-functional "dummy" BLs to ensure uniform I_{bias} levels for all the functional cells. However, thanks to the exponentially decreasing contribution from each subsequent neighboring cell further from the selected one, only a few (~2-3) of such dummy BLs may be sufficient, minimizing the area overhead.

V. Experimental MeSFET Demonstration

A. Device fabrication

In order to demonstrate the feasibility of a distributed diode architecture we focus first on its fundamental building block – a single MeSFET device. For this purpose we successfully integrated Pt/IGZO/TiN MeSFET stack, depicted in **Fig. 9a**. It consists of a ~30nm thick a-IGZO layer deposited on top of a high-workfunction metal (Pt), forming a Schottky contact that acts as a gate. The back gate electrode could be contacted via highly-doped p-type Si substrate, with additional n++ implantation and 5nm TiN under the Pt layer included to avoid Schottky barrier formation with underlying substrate. Note, this resulted in a parasitic pn diode in series with target device that must be compensated for during analysis. The TiN/Pt/a-IGZO stack was etched to define the active area, followed by the deposition and planarization of SiO_2 and subsequent contact hole definition. TiN/W stack was used to form four Ohmic contacts from the top side, mimicking the target distributed diode structure. Further details of an integration process can be found elsewhere [5-6]. Note, while the fabricated structure is inverted with respect to those discussed above (i.e., Schottky gate on the bottom), it is fully compatible with the overall concept (by swapping WL and BL notations).

B. Electrical characteristics

The I-V characteristics of the as-fabricated device and after 200C/1h anneal in air are shown in **Fig. 9b**. Before anneal no effective gate control over lateral channel is observed, while the slightly non-linear nature of gate current can be attributed to the parasitic pn-diode. This is likely caused by the excessive doping (N_D) of the as-fabricated IGZO layer due to its sensitivity to H_2, that is known to require O_2 anneal to recover effective gate modulation [7]. Similarly, in the case of MeSFET, post-fabrication anneal can reduce N_D

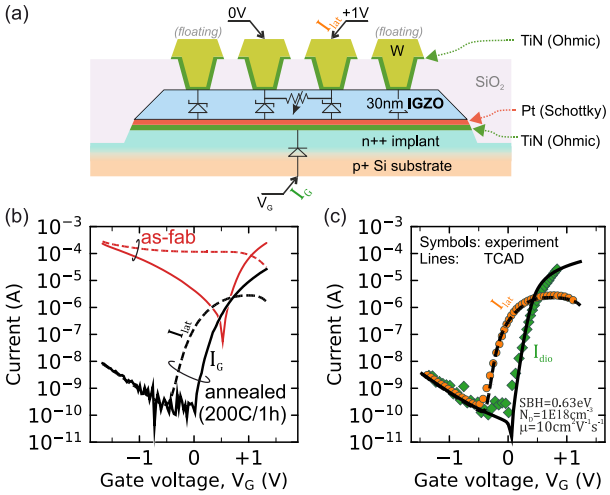

Figure 9. (a) Structure of the fabricated device. (b) Electrical characterization of the fabricated device before and after oxygen anneal. (c) Comparison of measured and simulated characteristics.

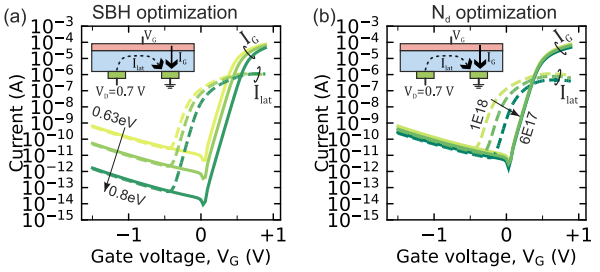

Figure 10. Pathways for further optimization. (a) Increasing SBH to suppress reverse leakage. (b) N_D reduction for improved channel control.

to enable effective gate control over lateral channel. The MeSFET channel can be fully switched OFF at V_{OFF}= −0.5V. **Fig. 9c** shows the measured I-V of the annealed sample, compensated for the additional voltage drop across the series pn diode. It is possible to completely reproduce the experimental data with a TCAD simulation (using the same material parameters as used in **Fig. 6** and **Fig. 7**).

Summary & Outlook

To summarize, we proposed a novel cross-point architecture with a distributed diode and an in-line embedded MeSFET lateral channel that is capable of achieving effective RM amplification. We further demonstrated MeSFET operation with an IGZO channel and verified array operation with TCAD simulations. While the fabricated device shows good performance, there is still room for further optimization by increased Schottky barrier height (SBH) and reduced N_D (see **Fig. 10**), to ensure low leakage and effective gate control even for aggressively scaled dimensions. Additionally, other semiconductor/metal materials may be considered.

Acknowledgment

This work was performed within Imec Industrial Affiliation Program on MRAM devices. T.R. thanks FWO – Research Foundation Flanders for funding (grant 1SD4721).

References

[1] M. Gupta et al., *ESSDERC 2022*, doi: 10.1109/ESSDERC55479.2022.9947187.
[2] S. H. Sharifi et al., *IMW 2020*, doi: 10.1109/IMW48823.2020.9108124.
[3] F. A. Perner, A. L. VanBrocklin, W. B. Jackson, US6937509B2, 2005.
[4] F. J. Klüpfel et al., *IEEE T-ED*, 60/6 (2013), doi: 10.1109/TED.2013.2257173.
[5] L. Kljucar et al., *SSDM 2019*, doi: 10.7567/SSDM.2019.G-1-02.
[6] A. Kruv et al., *IEEE T-ED*, 70/9, 2023, doi: 10.1109/TED.2023.3297976.
[7] S. Subhechha et al., *Symposium on VLSI Technology 2021*, pp. 1-2.