Differential Interconnects with Integrated Equalization and Common-Mode Filtering for Broadband Signal Integrity Enhancement in High-Speed PAM-4 Signaling

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***Abstract*—In high-speed differential interconnects on printed circuit boards, signal integrity (SI) issues arise when neglecting the inherent low-pass characteristic and ubiquitous presence of common-mode noise. This work proposes a novel open-circuited stub equalizer with integrated common-mode filter in order to compensate for the low-pass characteristic while simultaneously suppressing the transmission of unwanted common-mode noise to the receiver. A theoretical analysis of the open-circuited stub equalizer is conducted, and suitable approximations are derived to facilitate equalizer synthesis. Experimental validation is provided by a test structure consisting of a 20 cm microstrip serpentine delay line for which a 4 GHz equalizer is designed. Frequency-domain measurements show a 1-dB bandwidth up to 3.97 GHz with a passband ripple of 0.38 dB for the differential mode and a significant reduction in transmission for the common mode. The resulting SI enhancement increases the possible data rate from 6 Gbps to 20 Gbps using a PAM-4 (pulse amplitude modulation 4-level) modulation scheme.**

***Index Terms*—differential signaling, passive equalization, common-mode filtering, signal integrity, PAM-4**

I. Introduction

NOWADAYS, data rates in digital communication protocols, such as PCIe, are higher than ever and will keep increasing over the coming years [1]. However, this trend is a major source of signal integrity (SI) issues in high-speed data transmission. When going to higher frequencies, interconnects become electrically longer, which leads to a general low-pass characteristic in the transmission coefficient of the interconnect, caused by several types of frequency-dependent losses, such as the skin-effect (conductor), substrate and radiation losses. Additionally, the surface roughness and finish of the conductors, which are heavily influenced by the manufacturing process, are also an important source of losses, particularly at higher frequencies [2]. The resulting inherent low-pass effect in long interconnects is one of the principal limiting factors of communication speeds on printed circuit boards (PCBs). It causes pulse distortion and attenuation, which is detrimental for SI. However, several equalization techniques are available to address this problem, with passive equalization providing a cost-effective yet efficient solution [3]. A passive equalizer removes the unwanted low-pass effect by attenuating the low-frequency components, while leaving the higher frequency components unaffected to achieve a flat channel with a linear phase response.

A second problem in high-speed communication is related to differential signaling, which is often preferred over single-ended signaling owing to its favorable SI properties [4]. However, when the symmetry of the differential pair is broken, e.g., due to presence of bends [5], mode conversion leads to common-mode noise. This common-mode noise is unwanted, deteriorates the SI at the receiving end of the interconnect, and can result in EMI (electromagnetic interference).

In this work, a novel passive, differential equalizer topology is proposed based on the open-circuited stub compensation approach of [6]. However, its application potential and capabilities are augmented through integration of common-mode filtering into the topology. Additionally, simulation and measurement results of the novel equalizer are provided, yielding a more thorough validation of the functionality compared to [6], which only provided simulation results. The method for incorporation of common-mode filtering described in this work aligns with the approach reported in [7]. Nevertheless, employing the open-circuited stub technique results in an SI enhancement for the proposed topology that exceeds the one reported in [7].

Section II discusses the theoretical background of the open-circuited stub equalizer and introduces approximations to the topology where deemed appropriate for efficient design. Section III provides experimental validation of the topology in both the frequency domain and time domain. Conclusions are provided in Section IV.

II. Equalizer Topology

A. Operating modes of the equalizer

Fig. 1 presents the single-ended version of the proposed equalizer topology. The open-circuited stub TML_2 makes the load of TML_1 frequency-dependent. This introduces a bandwidth enhancement compared to only using TML_1 and R_t, as is the case in [7], assuming that TML_2 is shorter than TML_1. Applying microwave circuit theory to this novel topology,

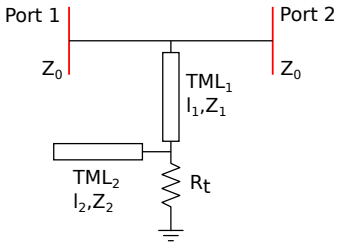


Fig. 1: Schematic representation of the single-ended equalizer topology.

yields an intricate expression for the transmission scattering parameter (S-parameter) S_{21}. This expression, however, does not allow straightforward equalizer synthesis. To tackle this, the frequency range of interest is split into different operating modes and approximations are introduced to the topology for each specific operating mode.

Three operating modes are distinguished. At DC, and very low frequencies, transmission line effects are neglected, so the topology reduces to a single shunt resistor R_t. For frequencies where TML_2 is electrically short, this open-circuited stub behaves predominantly capacitively and hence, it can be replaced by a capacitor in the schematic of Fig. 1. Finally, at its resonance frequency f_{res}, the stub becomes a short circuit. Consequently, TML_2 and R_t are replaced by a short circuit in the schematic of Fig. 1. The resulting expressions for S_{21} of the approximated topologies are less intricate and lend themselves better for design of the equalizer.

Fig. 2 compares the transmission $|S_{21}|$ of the exact equalizer impedance and the three aforementioned approximations. The DC approximation coincides nicely with the exact expression. Replacing the open-circuited stub by a capacitor yields accurate results up to a frequency $f_{cap} = f_{res}/2$. The stub impedance can no longer be accurately linearized to the one of a capacitor for frequencies above f_{cap}. Finally, at the resonance frequency f_{res}, both the $|S_{21}|$ value and its slope coincide with the exact result, but they obviously deviate for frequencies above and below f_{res}.

The aforementioned topology is subsequently applied

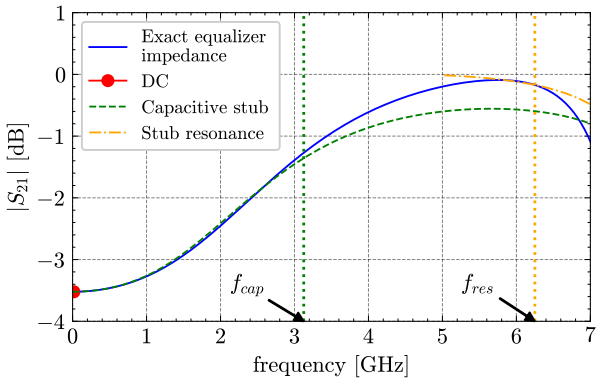


Fig. 2: Comparison between transmission for the exact equalizer impedance and for the proposed approximations facilitating equalizer synthesis.

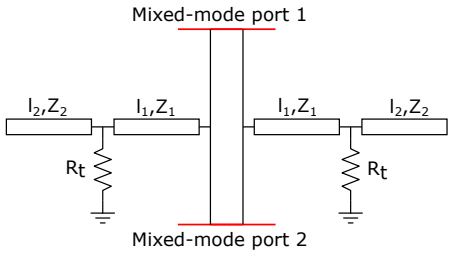


Fig. 3: Schematic representation of the differential equalizer combining two single-ended equalizers.

to differential interconnects. A differential version of the equalizer is obtained by combining two single-ended ones as shown in Fig. 3.

B. Common-mode filter

The astute reader might remark that the topology of Fig. 3 only introduces common-mode filtering to the differential pair through attenuation induced by the resistors R_t. However, by implementing the topology of Fig. 3 in microstrip line technology and placing the equalizer in the ground plane, as depicted in Fig. 4, a defect is introduced in the return path of the common-mode current. This defect attenuates the common-mode transmission and thus reduces the noise at the receiver [7]. Note, however, that this choice creates a slot in the ground plane which could be a source of radiation and hence evoke electromagnetic compatibility issues. Nevertheless, by dimensioning the slot such that it is poorly matched to the common-mode impedance, the common-mode power wave gets reflected by the slot, as such mitigating possible slot radiation.

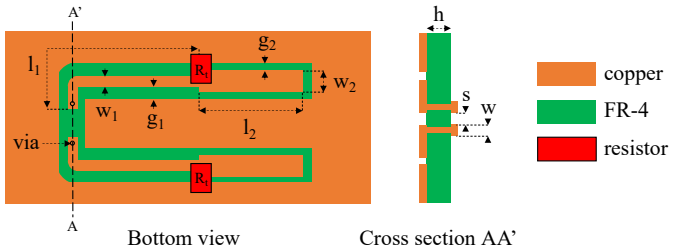


Fig. 4: Bottom view and cross-section of a 4 GHz equalizer for a 20 cm microstrip delay line on an FR-4 substrate.

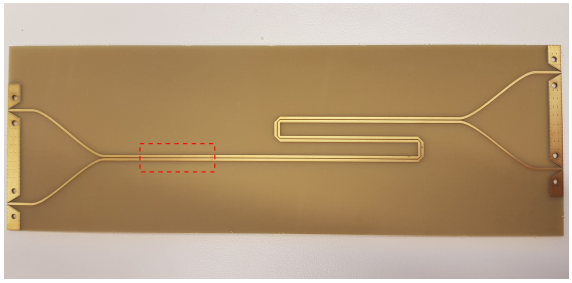
III. Design and Experimental Validation

To provide experimental validation for this topology, a test structure is designed on a two-layer PCB. More specifically, an equalizer with a 4 GHz bandwidth is designed to compensate the low-pass characteristic of a 20 cm differential serpentine delay line in microstrip line technology on a 1 mm thick, two-layer FR-4 substrate (ϵ_r = 3.9, tanδ = 0.022). The values of all the relevant parameters, as defined in Fig. 4, are listed in Table I. These values are obtained by following the design procedure described below.

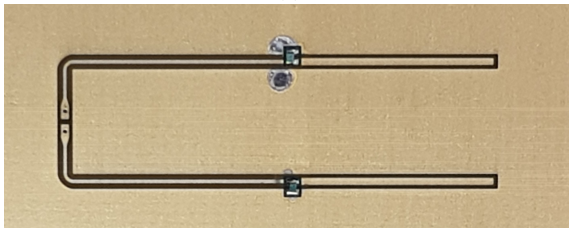
The design process consists of three distinct steps. First, the equalization level and bandwidth are determined based on the low-pass characteristic that needs to be equalized. In a next step, the parameter values are determined by employing

TABLE I: Design parameters for the 20 cm differential microstrip delay line with 4 GHz equalizer of Fig. 4.

Parameter	Value	Parameter	Value
l_1	17 mm	l_2	12 mm
w_1	0.20 mm	w_2	0.4 mm
g_1	0.35 mm	g_2	0.25 mm
Z_1	95.70 Ω	Z_2	70.97 Ω
R_t	50 Ω	h	1 mm
w	0.9 mm	s	0.32 mm



(a)



(b)

Fig. 5: Pictures of the fabricated microstrip delay line with 4 GHz equalizer: (a) Top view of the signal lines, where the dashed rectangle indicates the placement of the equalizer in the ground plane. The tapering is needed to attach four female Southwest End Launch 2.92mm connectors; (b) Close-up of the equalizer structure in the ground plane.

the approximations of Section II-A: the desired equalization level and DC approximation yield a value for R_t, the desired bandwidth and resonance approximation are used to dimension TML_2, and lastly the capacitive approximation combined with the slope of the low-pass characteristic yields the parameters of TML_1. In a final step, the characteristic impedances of both TML sections are optimized using a full-wave solver to obtain a maximally flat transmission coefficient.

Simulations, using CST Microwave Studio's frequency-domain solver, and measurements are performed to verify the obtained equalization effect and common-mode filtering. Pictures of the fabricated test structure are provided in Fig. 5. The following two sections discuss the realized frequency- and time-domain behavior, respectively.

A. *Frequency-domain performance*

The frequency-domain performance is assessed by observing the mixed-mode S-parameters of the differential circuit. These are obtained by means of a four-port measurement using the Keysight PNA-X Network Analyzer N5242B. Through-Reflect-Line (TRL) calibration is applied during post-processing to remove the effect of the connectors. Firstly, the equalization behavior is verified by analyzing the differential-mode transmission magnitude $|S_{\mathrm{dd21}}|$, provided in Fig. 6. It is clear that the equalizer succeeds in compensating for the low-pass effect of the delay line. The equalized line exhibits a flat passband, with a negligible ripple of 0.38 dB, and a 1-dB bandwidth of 3.97 GHz. Variations in the group delay are restricted to 63 ps inside the passband, ensuring that inter-symbolic interference is limited. From the aforementioned observations, it is deduced that the equalizer operates as intended. Additionally, simulated and measured results only show minor differences.

In order to asses the common-mode filtering, the common-mode transmission $|S_{\mathrm{cc21}}|$ of the test structure with and without equalizer is provided in Fig. 7. It is observed that the common-mode transmission is considerably lower when the equalizer is used. This is partly owing to the attenuation by the resistors R_t of Fig. 3 and partly owing to the defect in the return path for the common-mode current, as mentioned in Section II-B. The attentive reader notices the resonance around 1.5 GHz, which could be an indication for undesired slot radiation. However, when looking at the common-mode reflection $|S_{\mathrm{cc11}}|$ of the equalized delay line, also provided in Fig. 7, a peak is observed around 1.5 GHz. A detailed full-wave analysis revealed that the power gets reflected and not radiated.

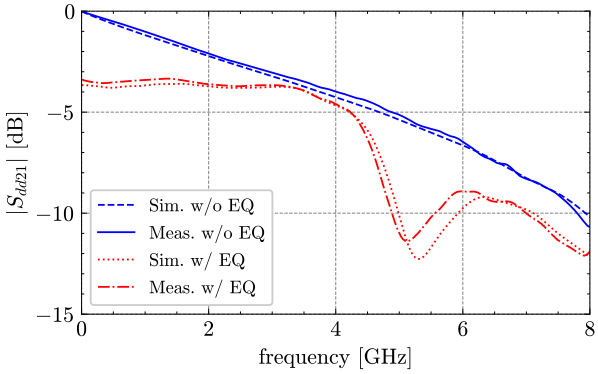


Fig. 6: Comparison between measured and simulated $|S_{\mathrm{dd21}}|$ of a 20 cm microstrip delay line with and without 4 GHz equalizer.

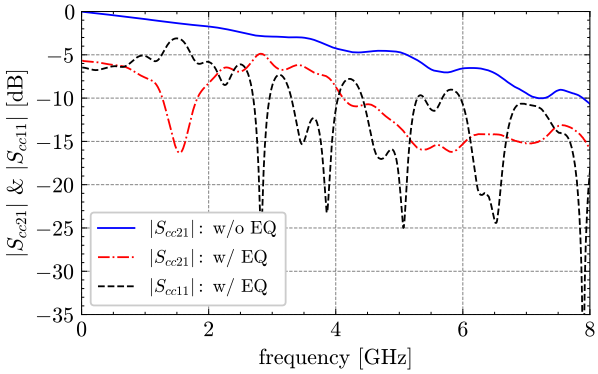


Fig. 7: Comparison between measured $|S_{\mathrm{cc21}}|$ and $|S_{\mathrm{cc11}}|$ of a 20 cm microstrip delay line with 4 GHz equalizer and measured $|S_{\mathrm{cc21}}|$ of the reference delay line.

B. Time-domain performance

The frequency-domain analysis shows promising results with regard to the desired equalization effect and common-mode filtering. However, a time-domain analysis is still essential to assess the SI enhancement. For this purpose, eye diagrams of a PAM-4 (pulse amplitude modulation 4-level) modulation scheme are simulated in Keysight ADS using the *measured* S-parameters. The maximum pulse amplitude is set at 1 V, the 10%-90% rise/fall times equal 10% of the symbol period and a trapezoidal pulse shape is used. Fig. 8 provides the obtained average eye height and width as a function of the bitrate for the delay line with and without equalizer. The reported values are the average value across the three eyes of the PAM-4 modulation scheme.

For low bitrates, compared to the reference delay line, the eye heights are lower when the equalizer is used due to the attenuation of the low frequency components. However, for bitrates of approximately 4 Gbps and higher, the eye heights are bigger. Moreover, from Fig. 8b it is clear that the eye widths are always bigger when the equalizer is added. At a bitrate of 6 Gbps, where the reference line's eyes are still (somewhat) open, the average eye height improves by 187.69% and the average eye width by 197.43% relative to the reference case. Additionally, it is demonstrated that the equalizer keeps the eyes open up to 20 Gbps (compared to only 6 Gbps for the reference delay line). Summarizing all the aforementioned findings, it can be stated that a significant improvement in SI is obtained.

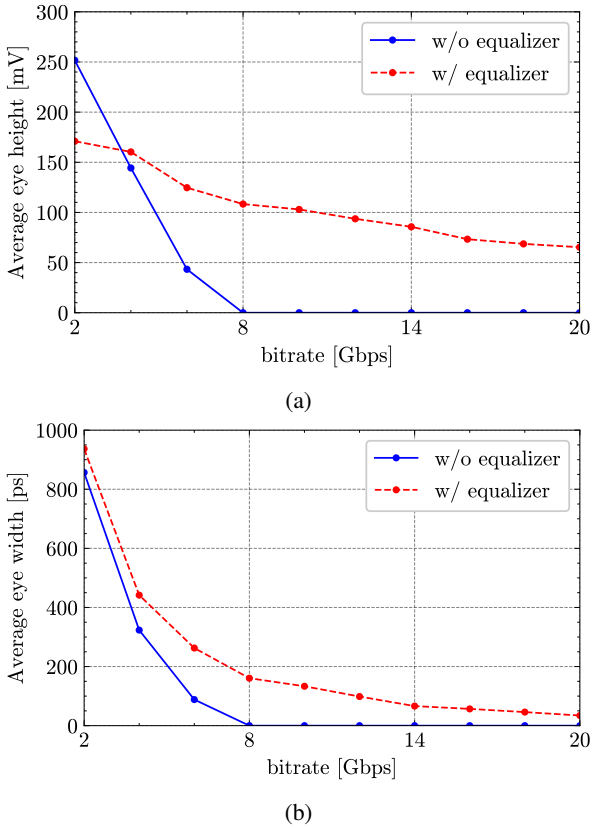


Fig. 8: Comparison between (a) average eye height and (b) average eye width for a 20 cm microstrip delay line with and without 4 GHz equalizer.

IV. Conclusion

This work focused on the design of a novel passive, differential equalizer with integrated common-mode filtering using an open-circuited stub topology. To perform the equalizer synthesis, design-oriented approximations were introduced to the topology based on specific frequency regions. The theoretical discussion was subsequently applied to a 20 cm differential delay line in microstrip line technology for which a 4 GHz equalizer was designed. A 1-dB equalization bandwidth of 3.97 GHz was obtained for the differential signal while simultaneously suppressing the undesired common-mode noise. Both of these observations lead to a significant SI improvement with possible bitrates up to 20 Gbps in a PAM-4 scheme compared to only 6 Gbps for the reference case. In addition, for this bitrate of 6 Gbps, adding the equalizer improves the eye height up to 187.69% and the eye width up to 197.43%. As final remark it is mentioned that the presented equalizer is not restricted solely to microstrip line configurations. It can also be applied to other types of interconnect technologies such as stripline and grounded coplanar waveguide. Hence, the discussed equalizer topology presents a cost-effective, broadband solution facilitating high-speed communication across long interconnects on PCBs.

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