npj | 2D materials and applications

Article

Published in partnership with FCT NOVA with the support of E-MRS

https://doi.org/10.1038/s41699-024-00482-9

Evidence of contact-induced variability in industrially-fabricated highly-scaled MoS_2 FETs

Luca Panarella [1,2] ✉, Ben Kaczer[2], Quentin Smets [2], Stanislav Tyaginov [2], Pablo Saraza Canflanca[2], Andrea Vici[1,2], Devin Verreck[1,2], Tom Schram [2], Dennis Lin [2], Theresia Knobloch [3], Tibor Grasser [3], César Lockhart de la Rosa [2], Gouri S. Kar[2] & Valeri Afanas'ev [1,2]

Evidence of microscopic inhomogeneities of the side source/drain contacts in 300 mm wafer integrated MoS_2 field-effect transistors is presented. In particular, the presence of a limited number of low Schottky barrier spots through which channel carriers are predominantly injected is demonstrated by the dramatic current changes induced by individual charge traps located near the source contact. Two distinct types of "contact-impacting traps" are identified. Type-1 trap is adjacent to the contact interface and exchanges carriers with the metal. Its impact is only observable when the adjacent contact is the reverse-biased FET source and limits the channel current. Type-2 trap is located in the AlO_x gate oxide interlayer, near the source contact, and exchanges carriers with the channel. Its capture/emission time constants exhibit both a gate and drain bias dependence due to the high sensitivity of the contact regions to the applied lateral and vertical fields. Unlike typical channel-impacting oxide traps, both types of reported defects affect the Schottky barrier height and width rather than the threshold voltage and result in giant random telegraph noise (RTN). These observations indicate that the contact quality and geometry play a fundamental role in the ultimate scaling of 2D FETs.

Alongside the increasingly challenging efforts to continue the scaling of silicon-based electronics, field-effect transistors (FETs) based on two-dimensional transition metal dichalcogenides (TMDs) stand out as one of the most promising candidates for the sub-nanometer technology nodes after 2030[1–4]. However, devices with high, stable, and reliable performance are still a distant goal requiring special research attention[5,6].

The two-dimensional nature of the semiconductor channel poses major challenges for the development of a commercially feasible 2D device technology, with the achievement of high-quality interfaces with the surrounding materials representing a particularly difficult task. Firstly, the weak out-of-plane Van der Waals (VdW) interactions exerted by 2D semiconductors hinder the nucleation of oxide materials and are responsible for the formation of non-passivated bond-rich interfaces and defect-rich gate dielectrics, which in turn result in large charge trapping and limit the use of typical 3D insulators[7–12]. Secondly, the fabrication of good metal/2D semiconductor contacts has proven to be anything but trivial due to untunable Schottky barrier heights and strong Fermi level pinning, which eventually cause excessively large contact resistances[13–15]. In addition to that, the choice of contact geometry for fully integrated devices is still a matter of debate, as two major options are currently under investigation[16,17]: top contacts, i.e. the metal/channel interface above the 2D material and parallel to its plane, and side contacts, i.e. the metal/channel interface at the edge of the 2D material. Top contacts can be obtained by depositing the metal on top of the 2D channel and generally provide better performance with lower contact resistance[18,19]. However, there is no straightforward path for scalable and integrable top contacts on monolayer TMDs in a high-throughput industrial processing environment[20]. Side contacts, on the other hand, can be more easily implemented in devices with stacked gate-all-around 2D channels[21–23], which will be needed to outperform the upcoming technology nodes based on gate-all-around stacked Si nanosheets[24]. Nevertheless, the achievement of high-quality side contacts is a challenging task[25–30]. Indeed, etching through the top capping layer and the TMD channel is required, which possibly introduces significant damage to the contact environment, such as defects and etch residues at the metal/TMD interface. Furthermore, the time delay and exposure to an uncontrolled ambient between the trench etch and the metal deposition steps contribute to the formation of

[1]KU Leuven, Celestijnenlaan 200D, Heverlee, 3001, Belgium. [2]imec, Kapeldreef 75, Heverlee, 3001, Belgium. [3]Institute for Microelectronics (TU Wien), 1040 Vienna, Austria. ✉e-mail: luca.panarella@imec.be

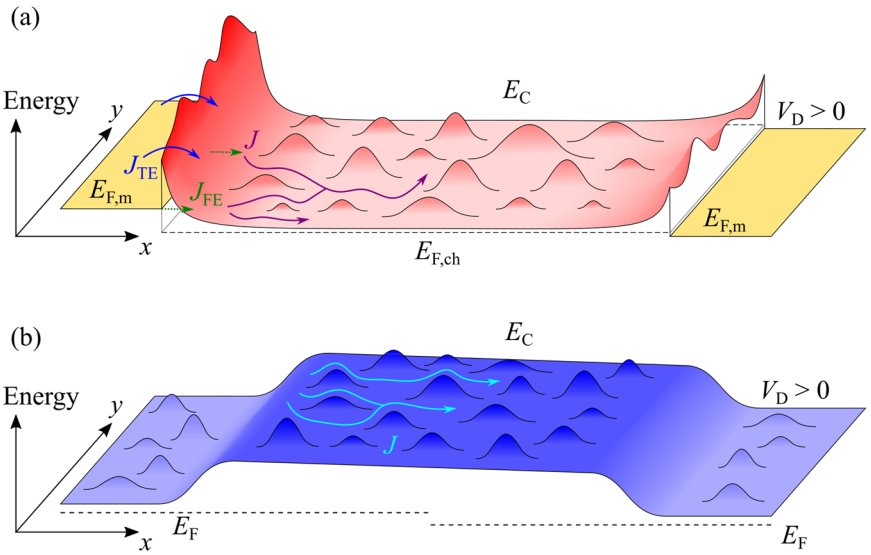

Fig. 1 | Percolative transport: Si vs TMD. **a** Schematic representation of percolative transport through the channel and non-uniform Schottky barriers in 2D FETs with side contacts electrostatically doped by the back gate. J_{TE} and J_{FE} are the thermionic-emission and field-emission components of the total current injected through the Schottky junction. **b** Schematic representation of percolative transport in conventional Si FETs. In this case, the highly doped source and drain do not limit the current.

hetereogeneous in-plane chemical interactions along the contact perimeter[27]. These factors, coupled with the highly non-uniform surface potential of 2D TMDs[31–34], result in the formation of inhomogeneous Schottky contacts[35,36] and individual low-barrier spots through which carriers are primarily injected, leading to non-uniform conduction through the channel (Fig. 1a).

Before we delve into the details of percolative behavior in 2D FETs, it is first useful to highlight some concepts concerning charge traps in silicon-based technologies to better understand the impact of similarly behaving defects on 2D devices. In a typical Si channel FET the effect of single charged defects on the threshold voltage depends on their spatial position with respect to the channel[37]. First, traps close to the source and drain p–n junctions contribute less to the threshold voltage shift than traps located at the center of the channel. Second, individual dopants, fixed charges, surface roughness, and metal granularity result in surface potential fluctuations that can reach tens of meV. Hence, the near-threshold regime channel transport is percolative (Fig. 1b) and the impact of individual defects is further randomized. In particular, a charge trap located in the vicinity of a percolation path will induce large RTN as it suppresses a current-limiting region of the channel. The activity of typical channel-impacting oxide traps is also gate voltage-dependent due to the electrostatic shift of the trap energy level with respect to the channel Fermi level induced by the applied gate bias (V_G)[38]. In general, the capture/emission time constants of defects far from the channel will have a larger V_G dependence than those of defects close to the channel due to the larger V_G leverage effect on the trap energy level.

In TMD-based FETs, charging/discharging traps near the low-barrier spots of the inhomogeneous Schottky contacts are predicted to generate substantial RTN as a result of the local perturbation of the Schottky barrier. Their capture/emission time constants are not only expected to exhibit gate voltage dependence based on their vertical position relative to the channel, but also strong drain voltage dependence, as the lateral potential drop in scaled 2D FET prototypes is larger across the metal/semiconductor junction than along the channel (i.e., contact resistance-limited). Furthermore, the bias conditions of the two side contacts are different, depending on the applied lateral field. If the left contact is grounded and the voltage V_D applied to the right contact is larger than 0 V, the left contact is the reverse-biased source and a charging defect close to a low-barrier spot will strongly affect the device current. In contrast, if $V_D < 0$ V, the left contact is the forward-biased drain and a change in the Schottky barrier height and width induced by a charging/discharging defect in its vicinity no longer affects the device current significantly, as it is limited by the reverse-biased right contact. Therefore, the magnitude of the RTN signal generated by a contact-impacting defect is expected to depend on the polarity of the applied lateral field.

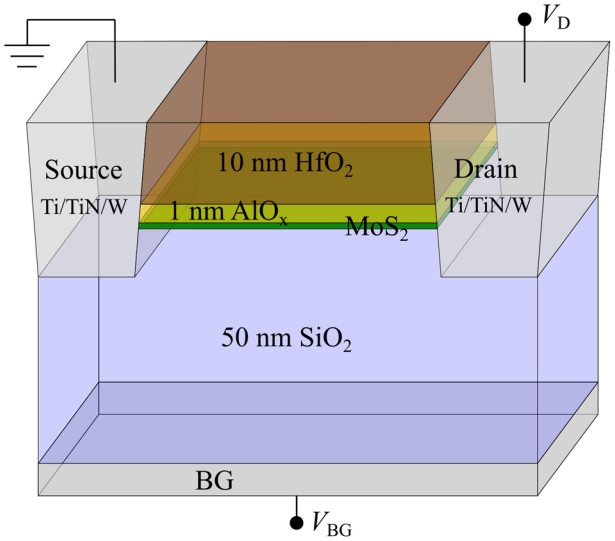

Fig. 2 | Device structure. Schematic structure of a back-gated 300 mm integrated MoS_2 FET with side source and drain contacts.

In this work, we study the detrimental effect of contact-impacting defects on the performance of 300 mm integrated MoS_2 FETs with scaled channel area. A schematic of the device structure is shown in Fig. 2. We show that the presence of charge traps not only affects the transistor threshold voltage as a consequence of the surface potential variation with carrier capture/emission[38], but can also perturb the Schottky barrier when the defect is located in the vicinity of the side source/drain contacts, resulting in large current fluctuations that can reach nearly 40% variation. To do so, we investigate random telegraph noise (RTN) given by two different types of contact-impacting traps. First, we extract their experimental capture/emission time constants as a function of the applied back-gate and drain potentials (V_{BG} and V_D, respectively). Then, we explain their distinct behavior by using a simplified circuit model and TCAD simulations.

The dramatic current changes induced by the observed defects represent evidence of the microscopic inhomogeneities of the source/drain Schottky contacts, resulting in non-uniform currents through the device.

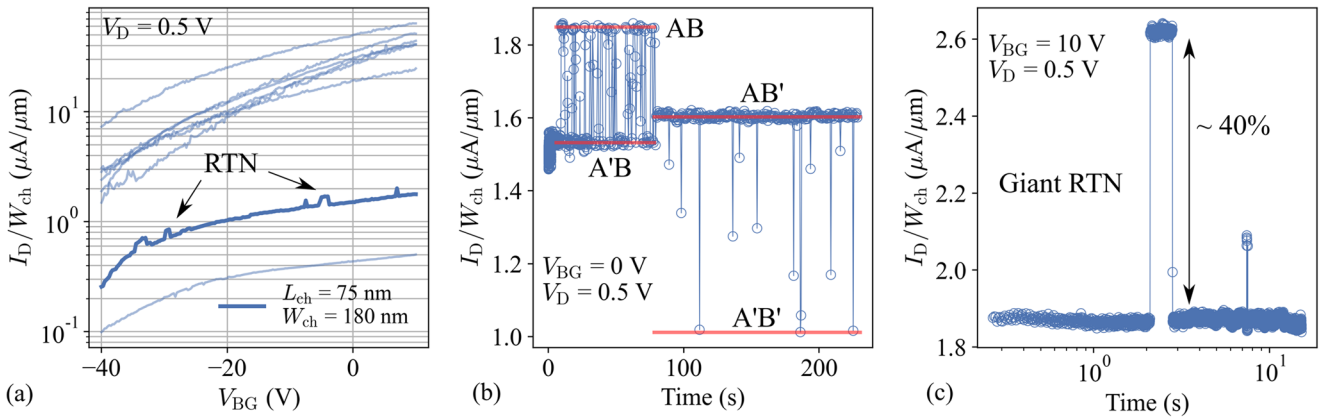

Fig. 3 | Transfer characteristics and RTN. Examples of transfer characteristics (**a**) and RTN traces (**b**, **c**) measured on scaled MoS_2 FETs. Complex interrelated defect activities (**b**) and high current fluctuations (**c**) suggest that the observed traps are located in the vicinity of current-limiting spots of the device system.

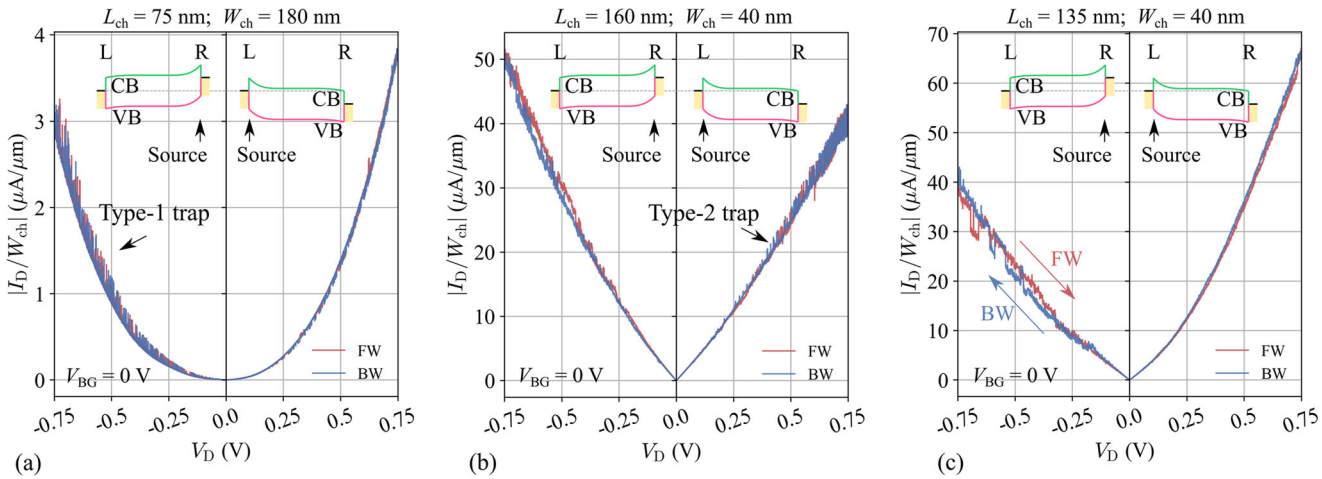

Fig. 4 | Output characteristics and RTN. Slow V_D-rate I_D–V_D curves collected on 3 different devices with L_{ch} = 75 nm and W_{ch} = 180 nm (**a**), L_{ch} = 160 nm and W_{ch} = 40 nm (**b**), and L_{ch} = 135 nm and W_{ch} = 40 nm (**c**). In all cases, distinct RTN features can be observed by switching V_D polarity, which supports the hypothesis about the presence of defects in the vicinity of the source/drain contacts. Insets: schematics of the horizontal channel band diagram for different V_D conditions. When $V_D > 0$ V, the left (L) junction is reverse-biased (source), while the right (R) junction is forward-biased (drain). When $V_D < 0$ V, the bias conditions of the two contacts are swapped.

Their detrimental impact is expected to become even larger as the channel and contact dimensions are further scaled down.

Results

Analysis of RTN

Back-gated FETs with 1–2 monolayers of MoS_2 grown on sapphire (MOCVD), transferred onto 50 nm SiO_2, and capped with 1 nm AlO_x/10 nm HfO_2 insulating stack (Fig. 1) are used in this work[39]. The side contact trenches are filled with Ti/TiN/W forming the source and drain side contacts. Transmission electron microscopy (TEM) images along the length and width of representative MoS_2 devices are included in the Supplementary Information (Supplementary Fig. 1).

Before studying the impact of individual charge traps, we first measure the transfer characteristics of several scaled FETs (channel length—L_{ch}—from 75 nm to 160 nm and channel width—W_{ch}—from 40 nm to 180 nm). All measured devices are affected by strong n-doping leading to poor current modulation (Fig. 3a) and cannot be completely turned off even at $V_{BG} = -40$ V. The reason behind this effect could be the presence of a high concentration of impurities (e.g., carbon) and/or oxygen vacancies in the AlO_x interlayer, which create an electron-rich environment and promote electron transfer to the underlying MoS_2[40,41]. Further details can be found in the Supplementary Information (Supplementary Note 2).

Unlike previously reported works where scaled 2D FETs were investigated at low temperatures to freeze out most defects and isolate only a handful of them[42], we are able to measure RTN by fixing the bias conditions and monitoring the current over time at room temperature. Each device is subjected to a repeated number of measurements (~50) in order to collect a statistically meaningful dataset. Two interesting cases are shown in Fig. 3. In the first RTN trace (Fig. 3b), the interrelated activity of two distinct traps, both controlling the same percolation path, is detected (see Supplementary Note 3 for details)[43–46]. During the first time frame of the measurement, defect B is discharged, while defect A captures and emits electrons repeatedly (A' ↔ A). At t ~ 90 s, defect B captures an electron (B → B'), causing a negative variation of net charge that partially obstructs the carrier flow through the percolation path. The negative net charge of B' also perturbs the energy level of defect A, resulting in a variation of its capture and emission time constants. As a consequence, A (defect discharged) becomes significantly more stable than A' (defect charged), and only a few capture events can be recorded. When both defects are negatively charged (A'B'), transport along the percolation path is substantially hindered and the lowest

current level is measured. Due to the high instability of the device under test, the properties of defects A and B are not investigated further.

In the second trace shown in Fig. 3c, a giant RTN step is observed with nearly 40% current variation, which indicates the presence of a trap near a current-limiting bottleneck of the system. Similar RTN has been already reported by Ravichandran et al., who observed comparably large current steps induced by individual defects in back-gated MoS_2 FETs[42]. Since our scaled devices are contact-limited due to high contact resistance (see Supplementary Fig. 3), the source/drain regions are identified as the most probable candidates for the trap location. As mentioned above, a trap located close to either contact can affect the Schottky barrier due to the local potential perturbation induced by its switching charge state. As a consequence, its impact is expected to be maximized when the affected contact is reverse-biased and thus limits the current. It is important to emphasize that defects next to the contacts are also expected to influence the device threshold voltage, as commonly known for Si-based technologies. However, due to the dominant resistance of the Schottky contacts and the peripheral position of the reported defects[37], the contribution of the threshold voltage shift on the measured RTN is believed to be negligible.

To prove our hypothesis on the defect location, we measure multiple I_D-V_D curves at varying V_{BG} biases using a slow sweep rate (SR = 2.5 mV/s) on 17 highly-scaled devices. Three examples are shown in Fig. 4. First, the large variability of the output characteristics, ranging from nearly linear to strong Schottky behavior across different devices and switching V_D polarity, corroborates our assumption about the inhomogeneity of the side Schottky contacts. Second, in nearly all cases, large current steps are observed and different RTN features are detected when the V_D polarity is switched, suggesting that most impactful defects are located close to an injection spot of the lateral contacts, in agreement with our previous suppositions. Note that the notation V_D is used for the potential applied to the right contact. When V_D is positive, the right contact is the forward-biased drain and the left contact is the reverse-biased source. When V_D is negative, the right contact becomes the reverse-biased carrier source. Within the 17 highly scaled devices, we can distinguish 14 different defects generating large RTN steps depending on the applied V_D polarity. The cumulative distribution function (CDF) of the collected step heights, each one corresponding to a different defect, is calculated for three gate biases and shown in Fig. 5. At $V_{BG} = -30$ V, the resistance of the electrostatically doped side contacts—i.e., source and drain are controlled by the overlapping back gate—significantly increases and, therefore, the effect of contact-impacting traps is larger. In this case, all collected step heights exceed 10% current variation, highlighting the tremendous impact of defects affecting contact properties in scaled 2D FETs.

Two defects, namely the type-1 and type-2 traps (defined in Fig. 4a, b), produce clear and rich RTN traces throughout the entire range of investigated voltages, which make them good candidates for further study. An in-depth analysis of their distinct behavior is reported in the following sections.

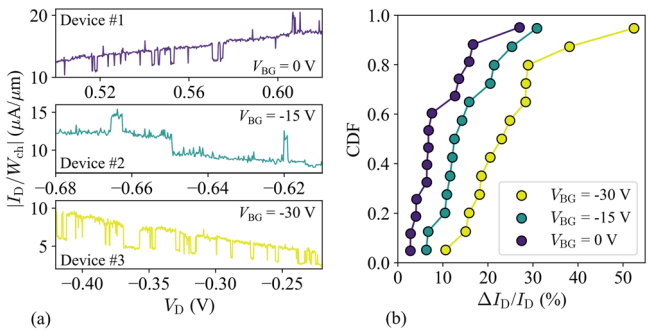

Fig. 5 | RTN step height distribution of contact-impacting defects. a Examples of RTN affecting the output characteristics of three different devices. **b** Cumulative distribution function of the RTN step heights generated by contact-impacting defects. For each i^{th} point of the sorted dataset, the CDF is calculated as $(i - 0.3)/(n + 0.4)$, where n is the total number of collected step heights. Step heights are collected from the slow I_D–V_D curves measured on 17 highly scaled devices. In total, 14 defects are found featuring different impact depending on the V_D polarity.

Type-1 trap

In order to extract the time constants of the type-1 trap, the I_D–V_D curves are divided into V_D intervals of 0.05 V. Then, the drain current is plotted as a function of time. For each slice, a baseline is calculated with an asymmetric least squares smoothing algorithm and subtracted from the data to simplify the step detection (Fig. 6a). Since the investigated 2D FETs are n-type devices operating in accumulation, each capture/emission event involves a trap near the MoS_2 conduction band minimum (CBM), suggesting that the investigated defects are likely acceptor traps. When the defect captures an electron, the net negative charge increases and the channel current drops. Conversely, when the defect releases an electron, the net positive charge increases and the channel current rises. Hence, the corresponding capture and emission times are collected at each negative and positive current step, respectively[37,38].

The time distribution of the capture and emission events is known to be exponential[38]. Thus, the capture and emission time constants, τ_c and τ_e, can be calculated using their maximum likelihood estimator:

$$\langle \tau \rangle = \frac{1}{N} \sum_{i=1}^{N} t_i, \tag{1}$$

where t_i is the time at which the i^{th} capture/emission event occurs. Further details on the extraction of the time constants can be found in the

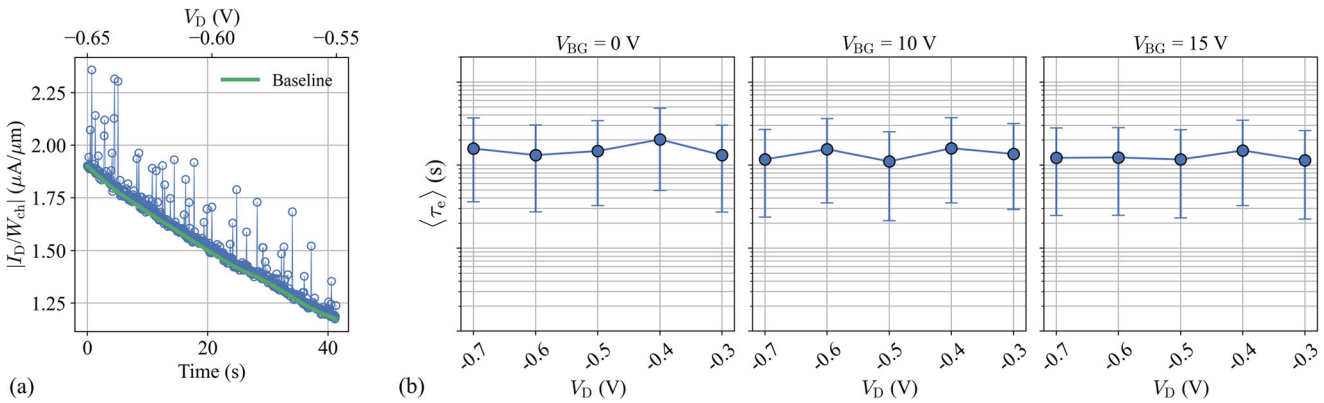

Fig. 6 | Time constants of the type-1 trap. Example of an I_D–V_D slice from Fig. 4a (**a**) and experimental $\langle \tau_e \rangle$ extracted for the type-1 trap (**b**). $\langle \tau_e \rangle$ is constant throughout the entire range of investigated voltages.

Supplementary Information (Supplementary Note 4). $\langle\tau_e\rangle$ of type-1 trap calculated for several bias conditions is shown in Fig. 6b. Interestingly, no dependence on V_{BG} or V_D is observed in this case. The capture times are too short to be resolved by the measurement sampling time and generate emission steps with a single data point and varying height. Therefore, $\langle\tau_c\rangle$ cannot be calculated. Nevertheless, the collected traces suggest that $\langle\tau_c\rangle$ does not depend on the applied voltages either as the average relative height of the emission steps is constant across the entire range of investigated V_{BG} and V_D values. The lack of V_D and V_{BG} dependence indicates that no shift of the trap energy level occurs with respect to the carrier reservoir's Fermi level. For this reason, the type-1 trap is identified as a defect adjacent to the interface of the right metal contact. This hypothesis is, in fact, compatible with both our main experimental findings: (1) large RTN can be observed at negative V_D only, i.e. when the right contact is the reverse-biased source, meaning that the trap is located in its vicinity, and (2) a change in V_D or V_{BG} does not result in a variation of the defect time constants because the trap energy level is pinned by the metal and its position is unchanged with respect to the metal Fermi level. Assumptions on the *vertical* position (bottom oxide, channel or top oxide) of type-1 trap are instead difficult to make as no V_D or V_{BG} dependence can be used to exclude any possibilities. Nevertheless, the trap is expected to be sufficiently close to the channel to have a significant impact on the injected current.

In order to further support our explanation, we develop a simple circuit model to qualitatively reproduce the effect of a change in the Schottky barrier of either contact due to a charging/discharging trap on the output characteristic of a MoS_2 device. A 2D FET in the on-state can be described as two back-to-back Schottky diodes, representing the source and drain contacts, with a resistor in between, mimicking the channel resistance (Fig. 7). Given a certain V_D, the current flowing through the circuit can be calculated by numerically solving the following system of non-linear equations:

$$\left.\begin{aligned} V_D &= V_s + V_{ch} + V_d \\ J &= J_{s_0}\cdot\exp\left(\frac{-qV_s}{n_s k_B T}\right)\cdot\left(\exp\left(\frac{qV_s}{k_B T}\right)-1\right) \\ J &= R_{ch}/\left(V_{ch}\cdot A\right) \\ J &= J_{d_0}\cdot\exp\left(\frac{qV_d}{n_d k_B T}\right)\cdot\left(1-\exp\left(-\frac{qV_d}{k_B T}\right)\right) \\ J_{s_0,d_0} &= A^{*}\,T^{1.5}\exp\left(-\frac{q\Phi_{s,d}}{k_B T}\right), \end{aligned}\right\} \quad (2)$$

with V_s, V_{ch}, V_d being the potential drop across the source junction, the channel, and the drain junction, respectively, R_{ch} the channel resistance, A the cross-sectional area of the channel (same as the contact area), $n_{s,d}$ the ideality factors of the Schottky contacts, $\Phi_{s,d}$ the Schottky barrier heights, T the temperature, k_B the Boltzmann constant, and A^* the Richardson constant. Two important simplifications must be mentioned here. First, electrostatically doped contacts are employed in our devices. Hence, the Schottky barriers are strongly dependent on the applied gate bias. However, since we only use this model for a *qualitative* description of the output characteristics collected at fixed gate bias, this dependence is not included in the Schottky diode equations. Second, the electrostatic perturbation introduced by a charged point defect is expected to locally affect both the *height* and the *width* of the inhomogeneous Schottky barrier. However, due to its overall complexity, this interaction is only treated as an effective variation of the Schottky barrier height, which is considered to be uniform along the contact perimeter.

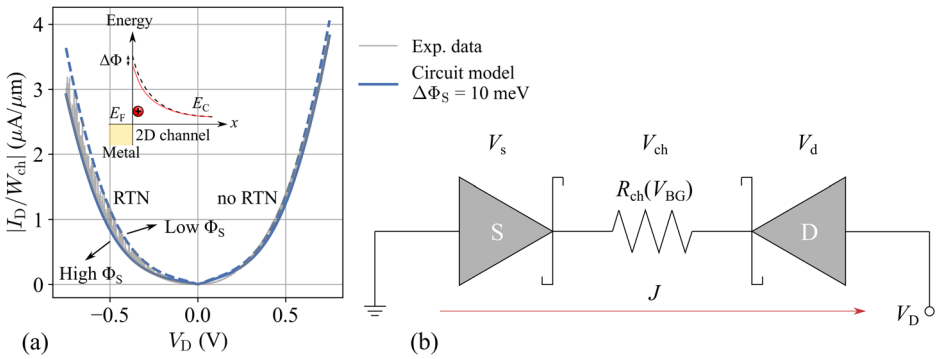

Fig. 7 | Circuit model. a Plot of the output characteristics affected by the type-1 trap. **b** circuit model used to fit the experimental data. A small change in the source Schottky barrier height correctly describes the V_D polarity-dependent RTN.

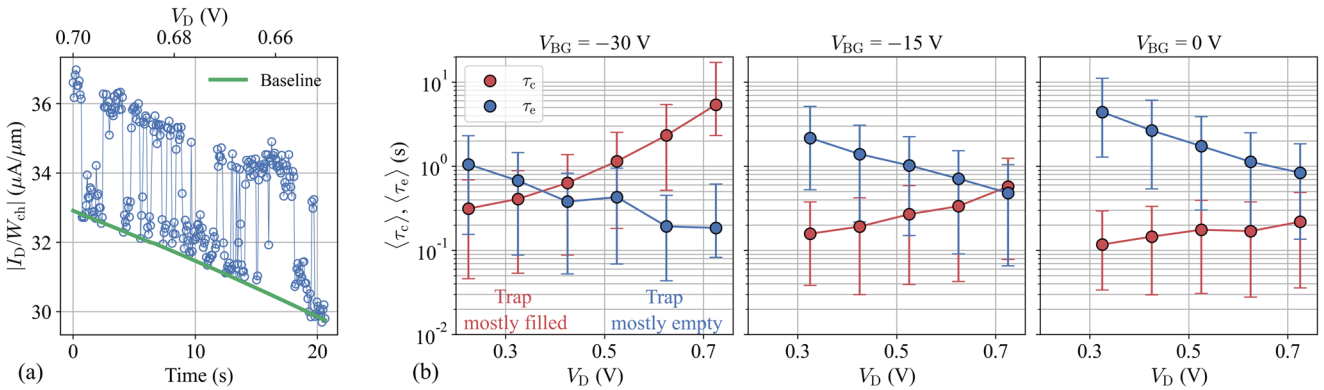

Fig. 8 | Time constants of the type-2 trap. Example of an I_D–V_D slice from Fig. 4b (**a**) and experimental $\langle\tau_c\rangle$ and $\langle\tau_e\rangle$ extracted for the type-2 trap (**b**). Both time constants depend on V_{BG} and V_D.

A plot of the experimental and modeled I_D–V_D curves is shown in Fig. 7. By changing the height of the source Schottky barrier Φ_S by 10 meV it is possible to accurately emulate the height of the RTN steps observed for negative V_D. In this case, the V_D-biased contact is the source and a charged trap located in the vicinity of a low barrier spot has a very strong impact on the device current. On the contrary, when a positive V_D is applied, the bias conditions of the two contacts are swapped and the same defect no longer affects the current significantly. The simple circuit model is able to correctly describe this feature as well, in agreement with the experimental data.

Because of its proximity to the side contact, type-1 trap could be argued to also enhance carrier injection by trap-assisted tunneling. However, this would require the defect to be located right next to the metal/MoS_2 interface, which is necessary to have sufficiently high trap-to-channel tunneling probability. In addition, it should also exhibit complex behavior featuring additional states with very fast transition rates in order to significantly contribute to the drain current ($I_D \sim 0.1\ \mu$A, hence τ_c and $\tau_e \sim 10^{-12}$ s)[47]. For these reasons, we believe that type-1 trap unlikely provides an efficient path for tunneling.

Further speculations on the nature of the type-1 trap are difficult to make as no information about its energy level and vertical position can be retrieved. Nevertheless, it is logical to assume that it may be generated by reactive ion etching used during side contact processing, as it is found to be adjacent to the source interface. Such traps could be cured using combinations of post deposition and post metal annealings, which are known to significantly reduce defect density in a wide variety of device architectures and gate stacks[48–50].

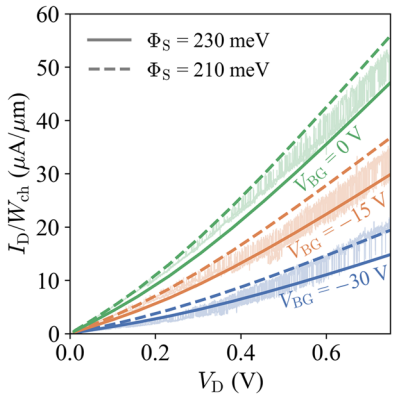

Fig. 9 | TCAD model calibration. Output characteristics of the MoS_2 device affected by the type-2 trap. The calibrated TCAD model provides a good description of the experimental data. A change of 20 meV in the source Schottky barrier height correctly reproduces the RTN step height for all bias conditions.

Type-2 trap

The same time constant estimation method described above is applied to the type-2 trap as well (Fig. 8). In this case, the capture time constant increases with V_D and decreases with V_{BG}, while the emission time constant exhibits the opposite trend. A first clue as to the location of this trap is the weak dependence on V_{BG}. Indeed, a ΔV_{BG} of 30 V results in a capture/emission time constant variation of about one order of magnitude only. A rough estimation of the distance y of a defect in the bottom gate oxide from the channel is given by the following equation[42]:

$$\frac{y}{t_{ox}} = -\frac{k_B T}{q}\frac{\delta(\langle\tau_c\rangle/\langle\tau_e\rangle)}{\delta V_{BG}}, \tag{3}$$

where t_{ox} is the gate oxide thickness. In our case, $y \simeq 0.2$ nm, suggesting that the vertical field has poor leveraging effect on the trap energy level. Therefore, the type-2 trap is likely an interface/channel defect or a defect in the top oxide, where the electric field generated by the bottom gate is screened by the charge carriers in the channel.

In order to obtain more detailed information on the behavior of the type-2 trap, we resort to the use of a TCAD model[51] to describe the electrostatic shift of its energy level E_T induced by the applied fields. The model is calibrated to fit the output characteristics of the device at $V_{BG} = -30$, −15, and 0 V (Fig. 9) using the same parameter set (see Supplementary Note 5 for details). Similar to the circuit model shown in Section "Type-1 trap", the V_D- and V_{BG}-dependent amplitude of the RTN signal can be accurately reproduced by varying the source Schottky barrier height Φ_S by 20 meV. Hence, also this type-2 trap is likely located close to the source contact (reverse-biased) and affects its barrier upon charging/discharging.

To shed further light on the precise spatial and energy position of the type-2 trap, we follow with the analysis of the energy shift of a defect placed in different spots of the device induced by either a gate or drain voltage change. The ratio of the capture and emission time constants depends exponentially on the difference between the trap energy level and the Fermi level of the carrier reservoir (e.g., the 2D channel):

$$\frac{\langle\tau_c\rangle}{\langle\tau_e\rangle} = \exp\left(\frac{E_T - E_F}{k_B T}\right). \tag{4}$$

Hence, the trap energy position can be estimated using the experimental time constants shown in Fig. 8. By choosing $V_{BG} = -30$ V and $V_D = 0.725$ V

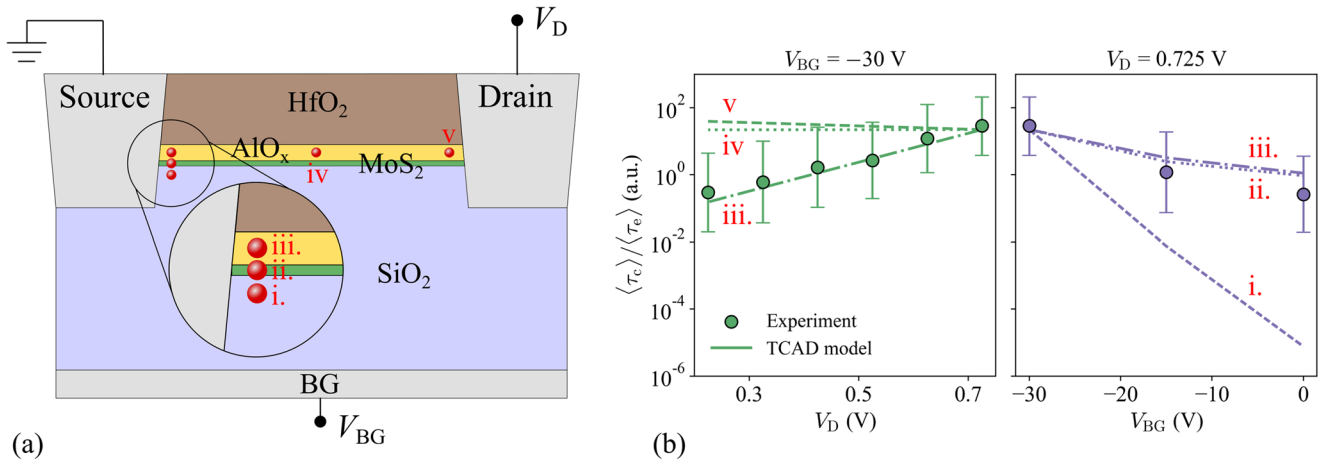

Fig. 10 | Extraction of the type-2 trap position. a Device schematic with several possible positions of the type-2 trap. **b** Bias-dependent time constant ratio of the type-2 trap fitted with the calibrated TCAD model. The best fit is obtained using a trap located ~4.5 nm from the source, ~0.5 nm above the channel (location iii), and ~20 meV below the conduction band minimum of MoS_2.

as the starting condition, E_T is found to be located ~20 meV below the conduction band minimum of MoS_2. Once the initial energy position of the type-2 trap is determined, we use the calibrated TCAD model to re-calculate $E_T - E_F$ as a result of the electrostatic shift induced by either a drain or gate bias variation. Then, Equation (4) can be used to estimate $\langle\tau_c\rangle/\langle\tau_e\rangle$ at each V_{BG} and V_D condition. We repeat this procedure for 5 possible locations of the trap in the device (Fig. 10a):

i. 4.5 nm from the source and 0.5 nm from the channel in the bottom oxide.
ii. 4.5 nm from the source and in the channel.
iii. 4.5 nm from the source and 0.5 nm from the channel in the top oxide.
iv. 80 nm from the source and 0.5 nm from the channel in the top oxide.
v. 4.5 nm from the drain and 0.5 nm from the channel in the top oxide.

Plots of the experimental and simulated $\langle\tau_c\rangle/\langle\tau_e\rangle(V_D, V_{BG})$ are shown in Fig. 10b. A defect located in the bottom oxide is expected to exhibit a much stronger dependence on V_{BG}, as most of the electric field variation following a back-gate bias change occurs in the bottom gate stack due to the screening effect of the charge carriers in the channel. Therefore, this defect location can be excluded. Similarly, a defect distant from both side contacts or close to the drain metal is expected to show no dependence (same as typical channel-impacting defects in Si FETs) or opposite dependence on V_D, respectively, and cannot describe the experimental data. Hence, only two options remain: the defect is located next to the source and in the channel (location ii) or next to the source and in the top oxide (location iii). Both cases are able to provide a good description of the V_D- and V_{BG}-dependent $\langle\tau_c\rangle/\langle\tau_e\rangle$.

The TCAD-calculated band diagrams in Fig. 11 help to understand the V_D- and V_{BG}-dependent behavior of both types of contact-impacting traps. The trap energy levels projected onto the plane defined by a horizontal cut through the middle of the channel are shown for three different bias conditions. $E_{T,1}$ is the energy level of a defect at the interface with the source contact (similar to the case of the type-1 trap). This trap can likely exchange carriers with the adjacent metal and the position of its energy level with respect to the metal Fermi level remains unvaried upon any V_{BG} or V_D change. $E_{T,2}$ is the energy level of a defect located in the top AlO_x interlayer, 0.5 nm above the channel, and 4.5 nm from the source contact (location iii). Hence, it likely exchanges carriers with the channel due to the narrower tunneling barrier. When V_D is increased, $E_{T,2}$ is pushed upwards, the probability of capturing an electron decreases (longer $\langle\tau_c\rangle$), and the probability of emitting an electron increases (shorter $\langle\tau_e\rangle$). On the contrary, when V_{BG} is increased, $E_{T,2}$ is pushed downwards and the opposite trend of $\langle\tau_c\rangle/\langle\tau_e\rangle$ is observed. Similar *average* V_{BG} and V_D dependence is expected in large devices for a large number of such defects forming bands.

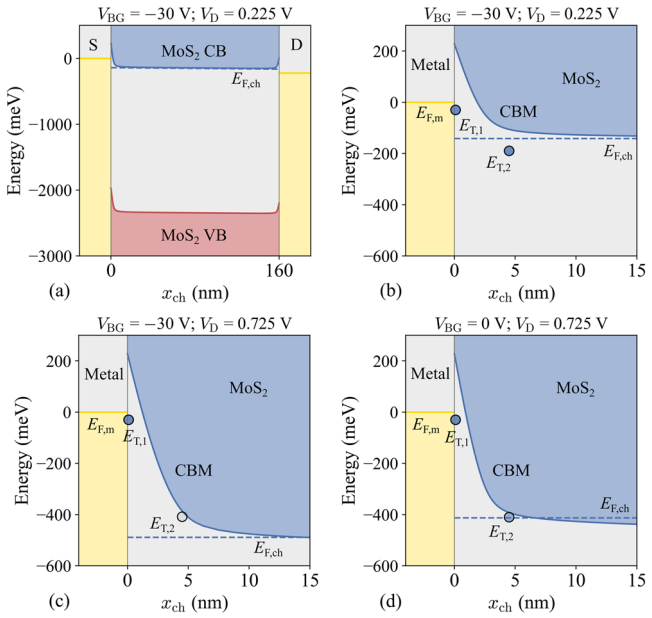

Fig. 11 | TCAD-calculated band diagrams at different bias conditions. a Full band diagram at $V_{BG} = -30$ V and $V_D = 0.225$ V. **b** Zoomed band diagram at $V_{BG} = -30$ V and $V_D = 0.225$ V. **c** Zoomed band diagram at $V_{BG} = -30$ V and $V_D = 0.725$ V. **d** Zoomed biand diagram at $V_{BG} = 0$ V and $V_D = 0.725$ V. $E_{T,1}$ is the energy level of a type-1 trap communicating with the source contact metal. Hence, a V_D or V_{BG} change does not shift the trap energy level with respect to the metal Fermi level $E_{F,m}$. $E_{T,2}$ is the energy level of a type-2 trap in the top oxide (position iii in Fig. 10a) located ~20 meV below the MoS_2 CBM and communicating with the channel. A variation of either applied bias (V_{BG} or V_D) shifts $E_{T,2}$ with respect to the channel Fermi level $E_{F,ch}$.

E_T extracted for the type-2 trap (~20 meV below MoS_2 CBM) is compatible with the defect levels of an oxygen vacancy or an interstitial aluminum in Al_2O_3[52]. In addition to this, several cases of charge trapping associated to AlO_x defects in TMD-based FETs have been reported in the literature[42,53]. The combination of these findings with the good agreement between experimental and modeling results obtained for the V_{BG}- and V_D-dependent $\langle\tau_c\rangle/\langle\tau_e\rangle$ suggest that the type-2 trap is probably a defect in the top AlO_x interlayer.

With future advances in the development of a 2D technology, the achievement of low-resistance ohmic contacts will drastically reduce the effect of contact-impacting defects (both type-1 and type-2) as the source will no longer be a current-limiting element of the device system. Nevertheless, similar traps will still be relevant as they are expected to be present along the entire longitudinal extension of the device (type-2 defect is indeed identified as a AlO_x defect) and will possibly affect transport along the channel, similarly to the Si case shown in Fig. 2b. In order to mitigate their detrimental effect, a two-fold action is required. First, improvement of the device processing and optimization of the dielectric stack, including the use of novel low-defect density materials[54–56], are needed to reduce the number of active traps. Second, the implementation of special dipole layers could enable efficient misalignment of the trap energy levels with respect to the channel Fermi level and significantly reduce charge trapping[57–59].

Discussion

Inhomogeneities of the 2D channel in TMD-based FETs, along with etch-induced damage during contact fabrication, result in the formation of side contacts exhibiting non-uniform Schottky barriers. To support this picture, we investigated the atypical V_D- and V_{BG}-dependent electron-trapping behavior of single defects in MoS_2 FETs integrated on 300 mm wafers. In particular, we were able to identify two distinct types of contact-impacting traps:

- the type-1 trap is a defect adjacent to the source interface exchanging carriers with the contact metal. Hence, its capture/emission time constants do not depend on the applied voltages and the RTN signal is observed at $V_D < 0$ V only, when the right contact is the reverse-biased source.
- the type-2 trap is a defect located in the top AlO_x interlayer, ~0.5 nm above the channel, and ~4.5 nm from the source (left contact in this case). It exhibits both a V_D- and V_{BG}-dependent RTN due to the electrostatic shift of its energy level with respect to the channel Fermi level induced by the applied biases.Both types of defects affect the Schottky barrier height and width rather than the threshold voltage and generate large RTN that can reach nearly 40% of current variation. Such a dramatic impact on the device current can be only explained by considering the presence of a limited number of low Schottky barrier spots through which carriers are predominantly injected, resulting in non-uniform conduction through the channel.

Our results highlight the urgency of finding suitable materials and processes to achieve ohmic source/drain contacts with low resistance, reduced defect density in the gate dielectrics, and uniform 2D channels, as the impact of traps located in the vicinity of the lateral contacts is expected to significantly grow by further scaling down the device size.

Methods

Device fabrication

All devices are fabricated entirely in a 300 mm pilot line[60,61]. The MoS_2 channel (1-2 monolayers) is grown by MOCVD on sapphire and then transferred onto the back gate stack (50 nm SiO_2/p+ Si). Next, it is capped using AlO_x interlayer (trimethylaluminum soak followed by oxidation), which enables subsequent deposition of 10 nm HfO_2 by atomic layer deposition (ALD). Finally, after active patterning, side contact trenches are etched through HfO_2, AlO_x, MoS_2 and ~5 nm into SiO_2 using BCl_3/Cl_2 plasma and subsequently filled with Ti (highly directional PVD), TiN (ALD), and W (CVD).

Electrical characterization and simulations

Scaled devices with varying channel length L_{ch} and channel width W_{ch} (L_{ch} from 75 nm to 135 nm; W_{ch} from 40 nm to 180 nm) are investigated in this work. The electrical performance of large area devices[39] is shown in the Supplementary Information (Supplementary Fig. 2). Electrical measurements are performed in an ambient environment at room temperature using a Süss PA300 probe station equipped with two Keithley 2636B sourcemeters. Each experiment is controlled over GPIB from a PC using a framework of Perl subroutines. TCAD simulations are performed with Synopsys Sentaurus Device.

Data availability

The data that support the findings of this work are available from the corresponding authors upon reasonable request.

Received: 29 February 2024; Accepted: 27 June 2024;
Published online: 14 July 2024

References

1. Chhowalla, M., Jena, D. & Zhang, H. Two-dimensional semiconductors for transistors. *Nat. Rev. Mater.***1**, 16052 (2016).
2. Akinwande, D. et al. Graphene and two-dimensional materials for silicon technology. *Nature* **573**, 507–518 (2019).
3. Ahmed, Z. et al. Introducing 2D-FETs in device scaling roadmap using DTCO. In: *2020 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2020). https://doi.org/10.1109/iedm13553.2020.9371906.
4. Das, S. et al. Transistors based on two-dimensional materials for future integrated circuits. *Nat. Electron.* **4**, 786–799 (2021).
5. Illarionov, Y. Y. & Grasser, T. Reliability of 2D field-effect transistors: from first prototypes to scalable devices. In: *2019 IEEE 26th International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA)*, 1–6 (IEEE, 2019).
6. Lanza, M., Smets, Q., Huyghebaert, C. & Li, L.-J. Yield, variability, reliability, and stability of two-dimensional materials based solid-state electronic devices. *Nat. Commun.***11** (2020). https://doi.org/10.1038/s41467-020-19053-9.
7. Cho, K. et al. Electric stress-induced threshold voltage instability of multilayer MoS_2 field effect transistors. *ACS Nano* **7**, 7751–7758 (2013).
8. Illarionov, Y. Y. et al. The role of charge trapping in MoS_2/SiO_2 and MoS_2/hBN field-effect transistors. *2D Mater.* **3**, 035004 (2016).
9. Yuan, H.-W. et al. PBTI investigation of MoS_2 n-MOSFET with Al_2O_3 gate dielectric. *IEEE Electron Device Lett.* **38**, 677–680 (2017).
10. Illarionov, Y. Y. et al. Energetic mapping of oxide traps in MoS_2 field-effect transistors. *2D Mater.* **4**, 025108 (2017).
11. Stampfer, B. et al. Characterization of single defects in ultrascaled MoS_2 field-effect transistors. *ACS Nano* **12**, 5368–5375 (2018).
12. Panarella, L. et al. Analysis of BTI in 300 mm integrated dual-gate WS_2 FETs. In: *2022 Device Research Conference (DRC)* 1–2 (IEEE, 2022).
13. Allain, A., Kang, J., Banerjee, K. & Kis, A. Electrical contacts to two-dimensional semiconductors. *Nat. Mater.* **14**, 1195–1205 (2015).
14. Schulman, D. S., Arnold, A. J. & Das, S. Contact engineering for 2D materials and devices. *Chem. Soc. Rev.* **47**, 3037–3058 (2018).
15. Liu, X., Choi, M. S., Hwang, E., Yoo, W. J. & Sun, J. Fermi level pinning dependent 2D semiconductor devices: Challenges and prospects. *Adv. Mater.* **34**, e2108425 (2022).
16. Zheng, Y., Gao, J., Han, C. & Chen, W. Ohmic contact engineering for two-dimensional materials. *Cell Rep. Phys. Sci.* **2**, 100298 (2021).
17. Kang, J., Liu, W., Sarkar, D., Jena, D. & Banerjee, K. Computational study of metal contacts to monolayer transition-metal dichalcogenide semiconductors. *Phys. Rev. X.* **4**, 031005 (2014).
18. Li, W. et al. Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **613**, 274–279 (2023).
19. Jiang, J., Xu, L., Qiu, C. & Peng, L.-M. Ballistic two-dimensional InSe transistors. *Nature* **616**, 470–475 (2023).
20. Cheng, Z. et al. Immunity to contact scaling in MoS_2 transistors using in situ edge contacts. *Nano Lett.* **19**, 5077–5085 (2019).
21. Chung, Y.-Y. et al. First demonstration of GAA monolayer-MoS_2 nanosheet nFET with 410 μa μm id 1v vd at 40nm gate length. In: *2022 International Electron Devices Meeting (IEDM)*, 34.5.1–34.5.4 (IEEE, 2022).
22. Dorow, C. J. et al. Gate length scaling beyond Si: Mono-layer 2D channel fets robust to short channel effects. In: *2022 International Electron Devices Meeting (IEDM)*, 7.5.1–7.5.4 (IEEE, 2022).
23. Schram, T., Sutar, S., Radu, I. & Asselberghs, I. Challenges of wafer-scale integration of 2D semiconductors for high performance transistor circuits. *Adv. Mater.* **34**, e2109796 (2022).
24. Ahmed, Z. et al. Introducing 2D-FETs in device scaling roadmap using dtco. In: *2020 IEEE International Electron Devices Meeting (IEDM)*, 22.5.1–22.5.4 (IEEE, 2020).
25. Yang, Z. et al. A fermi-level-pinning-free 1D electrical contact at the intrinsic 2D MoS_2/metal junction. *Adv. Mater.* **31**, e1808231 (2019).
26. Liao, W. et al. Interface engineering of two-dimensional transition metal dichalcogenides towards next-generation electronic devices: recent advances and challenges. *Nanoscale Horiz.* **5**, 787–807 (2020).
27. Choi, M. S. et al. Recent progress in 1D contacts for 2D-material-based devices. *Adv. Mater.* **34**, e2202408 (2022).
28. Shen, P.-C. et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
29. Wang, Y. & Chhowalla, M. Making clean electrical contacts on 2D transition metal dichalcogenides. *Nat. Rev. Phys.* **4**, 101–112 (2021).
30. Oberoi, A. et al. Toward high-performance p-type two-dimensional field effect transistors: contact engineering, scaling, and doping. *ACS Nano* **17**, 19709–19723 (2023).
31. Addou, R. et al. Impurities and electronic property variations of natural MoS_2 crystal surfaces. *ACS Nano* **9**, 9124–9133 (2015).
32. Kaushik, V., Varandani, D. & Mehta, B. R. Nanoscale mapping of layer-dependent surface potential and junction properties of CVD-grown MoS_2 domains. *J. Phys. Chem. C* **119**, 20136–20142 (2015).
33. Rhodes, D., Chae, S. H., Ribeiro-Palau, R. & Hone, J. Disorder in van der Waals heterostructures of 2D materials. *Nat. Mater.* **18**, 541–549 (2019).
34. Moore, D. et al. Uncovering topographically hidden features in 2D $MoSe_2$ with correlated potential and optical nanoprobes. *npj 2D mater. appl.* **4**, 44 (2020).
35. Giannazzo, F., Fisichella, G., Piazza, A., Agnello, S. & Roccaforte, F. Nanoscale inhomogeneity of the Schottky barrier and resistivity in MoS_2 multilayers. *Phys. Rev. B* **92**, 081307(R) (2015).
36. Moon, B. H. et al. Junction-structure-dependent schottky barrier inhomogeneity and device ideality of monolayer MoS_2 field-effect transistors. *ACS Appl. Mater. Interfaces* **9**, 11240–11246 (2017).
37. Kaczer, B. et al. A brief overview of gate oxide defect properties and their relation to MOSFET instabilities and device and circuit time-dependent variability. *Microelectron. Reliab.* **81**, 186–194 (2018).
38. Grasser, T. Stochastic charge trapping in oxides: from random telegraph noise to bias temperature instabilities. *Microelectron. Reliab.* **52**, 39–70 (2012).

39. Ghosh, S. et al. Integration of epitaxial monolayer MX_2 channels on 300 mm wafers via collective-die-to-wafer (COD2W) transfer. In: *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* 1–2 (IEEE, 2023).
40. Leonhardt, A. et al. Material-selective doping of 2D TMDC through Al_xO_y encapsulation. *ACS Appl. Mater. Interfaces* **11**, 42697–42707 (2019).
41. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High current density in monolayer MoS_2 doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).
42. Ravichandran, H. et al. Observation of rich defect dynamics in monolayer MoS_2. *ACS Nano* **17**, 14449-14460 (2023). https://doi.org/10.1021/acsnano.2c12900.
43. Zhang, Z. et al. New insights into the amplitude of random telegraph noise in nanoscale MOS devices. In: *2017 IEEE International Reliability Physics Symposium (IRPS)*, 3C–3.1–3C–3.5 (IEEE, 2017).
44. Becker, T. et al. An electrical model for trap coupling effects on random telegraph noise. *IEEE Electron Device Lett.* **41**, 1596–1599 (2020).
45. Vecchi, S., Pavan, P. & Puglisi, F. M. The impact of electrostatic interactions between defects on the characteristics of random telegraph noise. *IEEE Trans. Electron Devices* **69**, 6991–6998 (2022).
46. Vecchi, S., Pavan, P. & Puglisi, F. M. Local electric field perturbations due to trapping mechanisms at defects: what random telegraph noise reveals. *J. Appl. Phys*.**133**, 114101 (2023).
47. Kaczer, B., Toledano-Luque, M., Goes, W., Grasser, T. & Groeseneken, G. Gate current random telegraph noise and single defect conduction. *Microelectron. Eng.* **109**, 123–125 (2013).
48. Franco, J. et al. Demonstration of an InGaAs gate stack with sufficient PBTI reliability by thermal budget optimization, nitridation, high-k material choice, and interface dipole. In: *2016 IEEE Symposium on VLSI Technology* 1–2 (IEEE, 2016).
49. Franco, J. et al. BTI reliability improvement strategies in low thermal budget gate stacks for 3D sequential integration. In: *2018 IEEE International Electron Devices Meeting (IEDM)*, 34.2.1–34.2.4 (IEEE, 2018).
50. Franco, J. et al. On the impact of the gate work-function metal on the charge trapping component of NBTI and PBTI. *IEEE Trans. Device Mater. Rel*. **19**, 268–274 (2019).
51. Verreck, D. et al. The role of nonidealities in the scaling of MoS_2 FETs. *IEEE Trans. Electron Devices* **65**, 4635–4640 (2018).
52. Dicks, O. A., Cottom, J., Shluger, A. L. & Afanas'ev, V. V. The origin of negative charging in amorphous Al_2O_3 films: the role of native defects. *Nanotechnology* **30**, 205201 (2019).
53. Panarella, L. et al. Impact of gate stack processing on the hysteresis of 300 mm integrated WS_2 FETs. In: *2023 IEEE International Reliability Physics Symposium (IRPS)*, 1–6 (IEEE, 2023).
54. Illarionov, Y. Y. et al. Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors. *Nat. Electron.* **2**, 230–235 (2019).
55. Yang, A. J. et al. Van der waals integration of high-k perovskite oxides and two-dimensional semiconductors. *Nat. Electron.* **5**, 233–240 (2022).
56. Davoudi, M. R. et al. Multi-scale modeling of transistors based on the 2D semiconductor Bi_2O_2Se. In: *2023 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 49–52 (IEEE, 2023).
57. Arimura, H. et al. Ge nFET with high electron mobility and superior PBTI reliability enabled by monolayer-Si surface passivation and La-induced interface dipole formation. In: *2015 IEEE International Electron Devices Meeting (IEDM)*, 21.6.1–21.6.4 (IEEE, 2015).
58. Arimura, H. et al. Performance and electrostatic improvement by high-pressure anneal on Si-passivated strained Ge pFinFET and gate all around devices with superior nbti reliability. In: *2017 Symposium on VLSI Technology*, T196–T197 (IEEE, 2017).
59. Lan, H.-Y., Oleshko, V. P., Davydov, A. V., Appenzeller, J. & Chen, Z. Dielectric interface engineering for high-performance monolayer MoS_2 transistors via TaO_x interfacial layer. *IEEE Trans. Electron Devices* **70**, 2067–2074 (2023).
60. Asselberghs, I. et al. Wafer-scale integration of double gated WS_2-transistors in 300mm Si CMOS fab. In: *2020 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2020). https://doi.org/10.1109/iedm13553.2020.9371926.
61. Schram, T. et al. High yield and process uniformity for 300 mm integrated WS_2 FETs. In: *2021 Symposium on VLSI Technology* 1–2 (IEEE, 2021).

Acknowledgements

This work was done in the imec IIAP core CMOS programs and supported by The Research Foundation—Flanders (FWO grant number: 1S72623N). Fundings were received from the European Union's Horizon 2020 research and innovation programme under grant agreement 952792 (2D-EPL).

Author contributions

L.P. performed the measurements of RTN, the modeling, and wrote the manuscript. B.K., Q.S., and V.A. supervised the research. Q.S., T.S., C.L.R., and G.S.K. contributed to the development of imec 300 mm FAB process. D.V., S.T., T.K., and T.G. contributed to the development of the TCAD model. P.S.C., A.V., and D.L. contributed to the data processing and analysis. All authors discussed the results and contributed to the preparation of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41699-024-00482-9.

Correspondence and requests for materials should be addressed to Luca Panarella.