A 160 Gb/s PAM-4 optical receiver using a fully differential transimpedance amplifier in SiGe BiCMOS

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***Abstract*—This paper presents a 160 Gb/s four-level pulse-amplitude modulation (PAM-4) optical receiver based on a 130nm SiGe BiCMOS ($f_T/f_{MAX} = 350/450$ GHz) fully differential transimpedance amplifier (TIA) and two silicon photonic Ge photodiodes (PDs). The high-speed path of the TIA consists of a TIA input stage (TIS) followed by two variable gain amplifiers (VGAs) and an output buffer. A novel fully differential input DC current cancellation (IDCC) circuit is proposed to absorb the input DC currents and eliminate the DC offset of the TIS. 80 GBd PAM-4 operation is demonstrated with an off-line 5-tap feed-forward equalizer (FFE), achieving -7 dBm in-waveguide optical modulation amplitude (OMA) sensitivity at KP4-FEC (2.4×10^{-4}) and 0.99 pJ/b power consumption. 56, 64, and 72 GBd PAM-4 operations are demonstrated without any equalization, achieving -9.2, -8.4, and -5.9 dBm OMA sensitivity at KP4-FEC, respectively. To the best of our knowledge, this integrated optical receiver achieves the best sensitivity at KP4-FEC and the lowest power consumption for 64, 72 and 80 GBd PAM-4 operations.**

***Index Terms*—optical receiver, PAM-4, transimpedance amplifier (TIA), silicon photonic, photodiode (PD), SiGe BiCMOS.**

I. Introduction

THE rapid development of artificial intelligence models, cloud computing and 5G communications has continuously driven the demand for data computing and transmission capacity for intra-data center links. In intra-data center communication systems, optical transceivers serve as crucial components for their high bandwidth capacity and energy efficiency. Intensity modulation-direct detection (IMDD) is a choice for optical transceivers in short-reach applications, due to low complexity and low power consumption [1]. Compared with NRZ modulation [2], [3], PAM-4 achieves twice the spectral efficiency for each symbol carrying two bits [4], [5]. 53 GBd PAM-4 technologies are used in 400G optical transceivers, and higher data rate transceivers are in development to build emerging 800 Gb/s and 1.6 Tb/s optical transceivers [6]. The design of >53 GBd PAM-4 transceivers is particularly challenging due to the requirement for high bandwidth, low noise, and low power consumption.

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In optical receivers, TIAs are used to convert the current signals generated by PDs into voltage signals. Most of the high-speed TIAs utilize a shunt-feedback structure as the input stage for low noise and high bandwidth. Several ∼53 GBd PAM-4 optical receivers have been reported in CMOS process [7]–[13] and SiGe BiCMOS process [14], [15]. However, only a limited number of >64 GBd PAM-4 optical receivers have been reported [16]–[18]. In [16], a 64 GBd optical receiver has been reported with simulation results based on electrical measurement results and a PD model, however, lacking optical measurement results. Ref. [17] demonstrates an 80 GBd optical receiver using a commercial TIA, while a complicated 51-tap FFE is needed to compensate the loss at high frequency. In [18], a 100 GBd optical receiver has been reported based on a traveling wave amplifier, requiring a relatively high 2.5 pJ/b power consumption.

In this work, we present a 160 Gb/s PAM-4 optical receiver using a fully differential TIA in 130 nm SiGe BiCMOS wirebonded to a photonic IC with two Ge PDs. A shunt feedback structure is employed as the TIS, followed by two digitally programmable VGAs and an output buffer. The optical receiver achieves 80 GBd PAM-4 operation with a short off-line 5-tap FFE, which is sufficient to compensate the receiver for opening the eye diagram. The optical receiver also demonstrates 56, 64, and 72 GBd PAM-4 operation without any equalization. Based on the optical measurement results, the bit error ratio (BER) of the optical receiver has been analyzed.

This paper is organized as follows. Section II describes the optical receiver architecture. Section III discusses the details of TIA circuit design. The measurement setup is discussed in section IV, followed by the measurement results and a comparison with the state-of-the-art in section V. Finally, section VI concludes the paper.

II. Optical receiver architecture

Fig. 1 illustrates the simplified block diagram of the optical receiver, which comprises a fully differential TIA and two PDs. The high-speed path of the TIA consists of a fully differential TIS, two VGA stages, and one output buffer stage. The fully differential TIS utilizes a classic shunt feedback structure to achieve both low noise and high bandwidth. The voltage signals converted from current signals by the TIS are amplified by two digitally programmable VGAs. A buffer with

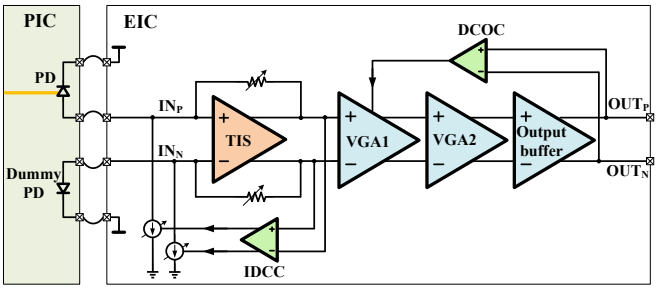

Fig. 1. Simplified block diagram of the optical receiver.

50 ohm output impedance is used to transfer the differential signal off-chip. The IDCC not only absorbs the DC currents from the PDs, but also removes the DC offset of the TIS. A DC offset cancellation (DCOC) circuit is used to eliminate the unintentional DC offsets accumulated in the two VGAs and the output buffer. The TIA circuit is powered by a 2.5 V supply voltage.

The silicon photonic integrated circuit (PIC), manufactured in imec's silicon photonics ISIPP200 process, consists of two Ge PDs and two grating couplers connected with the PDs through waveguides. The light can be directly coupled into grating couplers by fiber probes. Only one of the PDs is illuminated with light, while the other PD serves as a dummy to balance the impedance at both inputs. The additional dummy PD has a negligible impact on the overall PIC area and associated cost, note that it does not need to be connected to a grating coupler: here this was done only for testing purposes. The two Ge PDs, with >50 GHz bandwidth and $\approx$ 0.8 A/W responsivity in C-band, allow for high bandwidth and good optical receiver sensitivity. Compared with optical receivers with a single-ended input, a differential input structure has better immunity to any noise on the PD bias voltage line, power and ground supplies as these are rejected as common-mode noise [19].

The TIA and PDs are assembled with bondwires. The anodes of the two PDs are connected with the differential inputs of the TIA, and the cathodes of the PDs are connected with a 3.2 V voltage, to reversely bias the PDs. The equivalent inductance of the anode and cathode bondwires and the equivalent capacitance of the PD create a resonance, resulting in peaking in the transfer function of the TIA [20]. The peaking frequency is given by $f_p = 1/2\pi\sqrt{L_{bw}C_{pd}}$; here, L_{bw} denotes the equivalent inductance of the anode and cathode bondwires, and C_{pd} denotes the equivalent capacitance of the PD. The equivalent inductance is proportional to the length of the bondwire. To increase the peaking frequency, the PIC and electrical integrated circuits (EIC) are thinned to the same thickness and placed close to each other to reduce the length of bondwires. Furthermore, each PD cathode is designed with two pads, each connected to the 3.2 V voltage through an individual bondwire, to lower the equivalent inductance of the bondwires of the PD cathode.

III. TIA IMPLEMENTATION

A. TIS and IDCC

The simplified schematic of the TIS and IDCC is depicted in Fig. 2. The fully differential TIS is implemented as a typical shunt-feedback amplifier. Two electrostatic discharge (ESD) devices are placed at the inputs of the TIS to protect the internal circuits, although each ESD device contributes an additional ~50 fF parasitic capacitance. The bandwidth of the TIS is extended with the peaking generated by the equivalent inductance of the bondwires, which are highly dependent on the assembly process. The bandwidth is also highly dependent on R_F and the bias current of Q0, which determine the pole and the gain of the TIS loop. To reduce the bandwidth variation, R_F and the Q0 bias current I_{b1} have been designed to be tunable to compensate the variation of the bondwires and the process variation of R_F. The typical values of R_F and I_{b1} are 300 Ω and 10.5 mA. The R_F is implemented as a poly resistor in parallel to 5 NMOS transistors. The NMOS transistors operate in either the triode region or the cutoff region controlled by a 5-bit digital setting. The cascode transistor Q1 alleviates the Miller effect of the base-collector capacitor C_{bc} of Q0. The tunable current source I_{b0} reduces the collector current of Q1, thereby increasing the output DC voltage of the TIS. The second pole of the loop gain is determined by R_{C1}= 50 Ω and the parasitic capacitor at the collector of Q1. The shunt peaking inductor L_1= 50 pH, in series with R_{C1}, is employed to push the second pole to a higher frequency to increase the phase margin of the loop.

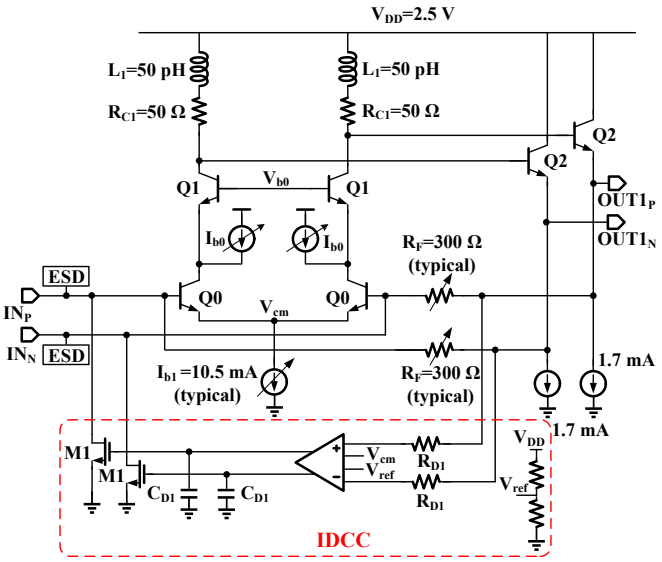

Fig. 2. Simplified schematic of the TIS and IDCC.

The IDCC senses the differential outputs of the TIS with two 30 kΩ resistors (R_{D1}), reducing the addition of parasitic capacitances to the high-speed path. The common mode voltage is sensed from V_{cm} at the emitter of Q0. In the traditional differential TIA, the reference voltage of the IDCC is generated by a dummy TIA [21], [22], which occupies a large area and requires relatively high power consumption. In this design, the reference voltage V_{ref} is generated by a

compact resistive divider of V_{DD}, which only consumes 500 μA DC current. The IDCC output transistors M1, operating in the saturation region, are connected to the inputs of the TIA. The size of M1 is chosen to absorb up to 2 mA of input DC current. The DC bias current of M1 is given by the following equation:

$$I_{D,M1} = \frac{[V_{DD} - R_{c1}(I_{b1}/2 - I_{b0}) - V_{be,Q2}] - (V_{cm} + V_{be,Q0})}{R_F} \quad (1)$$

When the IDCC circuit works normally, V_{cm} would be approximately equivalent to V_{ref}. $I_{D,M1}$ needs to be higher than 0 to keep the IDCC loop active. In this design, the DC bias current of M1 is equal to 250 μA.

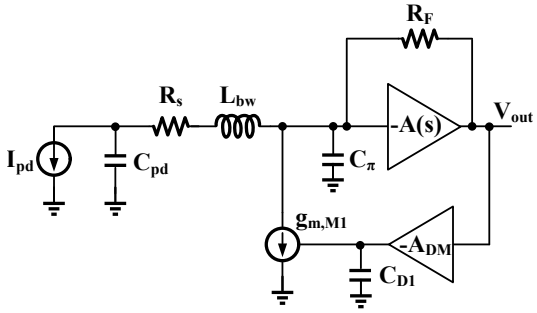

Fig. 3. Simplified differential-mode small-signal equivalent circuit of the TIS and IDCC.

To obtain the transfer function of the TIS and IDCC, the simplified differential-mode small-signal equivalent circuit is shown in Fig. 3. I_{pd}, C_{pd}, R_s and L_{bw} represent the PD current, the parasitic capacitance of the PD, the series resistance of the PD and bondwire, and the parasitic inductance of the bondwire, respectively. $g_{m,M1}$ denotes the transconductance of M1 and C_π denotes the total parasitic capacitance of the bond pad, ESD devices, and base-emitter junction of Q0. The DC gain $A_{DM} = g_m r_o$, where g_m and r_o represent the transconductance and output impedance of the IDCC opamp. Assuming the TIS opamp only has one pole, and its transfer function is given by $A(s) = A/(1 + s\tau)$.

At low frequencies, C_{pd}, R_s, L_{bw} and C_π can be neglected for simplification. The transimpedance is given by:

$$H_{LF} \approx \left(\frac{AR_F}{A+1}\right)\left(\frac{1 + sC_{D1}r_o}{1 + g_{m,M1}g_m r_o(\frac{AR_F}{A+1}) + sC_{D1}r_o}\right) \quad (2)$$

At high frequencies, C_{D1}, $g_{m,M1}$ and the DCOC opamp can be neglected. The transimpedance is approximated by [2]:

$$H \approx H_{(T=\infty)}\left(\frac{T}{1+T}\right) \quad (3)$$

T represents the loop gain of the high-frequency loop, and $H_{(T=\infty)}$ represents the transimpedance when the T is infinite.

Firstly, we consider the transimpedance with condition of $L_{bw} = 0$ and $R_s = 0$. $H_{(T=\infty,Z_{bw}=0)}$ and $T_{(Z_{bw}=0)}$ are given by:

$$H_{(T=\infty,Z_{bw}=0)} = R_F \quad (4)$$

$$T_{(Z_{bw}=0)} = \frac{A}{(1+s\tau)(1+sC_T R_F)} \quad (5)$$

$$C_T = C_{pd} + C_\pi \quad (6)$$

By substituting (4) and (5) into (3), the transimpedance $H_{(Z_{bw}=0)}$ is obtained:

$$H_{(Z_{bw}=0)} \approx \left(\frac{AR_F}{A+1}\right)\left(\frac{1}{1 + \frac{s(\tau + C_T R_F)}{A+1} + \frac{s^2 C_T R_F \tau)}{A+1}}\right) \quad (7)$$

When $L_{bw} \neq 0$ and $R_s \neq 0$, $H_{(T=\infty)}$ and T need to be adapted by [23] [2]:

$$H_{(T=\infty)} = \frac{H_{(T=\infty,Z_{bw}=0)}}{1 + \frac{s}{\omega_{n0}Q_0} + (\frac{s}{\omega_{n0}})^2} \quad (8)$$

$$\omega_{n0} = \frac{1}{\sqrt{L_{bw}C_{pd}}}, Q_0 = \frac{1}{R_s}\sqrt{\frac{L_{bw}}{C_{pd}}} \quad (9)$$

$$T = T_{(Z_{bw}=0)} \cdot \left(\frac{1 + \frac{s}{\omega_{n0}Q_0} + (\frac{s}{\omega_{n0}})^2}{1 + \frac{s}{\omega_{np}Q_p} + (\frac{s}{\omega_{np}})^2}\right) \quad (10)$$

$$C_{eq} = \frac{C_\pi C_{pd}}{C_\pi + C_{pd}} \quad (11)$$

$$\omega_{np} = \frac{1}{\sqrt{L_{bw}C_{eq}}}, Q_p = \frac{1}{R_s}\sqrt{\frac{L_{bw}}{C_{eq}}} \quad (12)$$

The transimpedance H can be obtained by substituting (8) and (10) into (3). The simulated post-layout transimpedance of the TIS and IDCC with the equivalent inductance of bondwires (150 pH or 0 pH for each bondwire) and a PD model (C_{pd} = 38 fF, $R_{s,pd}$ = 30 Ω) is shown in Fig. 4 (a). The transimpedance at 1 GHz is equal to 46.8 dBΩ. At the frequency range from 300 kHz to 3 MHz, the transimpedance curve has a high pass filter (HPF) feature with +20 dB/dec roll-off and 1 MHz 3-dB bandwidth, which is induced by the IDCC loop. For the transimpedance with 150 pH equivalent inductance, a small peak exists at 47.3 GHz, indicating the resonance created by the bondwire inductance and the PD capacitance. When the frequency is higher than 50 GHz, there is a sharp roll-off in the transimpedance curve. The high frequency 3-dB bandwidth of the transimpedance curve is equal to 55.8 GHz. Fig. 4 (b) shows the simulated post-layout transimpedance at the output of each stage with 150 pH equivalent inductance of each bondwire. The 3-dB bandwidths at the outputs of VGA1, VGA2 and output buffer are equal to 54.5 GHz, 54.4 GHz and 52.6 GHz, respectively. The four stages of the TIA have comparable 3-dB bandwidths. The simulated post-layout group delay above 1 GHz of the TIS and IDCC is shown in Fig. 5, the group delay variation below 55.8 GHz is equal to 15.8 ps.

To verify the function of the IDCC circuit, a time domain simulation has been carried out. Two different currents, shown

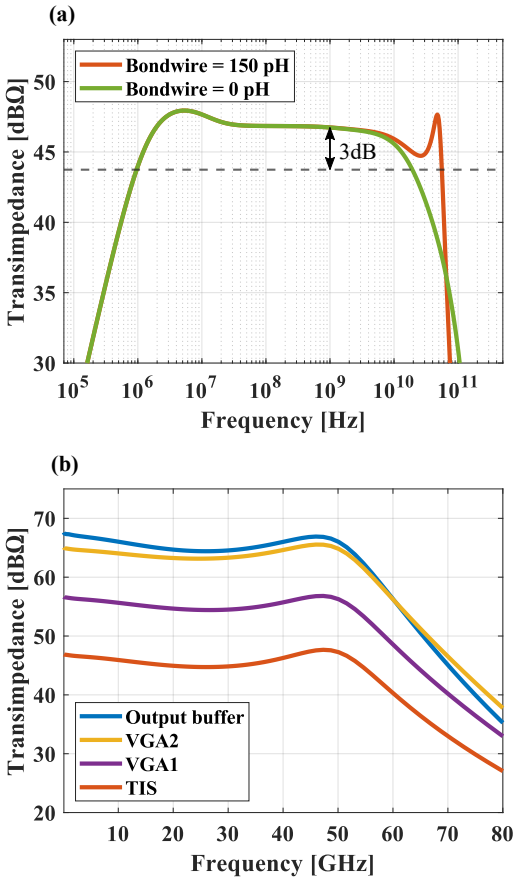

Fig. 4. (a) Simulated post-layout transimpedance gain of the TIS and IDCC (b) Simulated post-layout transimpedance gain at the output of each stage.

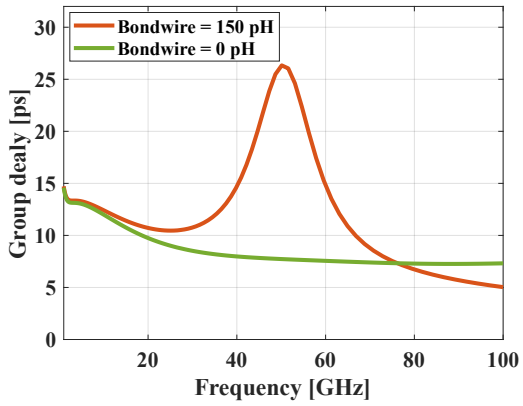

Fig. 5. Simulated post-layout group dealy above 1 GHz of the TIS and IDCC.

in Fig. 6(a), have been injected into the differential inputs of the TIA. The current flowing in the IN_P terminal is comprised of a PAM-4 signal and a 1 mA pulse, while the current flowing in the IN_N terminal is a 0.5 mA pulse. The waveforms in Fig. 6(b) and Fig. 6(c) show the IDCC circuit can absorb the input DC currents and maintain the TIS output DC voltages at a constant value.

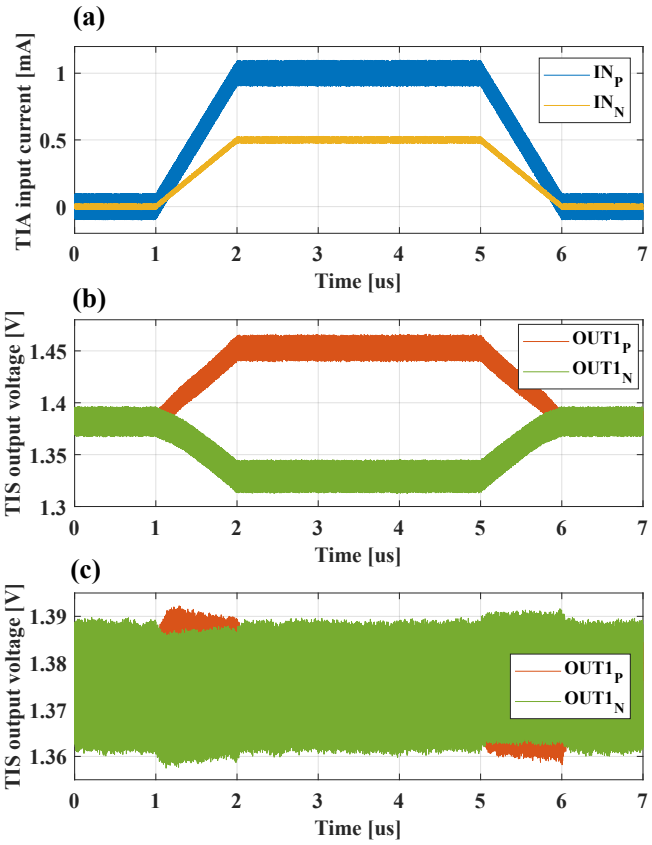

Fig. 6. (a) TIA input currents (b) TIS output voltages when the IDCC is powered off. (c) TIS output voltages when the IDCC is powered on.

As the drain of M1 is connected to the input of the TIS, the noise current of M1 directly contributes to the input-referred noise current. The input-referred noise current density of the TIS and IDCC is approximated by [2]:

$$i_{n,in}^2 \approx \frac{4kT}{R_F} + 4kTR_BC_D^2\omega^2 + \frac{2qI_{C,Q0}C_T^2\omega^2}{gm_0^2} + \frac{2qI_{C,Q0}}{\beta} + i_{n,IDCC}^2 + \cdots \quad (13)$$

where R_B represents the parasitic base resistance of Q0, and C_D denotes the total parasitic capacitance of the PD, bond pad and ESD devices. $I_{C,Q0}$, gm_0 and β represent the collector bias current, transconductance and current gain of $Q0$, respectively.

The IDCC noise current density $i_{n,IDCC}$ is dominated by the M1 transistors, and its noise current density is approx. $i_{n,M1}^2 = 4kT\gamma g_{m,M1}$ [24], where γ denotes the channel noise factor, $g_{m,M1}$ denotes the transconductance of M1. The value of $i_{n,M1}^2$ is proportional to the drain DC current $I_{D,M1}$ of M1. The simulated relative contributions to the output noise of the TIS are shown in Fig. 7. Q0 contributes the majority of the noise, including the thermal noise and the shot noise. M1 with 250 uA DC bias current only contributes 1.3% of the total output noise power of the TIS and IDCC stage, which is acceptable. M1 contributes more noise for high PD DC

currents, while the signal-to-noise ratio is proportional to the PD current.

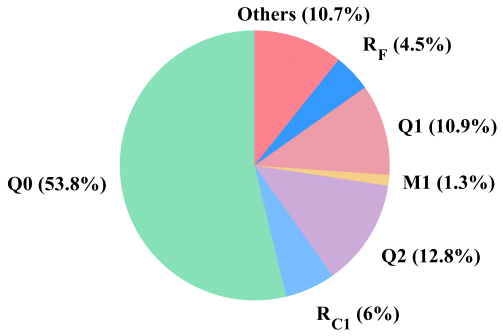

Fig. 7. Simulated relative contributions to the output noise of the TIS.

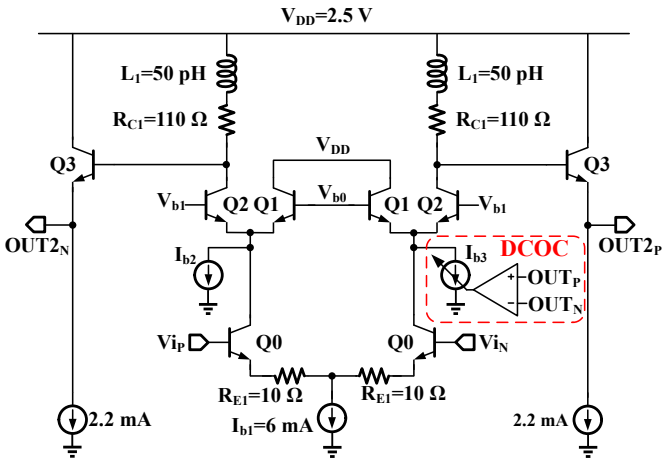

Fig. 8. Simplified schematic of the VGA1 and DCOC.

B. VGA1 and DCOC

Fig. 8 shows the simplified schematic of the VGA1 and DCOC. The gain of the VGA1 stage is variable by fine-tuning the bias voltage V_{b0} and V_{b1}, which are generated from voltage-mode digital-to-analog converters, controlled through digital registers. The shunt peaking inductor L_1 = 50 pH serves to extend the bandwidth. The DCOC loop senses the output voltages of the TIA, eliminating the DC offset of the TIA outputs. The output current I_{b3} of the DCOC loop is connected to the emitter of Q2, avoiding the reduction of the high-frequency bandwidth of the TIA.

C. VGA2 and output buffer

The simplified schematic of the VGA2 is shown in Fig. 9. The variable degeneration resistor R_{E2} is implemented using NMOS transistors in their Ohmic region, having a programmable resistance.

The simplified schematic of the output buffer is shown in Fig. 10. Two ESD devices are placed at the ends of two 50 Ω transmission lines (TLs) to protect the internal circuits. A

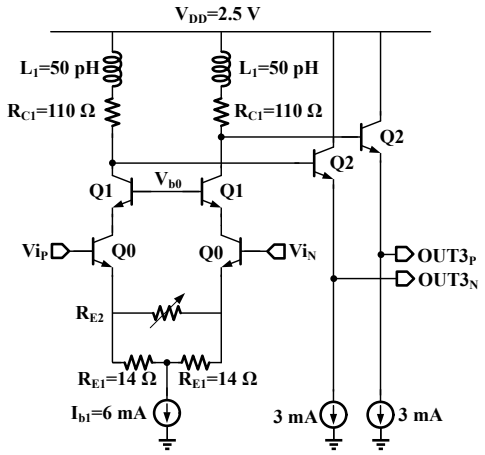

Fig. 9. Simplified schematic of the VGA2.

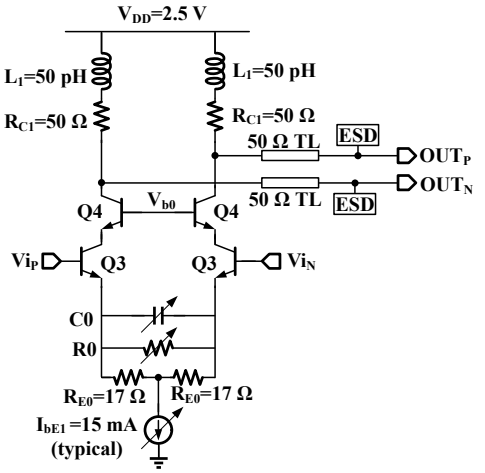

Fig. 10. Simplified schematic of the output buffer.

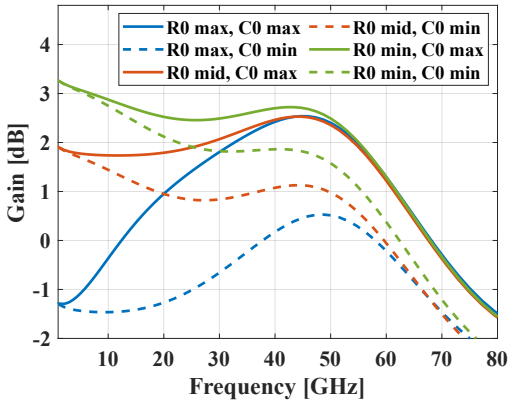

Fig. 11. Simulated post-layout gain of the output buffer.

shunt peaking and a tunable continuous-time linear equalizer (CTLE) are used to compensate for the loss at high frequency. The tunable CTLE is realized by a variable resistor $R0$ and a variable capacitor $C0$. The $R0$ and $C0$ are implemented as NMOS resistances and NMOS varicaps, respectively. Fig. 11 shows the simulated post-layout gain of the output buffer

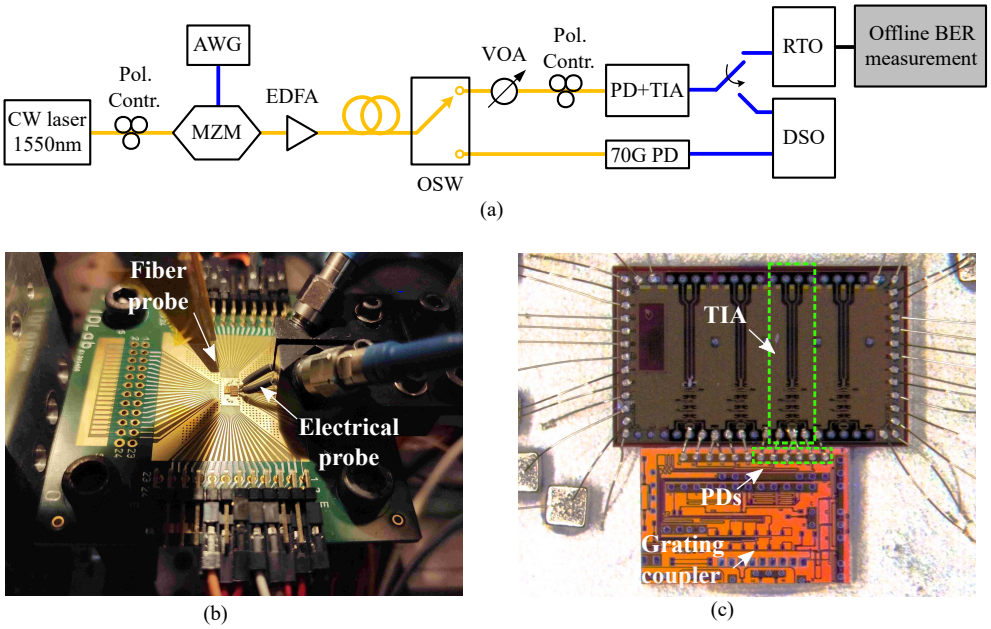

Fig. 12. (a) Measurement setup of the optical receiver (b) Photograph of the PCB with a fiber probe and an electrical GSSG probe (c) Micrograph of the optical receiver.

for different $R0$ and $C0$. The CTLE can provide a maximum peaking of 3.8 dB with the maximum $R0$ and $C0$. In the measurement of this paper, the CTLE is set with the middle $R0$ and maximum $C0$ which provide a 0.6 dB peaking at 44.6 GHz.

IV. Measurement Setup

The measurement setup of the optical receiver is shown in Fig. 12(a). A 256 GSa/s arbitrary waveform generator (AWG, Keysight M8199B) generates $2^{15}-1$ pseudo-random bit sequences (PRBS) mapped to a PAM-4 signal and drives a $LiNbO_3$ Mach-Zehnder modulator (MZM) directly. The MZM is biased at the quadrature point to modulate a 1550 nm (C-band) continuous-wave laser. The MZM output is amplified by an erbium-doped fiber amplifier (EDFA), which is followed by an optical switch (OSW). The OSW is followed by a variable optical attenuator (VOA) and a 70 GHz PD. The VOA is used to control the optical power coupled to the PD of the PIC. To calculate the in-waveguide OMA of the optical receiver, the PD currents are measured by a current meter. The differential outputs of the TIA are probed by a 67 GHz GSSG electrical probe and captured by a digital sampling oscilloscope (DSO) N1046A or a real-time oscilloscope (RTO) UXR1104A with 256 GSa/s sample rate. The DSO is used to capture and analyze the eye diagrams of the optical receiver. The transimpedance gains are calculated based on the waveform captured by the DSO and the measured PD currents. The optical receiver output noise voltages are measured by the DSO when VOA is turned off. The input referred noise currents are calculated based on the transimpedance gains and the output noise voltages. The BERs are obtained by offline data processing based on the data recorded by the RTO. The reference eye diagrams and extinction ratios (ER) are measured at the output of the 70 GHz PD by the DSO. The equalization function of the AWG is employed to compensate the limited bandwidth of the MZM with the 70 GHz PD. When measuring the optical receiver, the same equalization setting has been used so that there is no equalization for the optical receiver at the transmitter side.

The photograph of the PCB with a fiber probe and an electrical probe is shown in Fig. 12(b). The micrograph of the optical receiver is shown in Fig. 12(c), including a PIC and an EIC wirebonded on the PCB. The designed EIC contains four channel TIAs, the tested TIA is highlighted in the dashed green rectangle.

V. Measurement Results

Fig. 13 shows the PAM-4 eye diagrams at 56, 64, 72 and 80 GBd captured by the DSO. The reference eye diagrams captured at the 70 GHz PD output are shown in the first column. The eye diagrams captured at the TIA outputs without and with 5-tap FFE post-processed on the scope are shown in the second and third columns, respectively. The eye diagrams of the optical receiver are open at 56, 64 and 72 GBd without on-scope FFE; a 5-tap on-scope FFE can improve their eye diagrams. Although the eye diagram of the optical receiver is closed at 80 GBd without FFE, a 5-tap on-scope FFE is sufficient to open the eye diagram. The transimpedance gains are equal to 70 dBΩ for 56 and 64 GBd PAM-4 signals, and 65 dBΩ for 72 and 80 GBd PAM-4 signals achieved by reducing the gain of the VGA1 stage.

Based on the waveforms sampled by the RTO, the recorded data is upsampled followed by the determination of the sampling time and decision thresholds. The BERs are calculated by counting the errors bit by bit, ensuring that each BER point comprises a minimum of 10 errors. Fig. 14 shows the

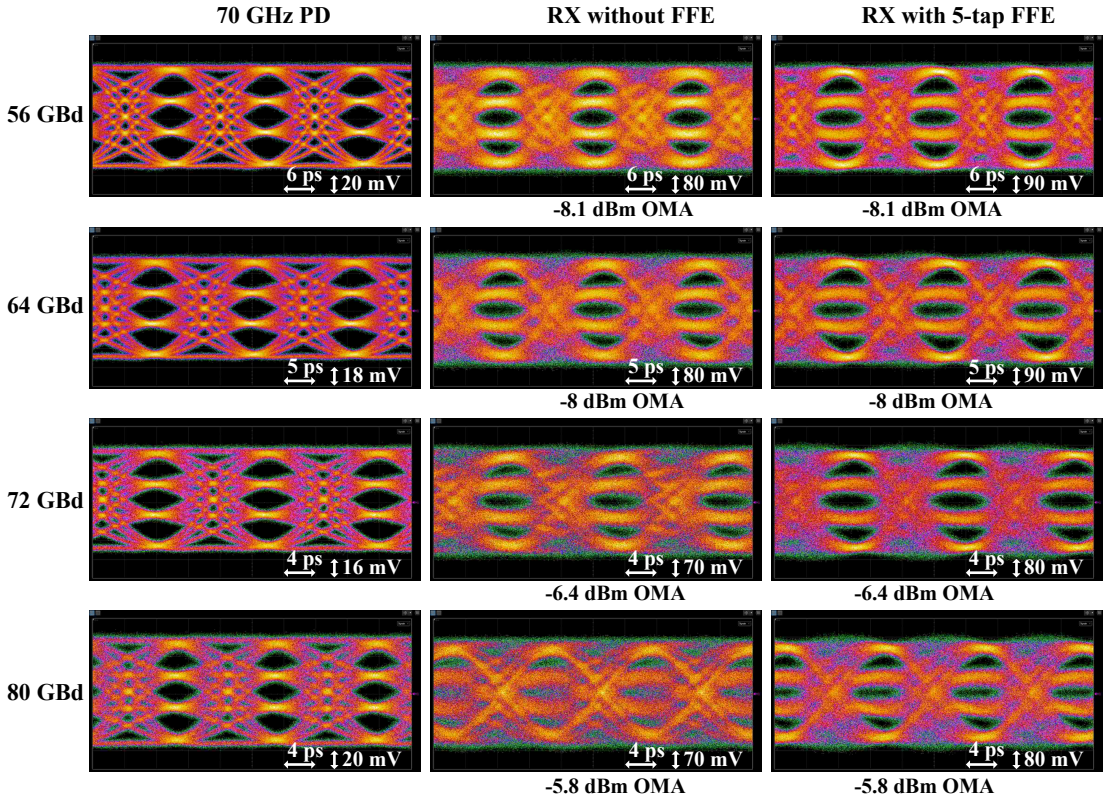

Fig. 13. Eye diagrams captured by the DSO, at the 70 GHz PD output (first column), at the TIA outputs without on-scope FFE (second column) and with 5-tap on-scope FFE (third column).

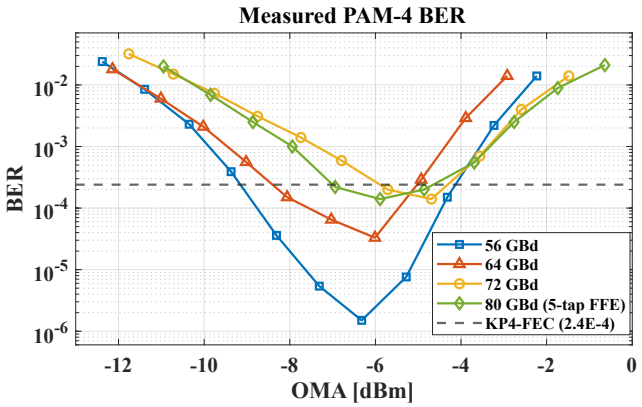

Fig. 14. Measured PAM-4 BER vs. $P_{OMA,dBm}$.

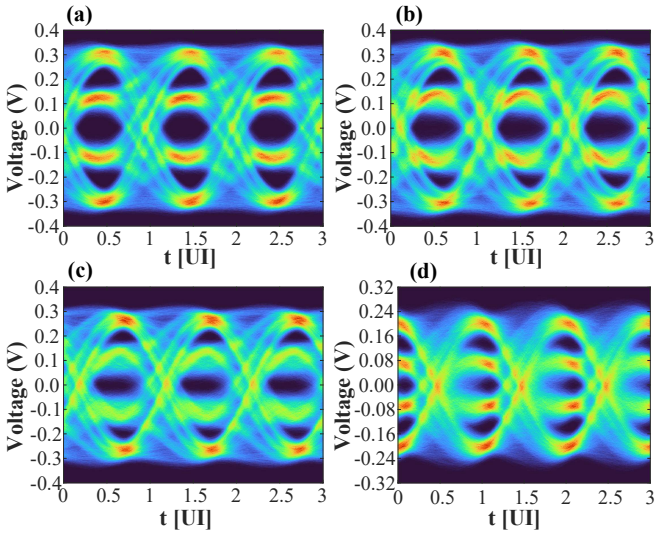

Fig. 15. Eye diagrams at minimal BER points captured by the RTO, (a) 56 GBd (-6.3 dBm OMA) (b) 64 GBd (-6.0 dBm OMA) (c) 72 GBd (-4.7 dBm OMA) (d) 80 GBd with 5-tap FFE (-5.9 dBm OMA).

measured PAM-4 BER vs. $P_{OMA,dBm}$ curves. For each baud rate, the setting of the TIA remains constant across all data points on the corresponding BER curve. The 56, 64 and 72 GBd PAM-4 signals are processed without employing any equalization in the data processing, while a 5-tap FFE has been introduced for 80 GBd PAM-4 signals. The in-waveguide OMA sensitivities are equal to -9.2, -8.4, -5.9 and -7 dBm for 56, 64, 72 and 80 GBd PAM-4 operations, respectively, at KP4-FEC (2.4×10^{-4}) threshold. All the BER curves exhibit a descending trend followed by an ascending trend. Taking the 56 GBd PAM-4 signal as an example, the BER curve exhibits a descending trend when the OMA is below -6.3 dBm. The descending trend of the BER is due to the increase of the signal-to-noise ratio of the PAM-4 signals as the increase of the optical power. While the BER curve exhibits an ascending trend when the OMA is higher than -6.3 dBm. The ascending trend is due to the BERs being limited by the total harmonic

TABLE I
COMPARISON WITH CURRENT STATE-OF-THE-ART PAM-4 OPTICAL RECEIVERS.

ref.	Technology	f_t (GHz)	Data rate (Gb/s)	R_T (dBΩ)	Input ref. Noise (μA_{rms})	R (A/W)	Sens. @KP4 (dBm)	pJ/b	Test pattern	DSP
[18] ECOC'23	55nm BiCMOS	320	200	56.9	N/A	0.8	<-4	2.5	PRBS13	5-tap FFE
[17] OE'23	N/A	N/A	160	N/A	N/A	0.85	-2.7	1.2	$2^{15}-1$	51-tap FFE
[11] ISSCC'23	16nm FinFET	N/A	106.25	77	1.14	N/A	-13.97	0.98	PRBS13Q	12-tap FFE + 1-tap DFE
[10] JSSC'22	16nm FinFET	N/A	112	63	3.0	0.6	-9.6 / -8.2	0.69	PRBS13Q	4-tap FFE + 4-tap DFE / no
[15] PTL'19	55nm BiCMOS	320	106	66	3.2	0.63	-5	1.51	2^9-1	no
This work	130nm BiCMOS	350	112	70	3.9	0.8	-9.2	1.41	$2^{15}-1$	no
			128	70	3.9	0.8	-8.4	1.23	$2^{15}-1$	no
			144	65	4.8	0.8	-5.9	1.1	$2^{15}-1$	no
			160	65	4.8	0.8	-7	0.99	$2^{15}-1$	5-tap FFE

distortion. The eye diagrams at the minimum BER points captured by the RTO are shown in Fig. 15.

A comparison with current state-of-the-art PAM-4 optical receivers is shown in Table I. At 160 Gb/s, compared with [17], this work only needs a 5-tap FFE to compensate the loss of the receiver, and the sensitivity is improved by 4.3 dBm. Although a 200 Gb/s optical receiver has been reported in [18], it employs a traveling wave structure to achieve high bandwidth, resulting in a relatively high 2.5 pJ/b power consumption. This work only needs 0.99 pJ/b power consumption at 160 Gb/s PAM-4 operation. Ref [11] demonstrates a 106.25 Gb/s PAM-4 optical receiver in 16nm FinFET process, achieving -13.97 dBm OMA sensitivity. Ref [10] reports a 112 Gb/s PAM-4 receiver with a sensitivity of -8.2 dBm without equalization. Ref [15] demonstrates a 106 Gb/s PAM-4 optical receiver with a sensitivity of -5 dBm. This work achieves BER below KP4-FEC at 144 Gb/s without equalization and 160 Gb/s with 5-tap FFE.

VI. CONCLUSIONS

A 160 Gb/s PAM-4 optical receiver consisting of a fully differential TIA in SiGe BiCMOS process wirebonded with two >50 GHz Ge PDs in silicon photonic process has been presented. A fully differential IDCC circuit has been proposed to absorb the PD current and eliminate the offset of the TIS. The optical receiver can achieve below KP4-FEC BERs at 56, 64, 72 GBd PAM-4 without any equalizer to compensate the receiver, the corresponding OMA sensitivities are equal to -9.2, -8.4, -5.9 dBm, respectively. At 80 GBd, a 5-tap FFE is sufficient to open the eye diagram, achieving a sensitivity of -7 dBm at KP4-FEC and a power consumption of 0.99 pJ/b.

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