A Multi-GHz Inverter-Based ASDM with Distortion Cancellation

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***Abstract*—This brief proposes and demonstrates an asynchronous sigma-delta modulator (ASDM) which is based entirely on pseudo-digital inverters. To achieve multi-GHz operation, the proposed ASDM employs a delay-based approach, with a quantizer consisting of a cascade of pseudo-differential inverters. The loop filter is a Gm-RC low-pass filter with a Nauta transconductor [1], which consists of two input inverter pairs loaded by a self-coupled and cross-coupled inverter pair. By suitably sizing the loop filter, the non-linearity of the quantizer compensates the non-linearity of the transconductor. Fabricated in 28 nm CMOS, the prototype oscillates at 6.9 GHz, achieving an SNDR of 46.5 dB and a dynamic range of 56.6 dB over a 500 MHz bandwidth. The prototype occupies an area of 58 (µm)^2, and consumes a power of 2.6 mW from a 0.9 V supply.**

***Index Terms*—inverter-based, asynchronous sigma-delta modulator (ASDM), pulse-width modulator (PWM)**

I. INTRODUCTION

ASYNCHRONOUS sigma-delta modulators transform their input signal to a two-level signal, without suffering from quantization noise [2]. For this reason, ASDMs are particularly useful at the input of ADCs [3]–[5] and class-D power amplifiers [6] to relax the linearity requirements of their input stage. Alternatively, using a time-to-digital converter, a complete ADC can be realized with most of its functionality in the digital domain [7], reducing area and power consumption.

Unlike its synchronous counterpart, the modulator is not clocked. Instead, the modulator exhibits a self-oscillation of which both the instantaneous frequency and pulse-width are modulated by the input signal, as shown in Fig. 1c. Prior implementations rely on a quantizer with hysteresis [2], [8] to establish a well-defined self-oscillation frequency. However, higher frequencies can be obtained by eliminating this hysteresis and by relying solely on the inherent delay of the quantizer.

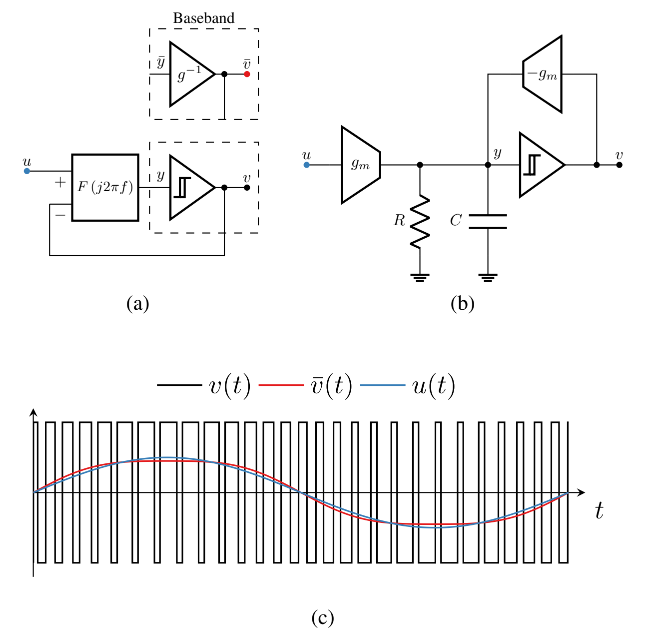

Fig. 1. (a) Block diagram of a generic ASDM, and its baseband representation. (b) Circuit diagram of a first-order ASDM using a Gm-RC low-pass filter. (c) Time domain waveform of the output signal v, and its baseband representation $\bar{v}$ (no carrier and its sidebands), for a sinusoidal input signal u.

This approach does not lead to a less linear design [9], contrary to what was previously believed.

We propose an inverter-based implementation that provides compatibility with the decreasing supply voltage and stricter layout rules of aggressively scaled CMOS technologies, while simultaneously benefiting from the improvements in switching speed and power efficiency. This approach results in a very compact modulator with a self-oscillation frequency at multi-GHz frequencies. Fabricated in $28\,\mathrm{nm}$ CMOS, the prototype oscillates at $6.9\,\mathrm{GHz}$, achieving an SNDR of $46.5\,\mathrm{dB}$ and a dynamic range of $56.6\,\mathrm{dB}$ over a $500\,\mathrm{MHz}$ bandwidth. The prototype occupies an area of $58\,(\mu\mathrm{m})^2$, and consumes a power of $2.6\,\mathrm{mW}$ from a $0.9\,\mathrm{V}$ supply. This prototype is intended for upstream sigma-delta-over-fiber transceivers [10]. However, it can be readily adapted to suit a wider range of applications.

This work is structured as follows. In Section II, we outline the performance-defining parameters of the ASDM. In Section III, we discuss our implementation. The experimental results are then discussed in Section IV. Finally, conclusions are drawn in Section V.

Manuscript received TODO; revised TODO; accepted TODO. Date of publication TODO; date of current version TODO. This work was supported by the Research Foundation - Flanders (file number 1S85222N) and the H2020 Int5Gent project (project number 957403). *(Corresponding author C. Meysmans.)*

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II. Asynchronous Sigma-Delta Modulation

The block diagram of a generic ASDM is shown in Fig. 1a. It is a closed-loop configuration consisting of a continuous-time loop filter $F(j2\pi f)$ and a quantizer, which generates the binary output signal. This structure is very similar to a conventional (synchronous) sigma-delta modulator, except that there is no sampling in the loop. Consequently, the error introduced by the quantizer cannot be modeled as a white noise sequence. Instead, as will be detailed below, it can be modeled by an odd, expansive non-linear function g^{-1}. As a result, the role of the loop filter shifts from shaping quantization noise to suppressing the non-linearity of g^{-1}. However, typically an active loop filter also compresses large input signals due to the non-linearity of its transconductor. Instead of optimizing both non-linearities independently, we propose to compensate the loop filter compression with the quantizer expansion, saving both power and area.

To quantify the intrinsic distortion of an ASDM, the high frequency behavior ($f \geqslant f_c$) of the loop filter $F(j2\pi f)$ should satisfy [9], [11]

$$\Re\{F(j2\pi f)\} \approx \frac{1}{(2\pi f\tau_r)^2}, \quad \Im\{F(j2\pi f)\} \approx \frac{-1}{2\pi f\tau_i} \tag{1}$$

where $\tau_r = \sqrt{g_m R}\cdot C/g_m$ and $\tau_i = C/g_m$ for the low-pass filter in Fig. 1b. Under these conditions, the baseband response of the ASDM can be modeled by the following non-linear differential equation [9], [11]

$$(u-\bar{v}) * f = g(\bar{v}) = g_1\bar{v} - g_3\sum_{m=1}^{\infty}\bar{v}^{2m+1} \tag{2}$$

where u is the input, $\bar{v}$ is the baseband output, f is the loop filter, and g is an odd, compressive non-linear function. The baseband representation is equivalent to substituting g^{-1} for the quantizer, as shown in Fig. 1a. Prior implementations rely on a quantizer with hysteresis [2], [8] (e.g., a Schmitt trigger). However, higher frequencies can be obtained by eliminating this hysteresis and by relying solely on the inherent delay of the quantizer. On top of that, the self-oscillation frequency now only depends on the quantizer delay T_D and is given by [9], [11]

$$f_c = \frac{1}{4T_D} \tag{3}$$

Additionally, the coefficients of g can now be approximated as [9], [11]

$$g_1 \approx \frac{T_D}{\tau_i} = g_m R\left(\frac{T_D}{RC}\right), \tag{4}$$

$$g_3 \approx \frac{2}{3}\left(\frac{T_D}{\tau_r}\right)^2 = \frac{2}{3}g_m R\left(\frac{T_D}{RC}\right)^2 \tag{5}$$

Using perturbation theory, (2) can be used to determine the level of third-order harmonic distortion, yielding [9], [11]

$$|A_3| = K_3(A)\frac{1}{\left|g_1^{-1}F(j2\pi 3\mu)\right|}\left|\frac{g_3}{g_1}\right| \tag{6}$$

where A and μ are the amplitude and frequency of the input signal, respectively. $K_3(A)$ describes the impact of the modulation depth on the distortion, and can be approximated as $A^3/4$ for $A \ll 1$.

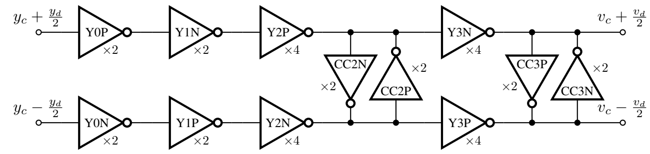

Fig. 2. Quantizer circuit

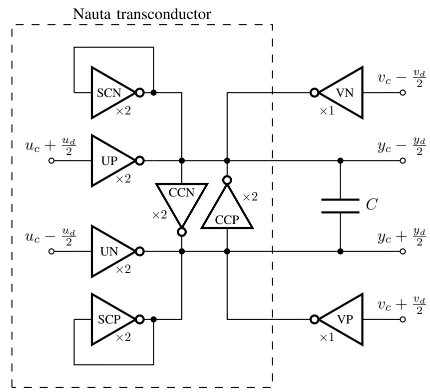

Fig. 3. Loop filter circuit

To compensate the third-order non-linearity of the transconductor, (6) should be tuned to match the level of third-order distortion of the transconductor. This can be realized by tuning the filter time constant RC. However, to ensure effective compensation over input frequency, we must ensure that $F(j2\pi\mu) = g_m R$ across the targeted bandwidth f_B of the ASDM, limiting the filter time constant, $RC \leqslant 1/(2\pi f_B)$.

III. Implementation

A. Quantizer

The quantizer comprises a cascade of pseudo-differential inverters, as shown in Fig. 2. A total of four stages was selected to obtain a sufficiently large gain. The last stage comprises four unit inverters to provide sufficient drive strength. The first stage comprises only two unit inverters. Although further reducing the size of the first stage results in a lower static power consumption, we decided against it in order to maintain a reasonable ratio between the first and last stage. A large ratio between these stages would negatively impact the overall propagation delay. For the intermediate stages, the number of unit inverters was chosen to minimize the overall propagation delay. Additionally, cross-coupled inverters were added to prevent common mode oscillations. The gain of the first two stages minimizes the resulting hysteresis, as seen by the input. Ultimately, this design procedure yielded a quantizer with a simulated propagation delay of $27.5\,\mathrm{ps}$, which corresponds to a $9.1\,\mathrm{GHz}$ self-oscillation frequency, according to (3).

B. Loop Filter

For high speed operation, a Gm-RC low-pass filter is used to implement the loop filter. This is shown in Fig. 1b. Both the input and feedback transconductor are implemented using

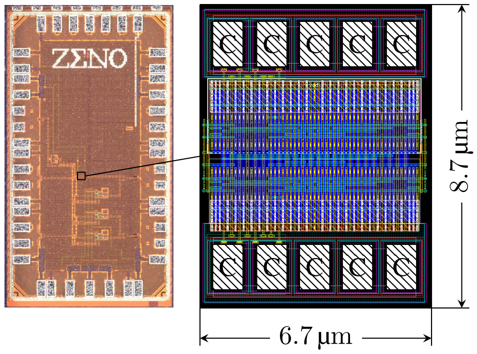

Fig. 4. Die micrograph and ASDM layout view

a Nauta transconductor [1], as shown in Fig. 3. A Nauta transconductor is a differential circuit comprising an input inverter pair (UP, UN) loaded by a cross-coupled inverter pair (CCP, CCN) and a self-coupled inverter pair (SCP, SCN). Since both the input and feedback transconductor share the same output, the cross-coupled and self-coupled inverter pair can be shared [12], saving both area and power. The output impedance of the Nauta transconductors is used to realize R. Contrary to the normal Nauta configuration, as explained in [1], where the output resistance is canceled, we intentionally sized the self-coupled invertor to realize the required output resistance R, realizing a low-pass filter without internal parasitic poles. In our design, the input inverter pair was sized twice as large as the feedback inverter pair. This introduces a gain of $6\,\mathrm{dB}$ in the ASDM operation and reduces the full scale differential input amplitude to half the supply voltage, i.e., $0.9\,\mathrm{V_{pp}}$. Consequently, the transconductor will relatively behave more linear.

If the transistors would follow the well known square law model, the Nauta transconductor is perfectly linear. However, a real deep submicron transistor deviates significantly from this model. Consequently, in this case a Nauta transconductor exhibits third-order distortion (see (9) in [1]). Additionally, mismatch introduces second-order distortion and further degrades the linearity.

Due to the very high self-oscillation frequency, and the rather limited linearity of the Nauta transconductor, the loop filter does not have to satisfy very stringent requirements. Using the design procedure of Section II, we found that a DC gain of $-2.2\,\mathrm{dB}$, combined with a $55\,\mathrm{fF}$ MOM-type capacitor enables the ASDM to compensate the non-linearity of the Nauta transconductor. The resulting $1.9\,\mathrm{GHz}$ cut-off frequency ensures that the distortion is independent of input frequency well beyond the targeted bandwidth of the ASDM.

IV. Experimental Results

The prototype was fabricated using a commercially available $28\,\mathrm{nm}$ CMOS technology. Fig. 4 shows the die micrograph, which includes test circuits beyond the scope of this brief. Also shown is the ASDM layout view. The ASDM measures $6.7\,\mu\mathrm{m} \times 8.7\,\mu\mathrm{m}$. Its input is directly connected to the bonding pads and is differentially terminated with an off-chip $100\,\Omega$ resistor. Its output is connected to the bonding

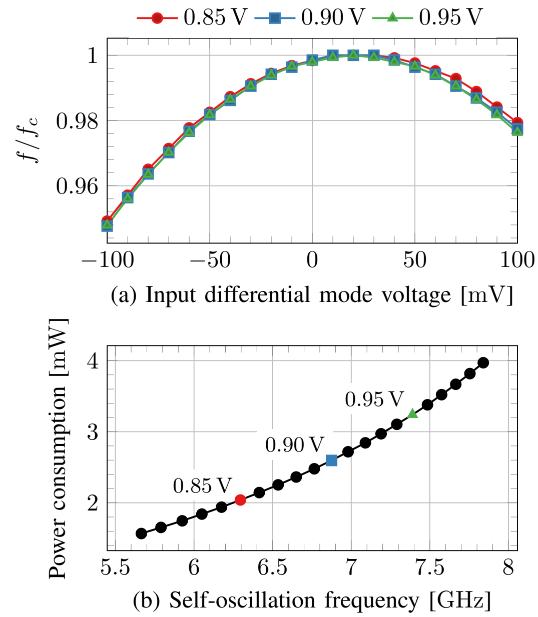

Fig. 5. (a) Ratio of the instantaneous frequency f to the self-oscillation frequency f_c as a function of the input differential mode voltage. The result is shown for different supply voltages. (b) Power consumption and corresponding self-oscillation frequency as a function of the supply voltage (in steps of $10\,\mathrm{mV}$)

pads through a current-mode logic driver, whose power consumption is not included in the reported measurements. The prototype is wirebonded to a custom printed circuit board.

The input signal is sourced from a Keysight N5247B PNA-X, which can generate an accurately balanced differential signal. The receivers of the PNA-X are configured as a differential spectrum analyzer. The available PNA-X, however, lacks support for noise measurements. Hence, a Keysight N9020A MXA spectrum analyzer is used for this purpose. This instrument, however, requires a single-ended input signal and hence a wideband balun is used to perform the differential to single-ended conversion. As will be detailed below, the imbalance of this balun introduces unwanted distortion, resulting in a degraded measured linearity. To overcome this, the PNA-X linearity measurements are combined with the MXA noise measurements to obtain the SNDR of the modulator

In a first set of measurements, the self-oscillation of our circuit is characterized. Assuming no offset, the self-oscillation frequency f_c is the instantaneous frequency f at which the ASDM oscillates when a zero input u is applied. When a non-zero input is applied, the instantaneous frequency is given by [9], [11]

$$f \approx f_c\left(1 - u^2\right) \tag{7}$$

We measured the instantaneous frequency as a function of the DC input voltage. The result, after dividing it by $\max(f)$ which, according to (7), is equal to the self-oscillation frequency, is shown in Fig. 5a for different supply voltages. As can be seen from the figure, the measurement matches the predicted parabolic behavior of (7). For the considered supply voltages, the vertex of the parabola occurs for an input

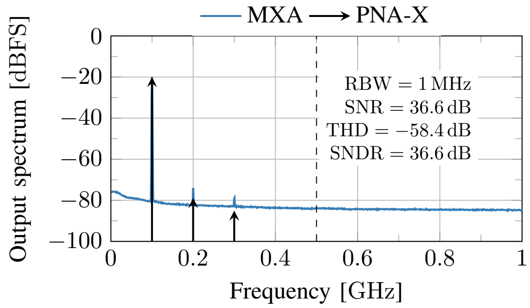

Fig. 6. Output spectrum of a $-20\,\mathrm{dBFS}$ $100\,\mathrm{MHz}$ input tone for a $0.9\,\mathrm{V}$ supply voltage, as measured by the MXA with a $1\,\mathrm{MHz}$ resolution bandwidth. Also shown are the levels of the fundamental tone and its distortion components, as measured by the PNA-X.

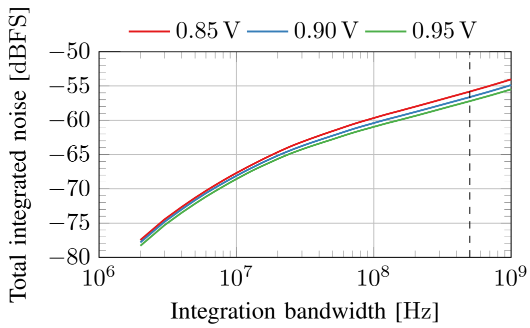

Fig. 7. Total integrated noise as a function of the integration bandwidth. The result is shown for different supply voltages.

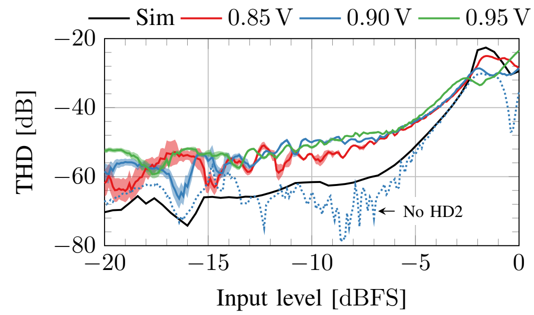

Fig. 8. THD for a $100\,\mathrm{MHz}$ input tone as a function of the input level. The measurement was repeated 201 times on a single die. The result is shown for different supply voltages. Also shown is the simulated result and the THD for a $0.9\,\mathrm{V}$ supply voltage when neglecting the second-order harmonic distortion. The lines represent the mean, while the shaded areas represent the range of values within one standard deviation of the mean.

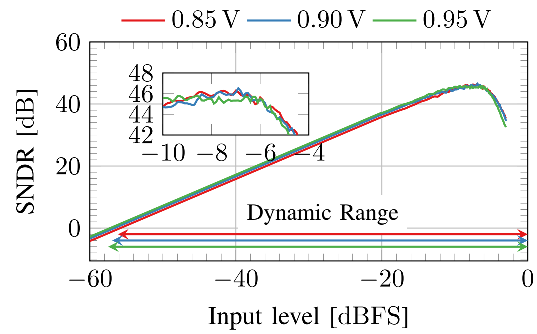

Fig. 9. SNDR in a $500\,\mathrm{MHz}$ bandwidth for a $100\,\mathrm{MHz}$ input tone as a function of the input level. The result is shown for different supply voltages.

differential mode voltage of around $20\,\mathrm{mV}$. Hence, we can conclude that this sample has a $20\,\mathrm{mV}$ offset voltage.

Next, the self-oscillation frequency and the corresponding power consumption is measured as a function of the supply voltage (in steps of $10\,\mathrm{mV}$). The result is shown in Fig. 5b. The input common mode voltage is set to half the supply voltage, while the input differential mode voltage is set to $20\,\mathrm{mV}$ to compensate the offset voltage. The measurement shows self-oscillation frequencies of $6.3\,\mathrm{GHz}$, $6.9\,\mathrm{GHz}$, and $7.4\,\mathrm{GHz}$ at supply voltages of $0.85\,\mathrm{V}$, $0.90\,\mathrm{V}$, and $0.95\,\mathrm{V}$, respectively. The corresponding power consumptions are $2.0\,\mathrm{mW}$, $2.6\,\mathrm{mW}$, and $3.2\,\mathrm{mW}$. These measurement points are marked for reference. The loop filter accounts for $53.3\,\%$ of this power, while the comparator utilizes the remaining $46.7\,\%$.

Fig. 6 shows the output spectrum of a $-20\,\mathrm{dBFS}$ $100\,\mathrm{MHz}$ input tone for a $0.9\,\mathrm{V}$ supply voltage, as measured by the MXA with a $1\,\mathrm{MHz}$ resolution bandwidth. This is the largest input signal for which we do not overload the input of the instrument without using an attenuator. Also shown are the levels of the fundamental tone and its distortion components, as measured by the PNA-X. These distortion levels are considerably better than those measured by the MXA. As was explained above, this is due to the imbalance of the balun at the input of the MXA. Hence, the PNA-X is used for distortion measurements (THD), whereas the MXA is used for noise measurements (SNR). Consequently, the SNDR is a combined measurement, employing the results of both instruments. Using this procedure, we obtain a $36.6\,\mathrm{dB}$ SNR, a $-58.4\,\mathrm{dB}$ THD, and a $36.6\,\mathrm{dB}$ SNDR.

Next, the total integrated noise as a function of the integration bandwidth is measured. The result is shown in Fig. 7 for different supply voltages. For the considered bandwidths, the total integrated noise is dominated by $1/f$ noise. In fact, the simulated $1/f$ corner frequency is $91\,\mathrm{MHz}$, which results from the small devices used. Nonetheless, this design choice is justified since the performance is still limited by distortion. It helps minimize power consumption for a given self-oscillation frequency and input bandwidth, and leads to a compact design. For a $500\,\mathrm{MHz}$ bandwidth, the measurement shows a total integrated noise of $-55.8\,\mathrm{dBFS}$, $-56.6\,\mathrm{dBFS}$, and $-57.2\,\mathrm{dBFS}$ at supply voltages of $0.85\,\mathrm{V}$, $0.90\,\mathrm{V}$, and $0.95\,\mathrm{V}$, respectively. These results are in very good agreement with the simulated noise performance of the loop filter.

Next, the THD is measured for a $100\,\mathrm{MHz}$ input tone as a function of the input level. This measurement was repeated 201 times on a single die. The result is shown in Fig. 8 for different supply voltages. Also shown is the simulated result and the THD for a $0.9\,\mathrm{V}$ supply voltage when neglecting the second-order harmonic distortion. The lines represent the mean, while the shaded areas represent the range of values within one standard deviation of the mean. The THD is dominated by second-order harmonic distortion, caused by mismatch resulting from the very small area of the circuit. Meanwhile, the third-order harmonic distortion closely mirrors the simulations.

Finally, the SNDR in a $500\,\mathrm{MHz}$ bandwidth is measured

TABLE I
PERFORMANCE OVER A 500 MHz BANDWIDTH

	Measured			Simulated[a]	
	0.85 V	0.90 V	0.95 V	μ	σ
Offset [mV]	20	20	20	4.9	16.6
P [mW]	2.0	2.6	3.2	2.9	0.2
f [GHz]	6.3	6.9	7.4	7.9	0.4
DR [dBFS]	55.8	56.6	57.2	57.5	0.2
SNDR [dB]	46.3	46.5	45.8	-	-
SNDR @ −10 dBFS [dB]	44.7	44.7	45.6	49.2	1.5

[a] $V_{DD} = 0.90\,V$, $T = 70°$

TABLE II
COMPARISON WITH STATE OF THE ART

	This work	[13][a]	[14]	[2]	[15]
V_{DD} [V]	0.9	1	1.8	1.8	0.25
Tech [nm]	28	65	180	180	130
Area [mm^2]	58×10^{-6}	6.5×10^{-3}	0.026	0.04	0.141[b]
Order	1	1	1	2	1
P [W]	2.6 m	240 µ	1.5 m	2.2 m	28 n
f [Hz]	6.9 G	300 M	140 M	120 M	630
BW [Hz]	500 M	2 M	8 M	12 M	30
DR [dBFS]	56.6	-	70	70	58
SNDR [dB]	46.5	-	-	-	58
FoM_s [dB]	169	-	167	167	148

[a] Used in cascade with a VCO-ADC. Separate performance of ASDM not reported.
[b] Without passive components (external).

for a 100 MHz input tone as a function of the input level. The result is shown in Fig. 9 for different supply voltages. A peak SNDR of 46.3 dB, 46.5 dB, and 45.8 dB is measured at supply voltages of 0.85 V, 0.90 V, and 0.95 V, respectively.

The measured performance, along with a post-layout Monte-Carlo process and mismatch simulation ($N = 200$), is summarized in Table I. Despite the poor power supply rejection of inverter-based solutions, the circuit proves to work reliably across varying supply voltages. Nonetheless, practical implementations would benefit from having a regulated supply.

As shown in Table II, the reported self-oscillation frequency is a 23× increase with respect to the previously reported fastest design [13]. Our design obtains the best Schreier figure-of-merit FoM_s [16], while being the most compact in size.

V. CONCLUSION

We have successfully demonstrated a multi-GHz ASDM. Its inverter-based implementation provides compatibility with the decreasing supply voltage and stricter layout rules of aggressively scaled CMOS technologies, while simultaneously benefiting from the improvements in switching speed and power efficiency. Fabricated in 28 nm CMOS, the prototype oscillates at 6.9 GHz, achieving an SNDR of 46.5 dB and a dynamic range of 56.6 dB over a 500 MHz bandwidth. The prototype occupies an area of $58\,(\mu m)^2$, and consumes a power of 2.6 mW from a 0.9 V supply.

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