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Efficient Low-Voltage Phase Shifter with Inkjet-Printed Liquid Crystal on a Silicon on Insulator Platform

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A new electro-optic phase shifter device architecture consisting of two lateral rail electrodes in doped silicon close to a waveguide with a liquid crystal cladding is demonstrated. Starting with a completed silicon photonics wafer of IMEC's iSiPP50G platform (including modulators, detectors, and metallization), the back-end-of-line stack is opened up locally down to the waveguides. Liquid crystal is deposited in the recesses using inkjet printing. The narrow gaps between the rail electrodes and the waveguide core allow for actuation with a low voltage, and increase the overlap with the actuated liquid crystal. The demonstrated device geometry has low carrier absorption losses even though the side-rails are doped. This allows an increased driving frequency, eliminating phase flicker. A phase shift of 2 π for 2.7 V is obtained within 100 µm, going up to 6 π at 10 V with an insertion loss of 1 dB. Models suggest a power consumption <1 nW. The performance of this phase shifter is unmatched by alternative techniques that either require a higher voltage, have a larger optical loss or consume more electrical power. A novel purely digital driving scheme is demonstrated enabled by the unique device architecture, simplifying the required driver electronics.

1. Introduction

Silicon-on-insulator (SOI) platforms have emerged as one of the most popular material systems for photonic integrated circuits in the telecommunication wavelength range (i.e., 1200–1650 nm). With increasing circuit complexity comes the need for more configurability and tuning to adjust the flow of light to perform different functions, but also to compensate the effect of fabrication variations.[1,2] For both purposes, we need optical phase shifters (PS) with following properties:

a) Low drive voltage (CMOS compatible)
b) Low power consumption
c) Low insertion loss, as light has to pass through many of these devices.
d) Compact (both in area as in the optical path length)
e) Low cross-talk between the actuators
f) Efficiently integrated on a photonics platform

Since there exists a fundamental trade-off between the magnitude of change in refractive index and the time-scale of the used electro-optic (EO) mechanism, slower electro-optic effects compared to high-speed modulators are preferred as these are more compact and have a lower drive voltage. Furthermore, the slower response time of a phase shifter simplifies the required

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driver electronics and consequently lowers the power consumption of the driver electronics, as the phase shifter automatically filters out high frequency components causing phase flicker. For this reason, effects with a timescale in the order of *ms* or *s* are preferred in the context of tuning, as opposed to modulators requiring a high bandwidth at the cost of device length.

These qualities are especially important for so-called programmable photonic circuits, as they scale up to hundreds or even thousands of on-chip phase shifters.[3–10]

Despite the compact passive waveguide components, silicon photonics does not provide such an ideal phase shifter. A phase shift ($\Delta\phi = \frac{\Delta n_{\text{eff}} L}{\lambda_0} 2\pi$) can be induced with various thermo-optic or electro-optic effects. Today, the most commonly used PS is based on a heater close to the waveguide, which consumes several mW to induce a π phase shift.[11] Another EO mechanism available in silicon is the plasma dispersion effect, typically used for modulation rather than tuning. This is weaker, requires longer optical lengths and the carriers also induce significant optical losses. A third mechanism that can be used in silicon, is based on micro-electromechanical (MEMS) actuators. These can achieve a large phase shift over a short length, but the technique requires significant additional processing and the actuators require a high driving voltage.[12]

All alternatives to implement EO-effects introduce new materials in the proximity of the silicon waveguide. High-speed modulators usually employ the Pockels effect[13,14], while slower phase shifters for tuners can use a more diverse range of effects that are usually stronger. For instance, phase-change materials (PCM) have two or more stable phases with different optical properties, indirectly actuated through a heater.[15,16] Another nonvolatile mechanism recently demonstrated is based on domain-flipping in ferro-electric materials, such as barium titanate (BTO).[17] One can also use the piëzo-electric effect, inducing a phase shift through strain[18] or mechanical motion.[19]

In this study, we make use of the anisotropy of liquid crystals (LC), by reorienting the molecules with an external electric field.[20,21] The new active materials needs to be integrated close to the waveguides. In most silicon photonics platforms, the waveguides are defined in the front-end-of-line (FEOL), where high temperatures are used and strict rules to prevent contamination complicates the introduction of new materials. Therefore, new materials are preferably added at a later stage, but then the waveguides are typically covered with a thick back-end-of-line (BEOL) stack of dielectrics and metal interconnects. Luckily, many platforms, such as the IMEC iSiPP50G platform used here, offer a process module to locally open this BEOL stack and expose the waveguide surface. We use this to locally add liquid crystals without compromising other functions on the silicon photonics chip (passive optics, high-speed modulators, and photodetectors) and we optimized the geometry to obtain an efficient EO tuner.

1.1. Liquid Crystal as an Electro-Optic Cladding

Liquid crystals are widely used for EO manipulation of light. The calamitic nematic phase of LC is an ordered state of rod-like molecules forming an anisotropic material that exhibits strong optical birefringence (e.g., $\Delta n = 0.2$ for the well-known E7 mixture [22]). The (average) optical axis of the rod-like molecules is referred to as the director $\vec{\mathbf{n}}$. LC can be used as an EO material in the cladding of a strip waveguide or slot waveguide (see **Figure 1a–d**). When no external electric field $\vec{\mathcal{E}} = -\vec{\nabla} V$ is present, $\vec{\mathbf{n}}$ aligns with the propagation direction of the waveguide along the *z*-axis (see Figure 1a).[14,20,21,23–25]

When $\vec{\mathcal{E}}$ exceeds a threshold value $\vec{\mathcal{E}}_t$ (corresponding to the threshold voltage V_t), the director $\vec{\mathbf{n}}$ starts to align with $\vec{\mathcal{E}}$. When the LC is incorporated as a cladding of a dielectric waveguide, this director change $\Delta\vec{\mathbf{n}}$ induces a change in the n_{eff} of the guided optical waveguide mode. This has been demonstrated in combination with silicon and silicon nitride waveguides, but the integration either requires a customized chip fabrication process,[26] or imposes limits on the phase shifter performance in terms of high drive voltage, long interaction lengths, or the need to use the TM polarization[20] (Figure 1b,c).

Many integrated silicon photonics platforms (such as the *iSiPP50G* platform from IMEC used here) typically use a thickness of 220 nm. Because the TM polarized waveguide modes are less confined, they are interesting to use in sensing applications as they have a stronger interaction with the waveguide cladding material, which can also beneficial to enhance electro-optic interactions. However, the lower confinement results in a required bend radius of 30 µm for low losses, as opposed to a 5 µm bend radius for the fundamental TE mode. For this reason, the TE polarization is widely used for large scale integrated silicon photonic circuits, as they can be made with a much smaller footprint. As a consequence, most components have been optimized for the TE polarization, and for this reason it is preferred to have a phase shifter that is highly compatible with fundamental TE mode of a standard strip waveguide in such a platform. Because TE-TM polarization converters would increase the insertion loss and the device length, a phase shifter operating on a TE mode is preferred.[27–30]

One way to increase the overlap with the director rotation without resorting to the TM polarization relies on a slot waveguide geometry. A slot waveguide filled with LC can achieve strong phase shifts with a TE polarized mode, however similar problems arise with mode converters (transitions) from a conventional strip waveguide to the slot mode and vice versa. Furthermore, narrow slots have increased sidewall roughness interacting with the strong field discontinuities that increase propagation losses. Both the transitions and the narrow slot are challenging to fabricate with large scale deep UV–lithography techniques[14,24,31] (Figure 1d).

In earlier demonstrations the LC cladding usually covers the entire chip surface. Recently, we explored a phase shifter geometry (Figure 1e) where LC could be integrated in IMEC's iSiPP50G silicon photonics platform,[21] using localized deposition with inkjet printing.

Based on these preliminary results, we propose a new phase shifter design with two doped silicon electrodes (called rails) in close proximity to the waveguide, allowing efficient actuation of the LC, with a high spatial overlap with the TE polarized waveguide mode (see Figure 1f). We refer to this geometry as a "dual-rail waveguide." Because in this "dual-rail waveguide" the optical TE polarized mode remains confined in the waveguide core, the mode conversion is fundamentally less abrupt. This

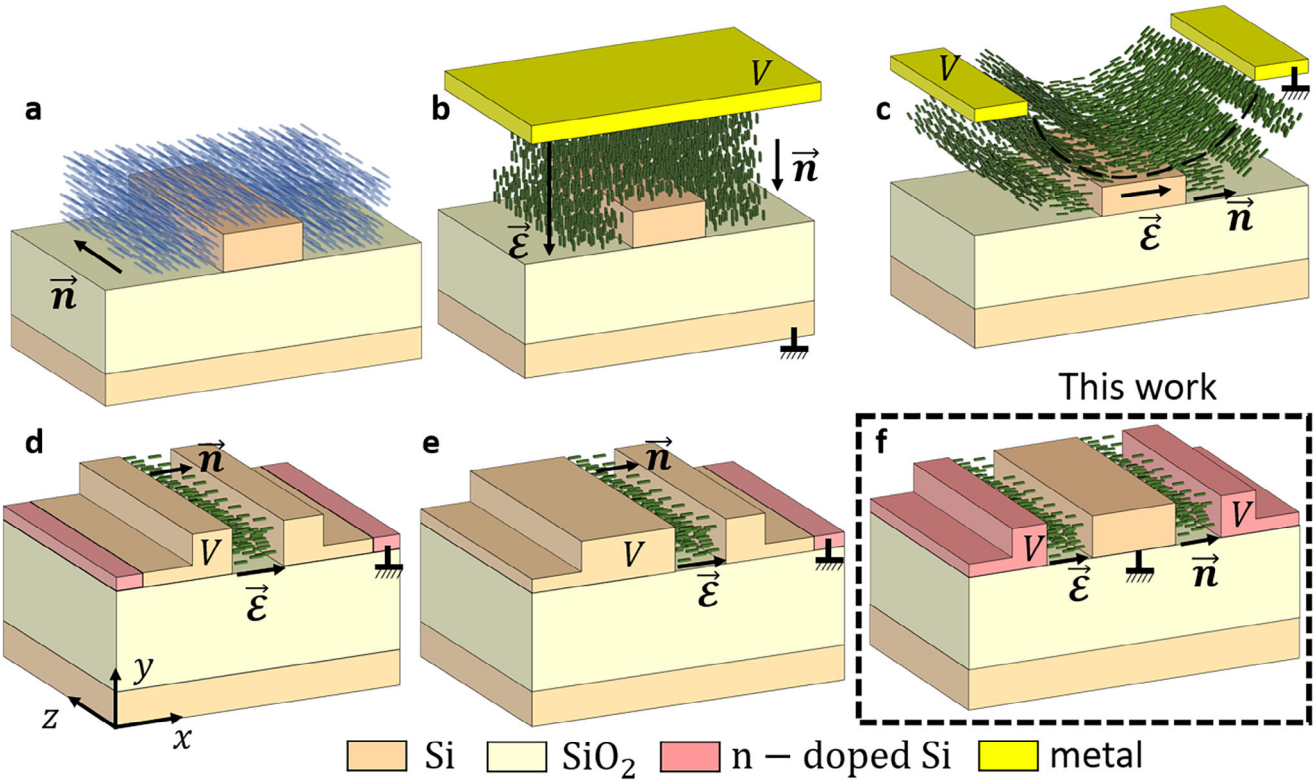

Figure 1. a) A strip waveguide with an upper LC cladding. The director $\vec{n}$ indicates the average orientation of the nematic LC molecules. In absence of an external field, $\vec{n}$ aligns with the longitudinal direction of the waveguide. b) Vertical actuation using a top and bottom electrode (i.e., grounded substrate) to apply a vertically oriented electric field $\vec{\mathcal{E}}$. c) In-plane switching using distant lateral electrodes to generate a quasi-horizontal field $\vec{\mathcal{E}}$. d) Slot waveguide actuation creates a stronger electric field $\vec{\mathcal{E}}$, thanks to the small distance between the rails. The high overlap with the LC and the guided slot mode yields a strong EO effect, but the slot waveguides and transitions can induce high propagation losses. e) To avoid the transition slot waveguide, one rail can be implemented as a strip waveguide, enabling localized electrical fields and reducing optical losses. f) In this work we demonstrate a new geometry where a strip waveguide is accompanied by two doped silicon rails serving as an electrode. The dual-rail geometry allows for a stronger EO effect compared to the single rail.

means the transition from a conventional strip waveguide to the proposed phase shifter can be short, has relaxed fabrication requirements and has a low insertion loss. Furthermore, the dual-rail waveguide has limited propagation losses even with doped side-rails due to the lower overlap with these side-rails compared to the slot waveguide. This means the driving frequency can be vastly increased to eliminate unwanted phase flickering effects. The rails provide a modest slot enhancement in the adjacent gaps, but without the excessive losses of a traditional slot waveguide, as sidewall roughness in the gaps is less pronounced compared to the narrower slot. The demonstrated dual-rail waveguide phase shifter design has a strong EO phase shift for low voltages, and allows for a new direct digital driving scheme with 3 V square waves.

2. Dual-Rail Waveguide Phase Shifter: Device Concept and Simulation

The dual-rail waveguide is shown in **Figure** 2a,b. The TE polarized mode profile in Figure 2c shows that the dual-rail waveguide geometry confines most light in the rectangular waveguide core but still provides strong electric fields $\vec{\mathcal{E}}$ in the gaps by using the waveguide core as a ground contact. The rails increase the evanescent TE electric field (E_x) component in the gaps (this is explained in detail in ref. [21]). When $\vec{\mathcal{E}} < \vec{\mathcal{E}}_t$, the director $\vec{\mathbf{n}}$ is oriented parallel to the waveguide (i.e., $\theta = 0$ in Figure 2a). When the voltage ($> V_t$) on each rail rises, $\vec{\mathbf{n}}$ rotates increasingly toward the x-axis (i.e., θ increases when $\vec{\mathcal{E}}$ ($> \vec{\mathcal{E}}_t$) is elevated in each gap), resulting in $\Delta\vec{\mathbf{n}}$ (see Figure 2a,b). Figure 2b illustrates the maximum $\Delta\vec{\mathbf{n}}$ (i.e., $\vec{\mathbf{n}}$ is parallel with $\vec{\mathcal{E}}$ in the x-direction, $\theta = \frac{\pi}{2}$). $\Delta\vec{\mathbf{n}}$ interacts mostly with the E_x-component of the waveguide mode (see Figure 2b,c): E_x interacts with an increasing refractive index in the gaps (from n_o toward n_e of the LC), resulting in a significant change in n_{eff}.

The director change is actually non-uniform (as $\vec{\mathcal{E}}$ is non-uniform). A 2D finite-element method (see Supporting Information Sections S2 and S3) determines the Q-tensor and extracts the spatial distribution of $\vec{\mathbf{n}}$ for a certain voltage (see Figure 2d).[32–36] This spatial distribution is combined with a 2D anisotropic mode-solver[37] to obtain EO response curves (Figure 2e) (see supplemental document section S4). These simulations indicate $V_t \approx 1$ V and saturation around 6 V. As expected, a narrower waveguide core ($w_{\text{core}} = 350$ nm) has a stronger effect, as there is decreased confinement of the optical mode.

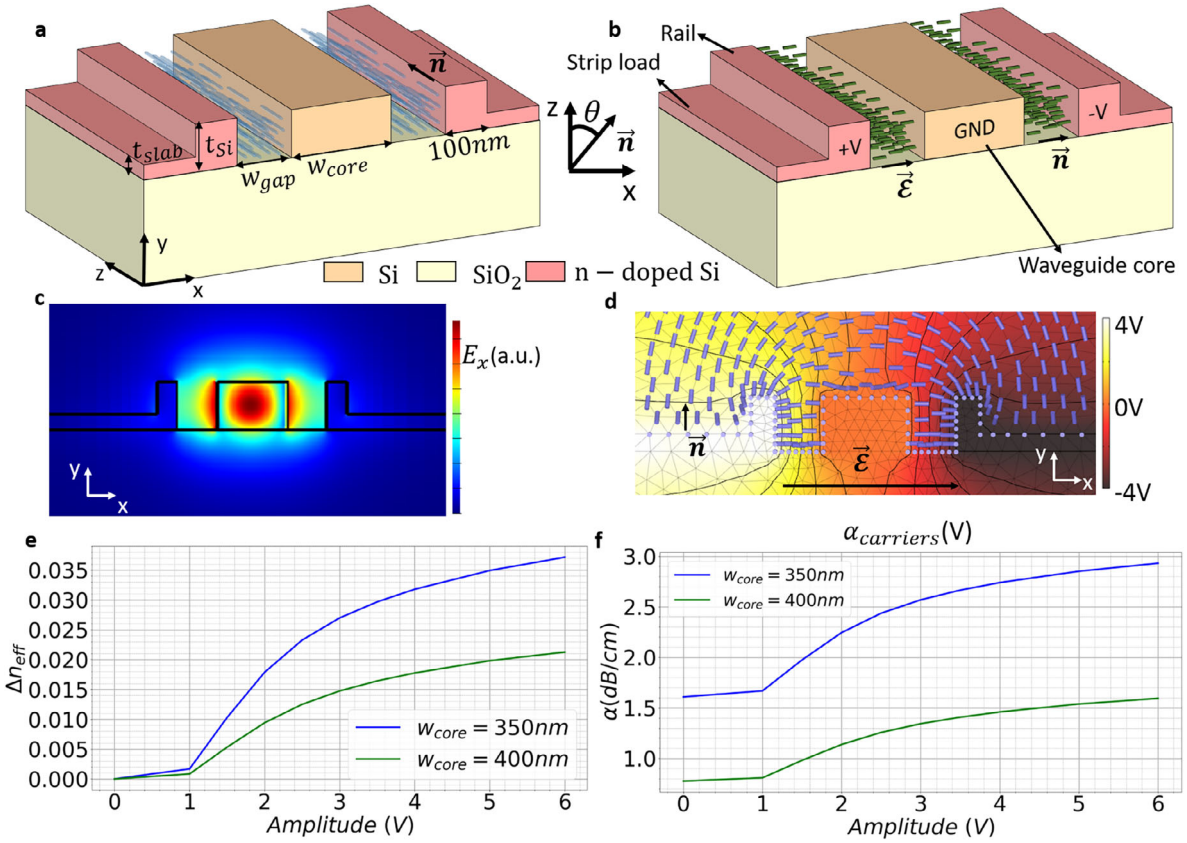

Figure 2. a) Concept of the dual-rail waveguide without voltage over the gaps. Two strip-loaded doped silicon electrodes accompany a single-mode waveguide with a high-resistivity connection to the ground. The LC aligns along the propagation direction in the waveguide. b) When a voltage is applied over the gaps, the director ($\vec{n}$) in the gap aligns with the electric fields. This changes the effective index of the propagating mode. c) Electric field distribution (E_x) of the optical mode. d) FEM simulation of director distribution in the LC cladding with ± 4 V between electrode structures and the waveguide (see Supporting Information Sections S2– S4). e) Δn_{eff} obtained by combining the director distribution with an anisotropic mode solver (see Supporting Information Section S4). **f** Propagation loss attributed to carrier absorption α_{carrier} (see Supporting Information Section S6B).

The mode plot in Figure 2c shows a small non-zero magnitude of E_x inside the side-rails (indicated by a lighter blue hue). As the director rotates, the confinement of the optical mode in the waveguide core decreases. This means that the non-zero overlap of E_x with the rails increases with higher voltages (similar to ref. [21]). This increases the carrier absorption of the optical modes due to the doping in the rails. The propagation losses due to carrier absorption effects in these doped side-rails are estimated with charge transport simulations[38] (see Supporting Information Sections S5 and S6). The optical propagation losses caused by carrier absorption in the side-rails depend on the director orientation in the xz-plane θ (and consequently on the voltage), which is notated here as $\alpha_{\text{carrier}}(\theta)$. The simulations indicate that $\alpha_{\text{carrier}}(\theta)$ ranges between $\alpha_{\text{carrier}}(\theta = 0) \approx 1.6\,\text{dB cm}^{-1}$ (Figure 2a) to $\alpha_{\text{carrier}}(\theta = \pi/2) \approx 3.22\,\text{dB cm}^{-1}$ (Figure 2b) with ($w_{\text{core}} = 350\,\text{nm}$). Increasing the w_{core} significantly improves the insertion loss, as the overlap with the rails decreases: $\alpha_{\text{carrier}}(\theta = 0) \approx 0.79\,\text{dB cm}^{-1}$ and $\alpha_{\text{carrier}}(\theta = \pi/2) \approx 2.01\,\text{dB cm}^{-1}$ for $w_{\text{core}} = 400\,\text{nm}$. The change in n_{eff} (i.e. by increasing the voltage, realizing a director rotation of θ) corresponds to an increase of $\alpha_{\text{carrier}}(V)$ shown in Figure 2f (see Supporting Information Section S6). These simulations also show that the changes in carrier concentration in the rails (injection/depletion) have no significant impact on n_{eff} of the propagating mode and a limited effect on its α: $\Delta\alpha < 0.01\,\text{dB cm}^{-1}$. Scattering losses (induced by either the LC or surface roughness) are not considered, but should exhibit a similar trend since the interaction of the optical waveguide mode with sidewall surfaces and the LC increases with larger voltages.

The analysis of the carrier absorption losses shows this cross-section has a clear advantage over slot waveguides. The overlap with the side-rails is much smaller compared to slot-waveguide implementations.[14,24] This means the side-rail electrodes can be doped, lowering the resistance and increasing the cut-off frequency. As will be discussed later this is beneficial for the elimination of phase flicker. Furthermore, the mode profile is similar to the mode-profile of a conventional strip waveguide as the mode remains guided by the central waveguide core. This means the transitions from a regular strip waveguide to the dual-rail geometry fundamentally exhibit lower insertion losses and are easier to fabricate with deep UV lithography. Furthermore, narrow slots typically have more side-wall roughness contributing to higher propagation losses. The dual-rail cross-section has a smaller overlap with the LC compared to slot waveguides, resulting in a smaller tuning range (a theoretical Δn_{eff} of 0.05 is reported in ref. [24] using the same LC parameters). However, this

cross-section still reaches a theoretically obtainable Δn_{eff} of 0.035 for $w_{\text{core}} = 350\,\text{nm}$.

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The charge transport simulations also provide an estimate for the capacitance of the cross-section, and how it changes when the director rotates ($c(\theta)$). The capacitance of the 200 nm gap is found to be $c(\theta = 0) \approx \frac{\Delta q}{\Delta V} \approx 114.2\frac{pF}{m}$, $c(\theta = \pi/2) \approx 404.8\frac{pF}{m}$ (see Supporting Information Section S7).

The opposing voltage polarity on the rails introduces two benefits: increased uniformity of $\vec{\mathbf{n}}$ in the modal area (see Figure 2c,d and Section S3 and Figures S5 and S6, Supporting Information) and opposing carrier dynamics on each side (i.e., injection vs depletion, see Supporting Information Section S5). The uniform $\vec{\mathbf{n}}$ also reduces scattering losses in the LC.

3. Experimental Section

3.1. Simulation

The charge simulations as described in Supporting Information Section S5 are implemented in *Ansys Lumerical CHARGE* software. The mode simulations to assess the influence of the carriers on n_{eff} are carried out in *Ansys Lumerical MODE* (see Supporting Information Section S6) and use discrete sections of uniform director orientation. The in- and output crossings of the rim are simulated in *Ansys Lumerical MODE*. The in- and output tapers of the side-rails based on circular bends are simulated in *Ansys Lumerical FDTD* (see Supporting Information Section S12).

The spatial variation of $\vec{n}$ with a given voltage is obtained with a dynamic Q-tensor simulation (as described in the Supporting Information Sections S2 and S3). The FEM to solve the Q-tensor is implemented in *Matlab* and the triangular mesh is generated with *GiD Simulation* software. The anisotropic mode solver as described in the Supporting Information Section S4 is implemented with a FEM in *Matlab* with a triangular mesh generated with *GiD Simulation*. This simulation employs the obtained director distribution from the Q-tensor simulations.

3.2. Fabrication

The devices are fabricated on IMEC's iSiPP50G silicon photonics platform.[39] The final process module (EXPO) in this platform is an option to locally remove the top oxide cladding of the silicon waveguides (i.e., to implement waveguide sensor devices). After this *EXPO*-step, a thin layer of 5 nm of oxide remains on top of the silicon waveguides. Then a timed buffered HF etch is used to remove the remaining oxide and clear the gaps (i.e., sidewalls) of the waveguide, exposing them to air (similar to the steps described in ref. [40], but without subsequently under-etching the structures). After the buffered HF etch, a *Dimatix DMP-2850* inkjet printer is used to deposit the LC[21,41] in the etched recess of the device, creating a localized upper cladding with LC. The resulting cross-section of the dual-rail waveguide is presented in **Figure 3**a.

The printer cartridge is filled with a commercially available *E7* LC mixture. To ensure proper droplet formation when printing, the LC in the print head is heated to 65 °C, above the clearing temperature (T_c = 58 °C). The volume of a single phase shifter cavity in this work is ≈ 40 pL when $L = 100\,\mu\text{m}$ (or 80 pL for the devices with $L = 200\,\mu\text{m}$), and the printer dispenses droplets as small as 2.4 pL.

After inkjet printing, the device is checked under a microscope with a polarization filter to confirm the LC deposition in the gaps (see Figure 3b,c). As there is no alignment layer, random domains are formed (Si and SiO_2 surfaces induce weak planar alignment of $\vec{n}$ with no in-plane preference). However, close to the devices there is a tendency for $\vec{n}$ to align along the corners in the device geometry.[23] This can be intuitively understood by considering the tendency for planar alignment on two orthogonal surfaces. As the director energetically favores alignment to both planes, the optimal orientation follows the intersection of the two anchoring surfaces, i.e., the corners present in the geometry. The dual-rail geometry has 12 aligning edges, compared to 4 edges in the case of a regular strip waveguide and 8 edges in the case of slot waveguides. This principle was also used in ref. [42], where etched groove arrays were used to control the alignment of an integrated LC cladding.

Figure 3d shows the on-chip MZI-circuit, embedded in the measurement setup. The MZI circuit is also indicated on the microscope image shown in Figure 3b. The MZI circuit employs two 50/50 splitters (based on multi-mode interferometers (MMI). One arm has both an extra section ΔL of standard strip waveguide ($450nm \times 220nm$) and the phase shifter as device under test (DUT) compared to the reference arm.

3.3. Measurements of the Dual-Rail Waveguide Phase Shifter

To characterize a phase shifter, the setup as illustrated in Figure 3b is constructed with a *Santec TSL-510-A-510630* tunable laser. The laser light is sent through a *Thorlabs FPC562* manual polarization controller with paddles. A *Newport 2936-C* optical power meter with a *Newport 818-IG/DB* photodiode is used. For the electronic signals, a *Tektronix AFG3102* is used to generate a square wave on each of the two outputs, with phase locking. Three separate DC probes are used to manually contact the bond pads on the chip, with BNC-splitters from the function generator to the probes as shown in Figure 3d.

A 200 kHz square wave is used on each output (locked in phase), where either the amplitude A or the phase delay ζ between the square waves is actuated. The frequency is high compared to conventional LC applications. This frequency is chosen to minimize phase flicker, as is elaborated in Section 4.1.1. To extract the EO response, all devices are connected to a computer with a GPIB or USB connection, and a python script triggers a wavelength sweep procedure on the *Santec* laser, which has a trigger connection to the *Newport* power meter with a coax cable to enable fast sweeping. The wavelength resolution in this sweep procedure is set to be 5 pm. The script sets a 200 kHz square wave with equal amplitude ($A_1 = A_2 = A$) on both outputs of the function generator ranging from 100 mV to 10 V, and performs a wavelength sweep for each 100 mV step in amplitude. For the amplitude sweep the phase delay between the two square waves (ζ) is set to be 180°. A similar measurement procedure is performed by activating a wavelength sweep for two square waves with 3.0 V amplitude but increasing ζ from 0 ° to 180 ° in 10 ° steps.

3.4. Data Extraction from the MZI Spectra

The phase shift is extracted from the measured MZI spectra by obtaining the free spectral range, *FSR*, with *Scipy*'s *findpeaks* function, which can then be used to obtain the phase shift from the resonance shift:

$$\Delta\phi(\pi) = \frac{2 * \Delta\lambda_{\text{peak}}}{FSR} \tag{1}$$

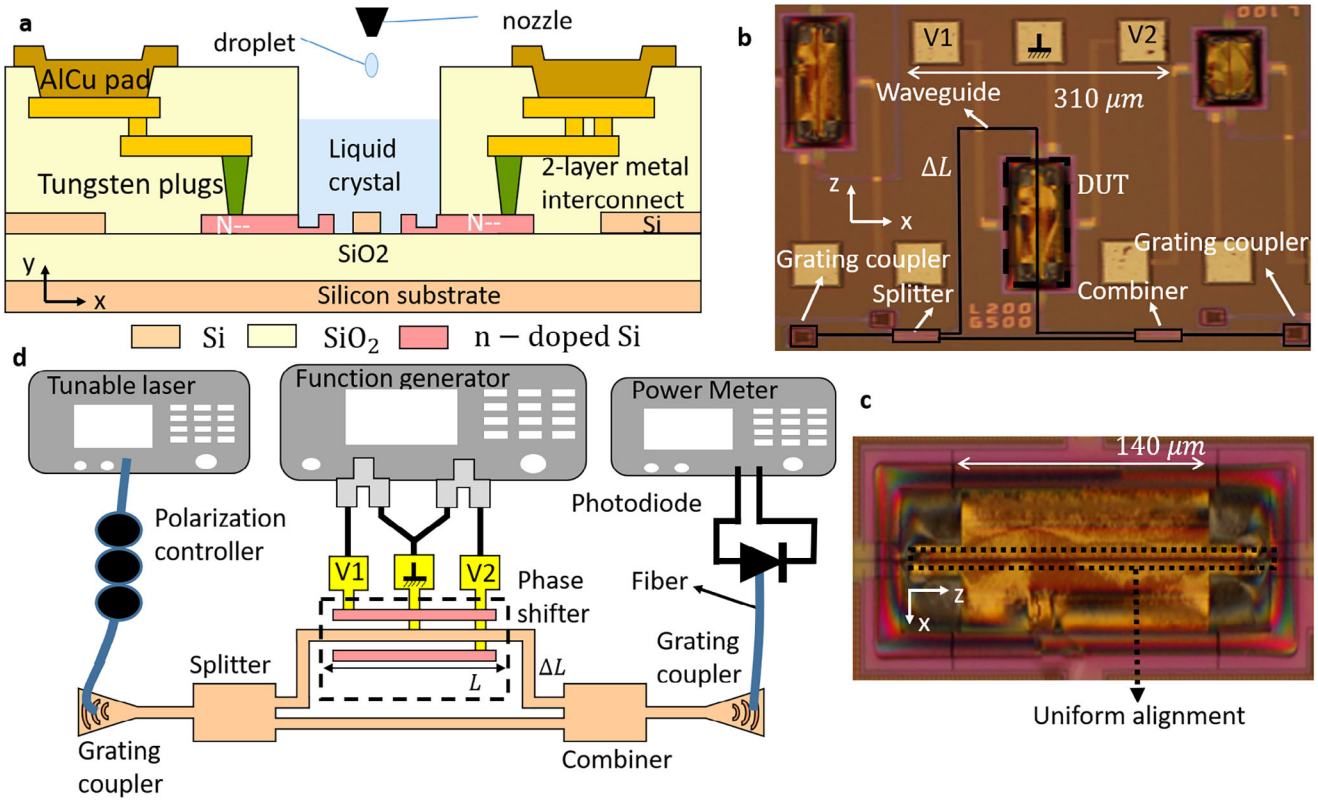

Figure 3. a) Inkjet printing is used to deposit the LC locally in a recess on the chip. b) Microscope image of deposited LC, analyzed with a polarization filter. The MZI circuit is indicated on top of the image. c) Detail of a single device. The polarization filter indicates random domain formation, but a dark line indicates a well-defined orientation near the waveguide along the *z*-axis. d) schematic of the measurement setup to characterize the EO phase shift with the help of an on-chip Mach–Zehnder interferometer (MZI) with a designed delay length $\Delta L = 176,488\,\mu m$ (or $\Delta L = 276,488\,\mu m$ when the PS is 200 µm long). Light is coupled from and to the chip using grating couplers and electrical contact is made with DC probes.

To extract the insertion loss, the transfer function of the MZI is fit to the measured data points:

$$T(\lambda) = 10\log\left[\frac{1}{4}\left|1+\exp\left(-i.\frac{2\pi(\lambda-\lambda_{peak})}{FSR}-\frac{IL_{tot}\ln(10)}{20}\right)\right|^2\right]+O \quad (2)$$

The earlier obtained *FSR* is used as an input in Equation (2). The offset *O* is determined in a straightforward procedure, normalizing the data to exhibit a 0 dB peak value. The remaining parameter, IL_{tot}, is determined with *Scipy*'s *curvefit* function. If the splitters and combiners are assumed to have an ideal splitting ratio of 50–50, IL_{tot} corresponds to the total extra loss in the arm with the phase shifter device. This includes both the IL of the PS and the propagation loss of $\Delta L \approx 300\,\mu m$ (i.e., the extra waveguide sections with oxide cladding): $IL_{tot} = IL_{\Delta L} + IL_{PS}$. $IL_{\Delta L}$ was estimated to be 0.042 dB ($\alpha_{\Delta L} = 1.4\,dB\,cm^{-1}$). The measured spectra contain several peaks, each with a different extinction ratio (ER). $IL_{PS} = IL_{tot} - 0.042\,dB$ is extracted for each peak, resulting in a range of possible values.

4. Results and Discussion

4.1. Dual-Rail Waveguide Phase Shifter

4.1.1. Equivalent Electrical Circuit: Frequency Response and Power Consumption

The full 3D design of the device is shown in **Figure** 4a. The phase shifter rails are actuated with an alternating voltage with an average of 0 V, to limit ion drift in the LC that can cause charge screening effects.[21,43,44] Typically LC technology is actuated with square waves, which have a higher root mean square (RMS) voltage than sinusoidal waves and can be generated directly by digital electronics. The dual-rail setup is characterized with two separate square waves with equal amplitude *A* and a controlled electronic phase offset ζ, see Figure 4b. From the full 3D design we can calculate an equivalent distributed RC-ladder circuit with the simulated capacitances of the gaps and a resistivity estimate of the undoped silicon combined with measured sheet resistances (see supplemental document sections S7,S8 and S9). This distributed circuit is simplified with a first order lumped approximation, and simulated in *LTspice* (see Section S10, and Figures S18– S20, Supporting Information). When both square waves are in phase ($\zeta = 0°$) both rails are always on the same potential, and the high resistance of the undoped waveguide core limits the cut-off frequency. The first-order lumped circuit has a cut-off frequency $f_{c0} \approx 24\,kHz$. When the driving signals have opposite phase ($\zeta = 180°$) the field between the rails is maximal. The lower resistance of the doped silicon rails results in a much higher cut-off frequency $f_{c\pi} \approx 6.6\,GHz$ (in reality, $f_{c\pi}$ is much lower due to parasitic capacitance of metal interconnects and bondpads). An analysis of the director dynamics (Supporting Information Section S11) demonstrates an operational frequency of 200 kHz, much higher than f_{c0}, is

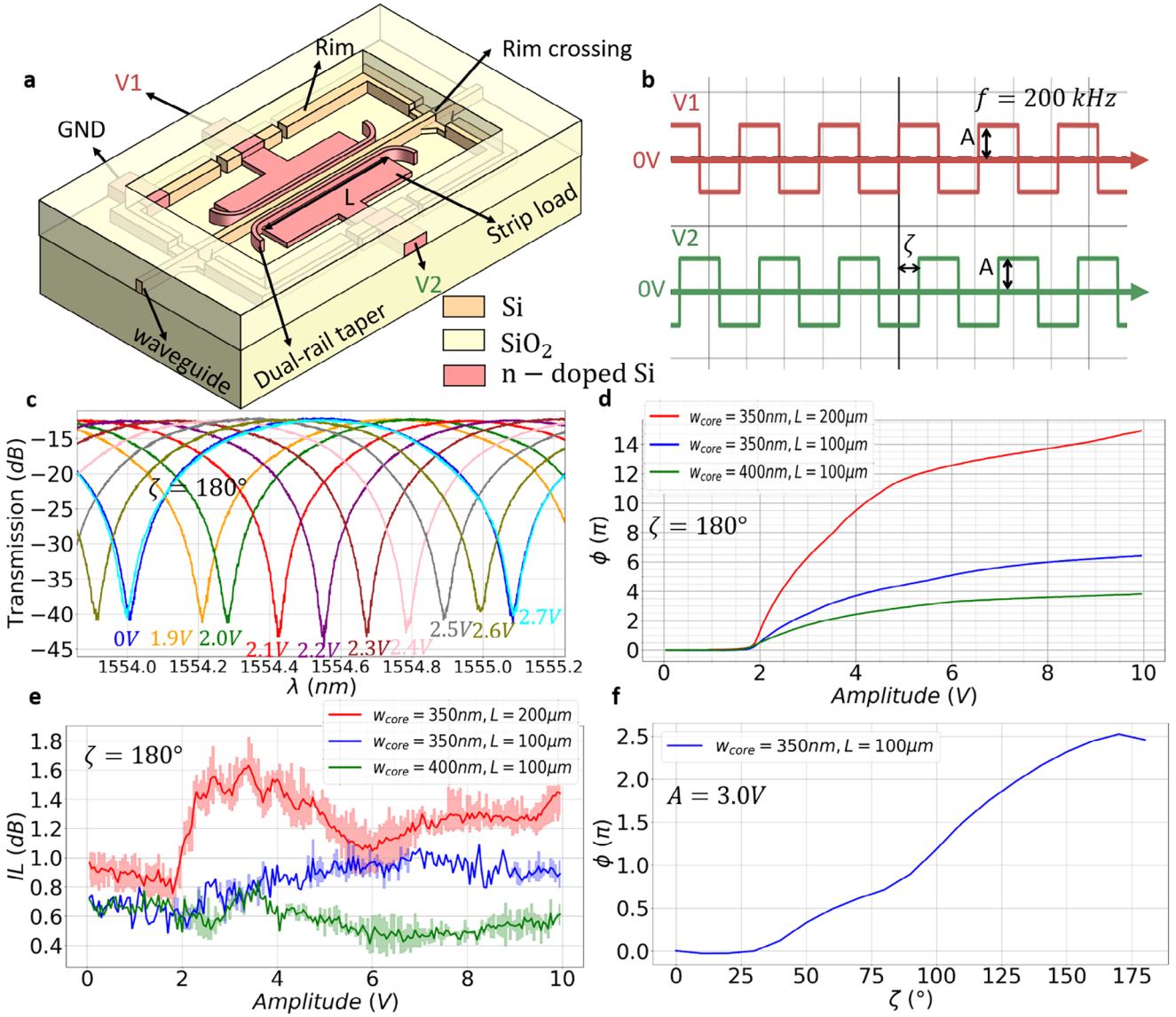

Figure 4. a) Geometry of the dual-rail waveguide. The silicon rim is used to stop the etch to clear the waveguide side walls. The waveguide core is electrically contacted with this rim, resulting in a high resistivity connection to the ground. From this geometry, an equivalent circuit model can be obtained (see Supporting Information Sections S7– S10). b) The voltage signals used to actuate the phase shifter. The frequency of 200 kHz avoids phase flicker due to elastic wiggling and ion drift (see Supporting Information Sections S10 and S11). In the device characterization, both voltage signals have an equal amplitude *A*. c) Examples of the obtained MZI spectra for the device with $w_{core} = 350$ nm and $L = 100$ µm and with $\zeta = 180°$. d) Extracted optical phase shift for different device geometries with increasing amplitude and $\zeta = 180°$. e) Extracted insertion loss for different device geometries with increasing amplitude and $\zeta = 180°$. f) Extracted phase shift for $w_{core} = 350$ nm and $L = 100$ µm with variable ζ and $A = 3.0$ V.

sufficient to suppress phase flicker.[45] The E7 LC compound used here has a specific frequency response: the dielectric anisotropy $\Delta\varepsilon$ decreases with increasing frequency (i.e. $\Delta\varepsilon \approx 14.5$ at 10 kHz, $\Delta\varepsilon \approx 12$ at 200 kHz and $\Delta\varepsilon \approx 0$ at 1MHz[46,47]). The frequency of 200 kHz minimizes phase flicker while maintaining a respectable $\Delta\varepsilon$.

The simulations of the first order lumped circuit model gives an indication of the expected power consumption: $P_{active} = 9.68$ nW, $P_{reactive} = 11.2$ nW ($\zeta = 0°$, $f = 200$ kHz), $P_{active} = 246.4$fW, $P_{reactive} = 28.6$ nW ($\zeta = 180°, f = 200$ kHz).

4.1.2. Electro-Optic Response of the Devices

The square waves (V_1 and V_2, see Figure 4b), have two degrees of control: the amplitude of both waves, and their phase offset ζ ($A_1 = A_2 = A$ to maintain a zero time-averaged voltage over both gaps). In Figure 4c, the MZI transmission for different amplitudes A (with $\zeta = 180°$) is shown for the device with $w_{core} = 350$ nm. We observe no phase flicker, which becomes apparent as a ripple on the spectrum (phase flicker was a considerable problem in our earlier non-optimized devices[21]). From the

MZI-spectra the EO response in Figure 4d can be obtained (see Section 3.4). We observe a higher threshold voltage V_t compared to simulations, which is attributed to the loss of higher harmonics of the square waves beyond the cut-off frequency of the equivalent circuit, resulting in a lower RMS voltage (as observed in measurements). The decrease of $\Delta\varepsilon$ at 200 kHz also contributes to an increase of V_t.[47] The EO curves shown in Figure 4d show a phase shift of 2π at 2.7 V, going up to 6π at 10 V for the device with a core width of 350 nm. A more modest phase shift can be noticed in a wider core of 400 nm, going up to 4π at 10 V.

4.1.3. Insertion Loss and Estimation of the Scattering Losses

Figure 4e shows the IL for each device which are extracted by fitting the transfer function of the MZI response as described in section 3.4. The IL is similar for both waveguide cores (around 0.7 dB) and increases to 1 dB for higher voltages for the narrow waveguide core of 350 nm. The longer device obviously has a higher insertion loss attributed to the extra device length. The narrower waveguide has a stronger overlap with side-walls and the LC cladding, leading to higher scattering losses.

To estimate the scattering losses in the phase shifter, the insertion loss of the device can be split up per contribution, i.e., the crossing of the rim and the tapering of the side-rail electrodes (as indicated in Figure 4a). An analysis is made for the device with the narrowest core (i.e., 350 nm) and a length of 100 µm. The insertion loss change from an oxide upper cladding to the LC cladding is minimized by using a rib waveguide. The adjacent silicon slabs confine the mode minimizing the overlap with the upper cladding. Eigenmode expansion simulations indicate that the total insertion loss for crossing the rim (which includes the change in upper cladding and the in- and output rib-strip waveguide tapers) is ≈0.18 dB (see Supporting Information Section S12). This loss is actually dominated by reflections occurring in the short rib-to-strip waveguide taper exiting the rim surrounding the device (as evidenced by the field monitor in the simulation, see Supporting Information Section S12). After the rim section, the narrow waveguide core is tapered into the dual-rail waveguide geometry by bending the electrode rails simultaneously from each side. Because there is a strong overlap between the input and output mode, this tapering introduces virtually no insertion loss (FDTD simulations indicate an IL <0.01 dB, see Supporting Information Section S12). Furthermore, the carriers in the doped side-rails have a limited contribution to the loss as discussed in section 2: 0.03 dB over a length of 100 µn. Using the extracted IL values for this device range between 0.6 dB and 1 dB (see Figure 4 e). Since all transition losses and the estimated propagation losses attributed to carrier absorption amount to 0.4 dB, the scattering losses of the device without voltage are 0.3 dB before threshold. With this value, a scattering loss of the phase shifter can be estimated $\alpha_{\text{scattering}} \approx 30\,\text{dB cm}^{-1}$ before threshold, going up to $\alpha_{\text{scattering}} \approx 60\,\text{dB cm}^{-1}$ with increasing voltage (see Supporting Information Section S12). This increase can be attributed both to the decrease in confinement when the voltage increases (i.e., the mode interacts more with the LC cladding and the sidewall roughness) and non-uniformity in the surrounding LC cladding (which will be most pronounced in the fringe fields of the input and output tapers).

4.1.4. Digital Drive Scheme

This device architecture enables a unique driving scheme based on the time delay between two square waves with constant amplitude. Above f_{c0}, the phase shifter will not respond for $\zeta = 0°$. This enables the electrical phase offset ζ (with fixed amplitude $A = 3.0\,\text{V}$) to tune the optical phase shift, see Figure 4b,f. The 100 µm long device with narrowest gap can tune between $\phi = 0$ and $\phi = 2.5\pi$. As indicated in Figure 4c, an amplitude $A = 2.7\,\text{V}$ would suffice to cover a full 2π tuning range. This is an attractive driving method, as it doesn't require a digital-to-analog converter. The digital drive signals can be generated directly from a microcontroller or FPGA.

4.2. Comparison with Other Implementations

For the phase shifter with $w_{\text{core}} = 350$ nm and $L = 100\,\mu\text{m}$, we find $V_\pi L = 0.0714\,\text{V mm}$. The device has a threshold voltage of 2 V as can be seen in the EO curves shown in Figure 4d. The $V_\pi L$ is calculated by obtaining the differential phase shift ($\frac{\delta\phi}{\delta V}$) of the EO response at the voltage with the highest modulation efficiency (see supplemental document section S13). There are insufficient data points to make an accurate statement on the propagation loss α (we only obtain the total IL of each device). However, the scattering losses are estimated to range between 3 and 6 dB mm^{-1}. $V_\pi L$ is more often used for fast modulators and the metric for phase tuners is more often the maximum Δn_{eff} at a given voltage. Together with reported device lengths, IL and power consumption this provides a framework to situate the results in the field, see **Table 1** and Supporting Information Section S14.

The LC-based devices require the lowest voltages. The work presented here has a smaller phase shift compared to the slot waveguide-based devices[14,24] (as is expected), but has a lower insertion loss. In the work of Xing et al.[24] the same LC (E7) is used, and a $V_\pi L$ of 0.0224 V mm is reported. In [14] has a $V_\pi L$ of 0.06 V mm is reported. The dual-rail geometry has relaxed fabrication requirements and avoids the lossy strip-to-slot transitions (the overlap of the dual-rail waveguide mode with a conventional strip waveguide is large). Furthermore, the side-rails can be doped without introducing excess carrier absorption losses, increasing the cut-off frequency of the drive voltage to reduce phase flicker. The dual-rail waveguide phase shifter still achieves 62% of the Δn_{eff} from the slot waveguide demonstrated by Xing et al. at 5 V.

The work from Notaros *et al.* has a lower Δn_{eff}, but was implemented on a custom-developed SiN platform and operates at a shorter wavelength $\lambda = 632.8$ nm, which gives a higher phase shift for a given Δn_{eff} (as $\Delta\phi = 2\pi\Delta n_{\text{eff}} L/\lambda$).

Thermo-optic phase shifters can be low voltage, have limited IL and short device length but the power consumption is in the order of several mW (even with optimization strategies such as undercutting the heater for thermal isolation).[48] The MEMS-based phase shifter have a low power consumption, device length and power consumption but require larger voltages ($V_\pi = 10.7^{+2.2}_{-1.4}$).[40] The PCM based phase shifters have the strongest index change, and are non-volatile which logically lowers the power consumption. But voltages of 21 V are re-

Table 1. Comparison of different phase shifter technologies.

	Voltage	max Δn_{eff}	Device length	IL	Power consumption
Liquid Crystal					
Xing et al.[24]	4.25 V	0.0558	1 mm	10 ± 1 dB	<2 nW
Notaros et al.[c)][26]	2.4 V	0.0259	500 µm	0.5 dB(1 $\frac{dB}{mm}$ [d)])	–[e)]
This work	10 V(5 V[a)])	0.05(0.035[a)])	100 µm	0.6 – 1.0 dB	246.4 fW[b)] ($\zeta = 180°$)
Other type					
Edinger et al. (MEMS) [40]	35 V	0.04495	50 µm	$0.33^{+0.15}_{-0.10}$ dB	< 1 µW
Rios et al.[f)] (PCM) [16]	6.2 V(21.0 V)	0.07	12 µm	0.5 dB	38.4µJ (176 nJ)
Parra et al.[g)] (thermo-optic) [48]	–	–	40 µm-1000 µm	0.5 dB–20 dB	0.5 mW–25 mW

[a)] The index change for 5 V is reported because at higher voltages the effective device length increases (>100 µm). This happens as the fringe fields on the in- and output transitions realize an extra phase shift at higher voltages. The Δn_{eff} at 5 V is in good agreement with simulations. [b)] This value is based on modeling and not directly measured. When the phase between the two applied square waves changes power consumption increases, with a maximum value of 9.68 nW ($\zeta = 0°$) [c)] This work is demonstrated on a SiN platform, and uses a wavelength of 632.8 nm. All other mentioned publications are demonstrated on SOI platforms with a wavelength of 1550 nm. [d)] The publication only mentions the propagation loss. The loss of the transitions is not specified, we calculated the total insertion loss based on the reported propagation loss and device length. [e)] No mentioned value of power consumption in this work. [f)] Since this actuation mechanism is non-volatile switching between an amorphous and crystalline state of the PCM, both the pulse voltage and power consumption are mentioned for total crystallization (amorphisation) of the reported PCM. [g)] Review paper summarizing different thermo-optic phase shifter implementations. Voltages and Δn_{eff} are not reported.

quired, resulting in a similar limitation compared to the MEMS devices.[16]

The device presented in this work is the first demonstration of a phase shifter that has all the required properties mentioned in the introduction. This phase shifter has a low power consumption due to the capacitive nature of the device and low insertion loss due to the new architecture presented here. The best performing phase shifter demonstrated in this work has a V_π of 2.2 V.

5. Conclusion

In this work dual-rail waveguide phase shifters based on liquid crystal actuation are presented. The best performing phase shifter realizes a phase shift of 2π at 2.7 V with an insertion loss around 0.6-0.8 dB over a length of 100 µm and an estimated power consumption in the order of 1 nW. This combination of metrics is unmatched by alternative technologies on SOI platforms at 1550 nm which either require higher voltages, exhibit larger insertion loss or consume more power. The unique properties of the dual-rail waveguide architecture allow for doped side-rails with low carrier absorption losses. This allows an increase in the drive frequency, eliminating phase flicker. The dual-rail waveguide allows for easy to fabricate in- and output tapers with limited insertion loss, and has a low propagation loss compared to slot waveguides.

The dual-rail waveguide cross-section enables a new purely digital driving scheme. This scheme relies on the phase difference between two square waves with equal and constant amplitude. The driving signals could be adapted such that the waveforms are directly generated by digital 3.3 V or 5 V transistor-to-transistor logic (TTL). In this case the waveguide core requires a half-way 1.85 V or 2.5 V potential to suppress ion drift.

With polymerizable LC mixtures,[49] these LC based electro-optic tuners can be extended to nonvolatile actuators for one-time correction (trimming) or one-time programmable chips.

The main impact of our demonstration is in large-scale photonic circuits that combine programmable passive functionality (connections, filters, linear transformations) with all other high-speed functions available in a silicon photonics platform. Localized inkjet-based deposition provides a high-throughput integration of LC that can be performed on wafer scale. The dual-rail phase shifter geometry circumvents the high losses of slot waveguides, while still providing close-proximity electrodes and a modest slot enhancement. Moreover, the dual electrodes make it possible to implement a unique driving mechanism based on pure digital electronics. There is still considerable room for improvements, by optimizing the device geometry for lower insertion losses, improving electrical characteristics, and using LC with stronger anisotropy. The alignment of the LC could be improved by adding more etched grooves to the design.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

inkjet printing, integrated photonics, liquid crystal, optical phase shifter, silicon photonics

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