Extended Methodology to Determine SRAM Write Margin in Resistance-Dominated Technology Node

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Abstract—**An extended write-ability methodology of static random-access memory (SRAM) in advanced technology nodes is proposed in this paper. Increased bitline (BL) resistance in sub-10nm node has hindered BL from fully discharge during a write operation. Furthermore, the write ability is degraded by an increased leakage current of half-selected bitcells on BL and BL capacitance operated in high frequency. In a realistic write operation, BL parasitics also cause 30% SRAM yield loss in interconnect resistance-dominated technology nodes. Thus, this proposed method analyzes the time-dependent impacts of BL parasitic resistors, capacitors, and pass-gate transistors on write margin considering the negative bitline (NBL) assist technique.**

Index Terms—**SRAM, write margin, negative bitline, bitline parasitics.**

I. Introduction

Continued geometric scaling of devices with advanced CMOS technology increases process variation and enhances driver strength of PMOS transistors [1-5]. These are becoming the major sources that degrade the write ability of static random-access memory (SRAM) [1]. To improve the write ability of SRAMs, circuit assist techniques such as negative bitline (NBL) have been introduced [1-4]. However, the write-ability enhancement with NBL is still limited by the rapidly increasing bitline resistance in sub-10nm technology nodes due to metal geometric scaling and surface scattering [4, 5]. The value of write driver voltage with NBL assist circuit can be controlled by a boosting capacitor (C_{boost}) [1]. As shown in Fig. 1, the NBL voltage requirement for a successful data flip is increased with larger R_{BL} and C_{BL}. Otherwise, an increased data flip time or write failure may incur. Note that a typical range for BL parasitic resistance (R_{BL}) and capacitance (C_{BL}) would be 10 to 100 Ω/cell and below 50aF/cell, respectively [5]. Therefore, R_{BL} of 20 and 40 Ω/cell, and C_{BL} of 25 and 50 aF/cell are taken as references in Fig. 1. The effects of BL parasitic circuits under NBL write process are also determined by the BL ramp-down speed. Thus, it is necessary to predict the time-dependent impact of BL parasitics on write operation by introducing a proper write margin methodology in deeply scaled nodes.

Several approaches have been reported to obtain static write margin of SRAM such as voltage transfer curves (VTC) [6], sweeping bitline (BL) [7] and wordline (WL) voltages [8, 9], and N-curve [10]. However, the assumption of infinite WL pulse width without considering time dependencies in the above approaches may underestimate write failures [11]. Hence, dynamic write margin analysis [12, 13] is proposed to include dynamic noise source, finite WL pulse width, and transient behaviors. However, the time-dependent effects of BL parasitic components caused by NBL technique have not yet been reported in the exiting write ability metrics using computer-based simulation [6-14]. Although these parasitics can indeed be neglected for less scaled nodes, their impacts on write margin with NBL assist technique are too significant to neglect in advanced resistance-dominated technology nodes. As the BL discharging procedure occurs during WL activation in a typical NBL process [2, 15], the write margin is determined by the impact of BL parasitics and SRAM operating speeds. Therefore, the conventional BL write margin (BLWM) [6, 7, 14] method is extended to capture the time-dependent BL parasitics effects in this paper. We demonstrate that the current flow from the internal nodes of the half-selected bitcells to BL through unintentionally activated pass-gate (PG) transistors, while BL is discharging, makes it difficult to flip the data and result in degraded write margin. In addition, at high-frequency operation, the write margin further deteriorates due to voltage drop on BL caused by parasitic capacitors.

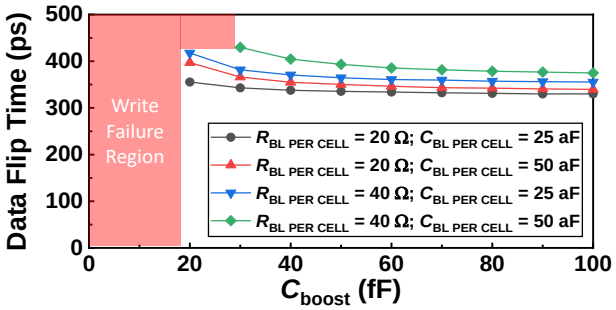

Fig. 1. Data flip time with varying C_{boost}, R_{BL}, and C_{BL} of HD SRAM designs for a typical NBL write operation. The requirement of NBL voltage (controlled by C_{boost}) for a successful data flip is increased with larger BL parasitics.

II. Proposed Write Margin Methodology

Fig. 2 illustrates a schematic view of 6-transistor (6T) SRAM bitcell with 2 pull-up (PU), 2 pass-gate (PG), and 2 pull-down (PD) transistors assuming 2 nm CMOS nanosheet (NS) transistor technology. The SRAM design rules using four-stacked nanosheet transistors are presented in Table I [16]. Table II lists the nanosheet width (W_{NS}) ratio (PU : PG : PD),

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BL and WL BEOL parasitic values extracted from the layout, and array configuration of high-density (HD) and high-performance (HP) SRAM design. HD SRAM features a W_{NS} ratio of 111 with 256-bit WL and BL. HP SRAM has a W_{NS} ratio of 122 with 256-bit WL and 128-bit BL [2-4]. The internal nodes in the SRAM bitcell Q and QB are initialized to store '1' and '0', respectively since the write driver is set to enable the BL path for applying negative voltage. The results would be the same with the opposite setting in symmetric SRAM.

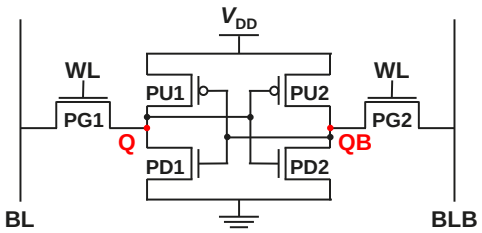

Fig. 2. Schematic view of 6T SRAM.

Table I. SRAM design rules in 2 nm node [16]

Parameters	Value (nm)
Gate Length	15
Metal Pitch	18
Contacted Poly Pitch	42
Nanosheet Width	11
Nanosheet Height	5

Table II. Nanosheet width (W_{NS}) ratio, BL and WL parasitics of 2nm NS SRAM layout, and array configuration of HD and HP Designs

Type	W_{NS} Ratio	R_{BL}/R_{WL} (Ω/cell)	C_{BL}/C_{WL} (aF/cell)	Configuration
HD	1:1:1	38/20	30/79	256 bits/WL; 256 bits/BL
HP	1:2:2	18/23	33/86	256 bits/WL; 128 bits/BL

During write operation, the BL voltage (V_{BL}) is pulled down to a lower voltage to write '0', and BLB is kept at the supply voltage (V_{DD}) of 0.7 V to write '1' while the WL is asserted to turn on the PG transistors. The tri-state inverters are used as a write driver (WD), and the voltage source for ramping BL down is connected to the write driver. The BL discharging starts when WL is activated to capture the NBL characteristics as reported in [2, 15]. To avoid write failure, the ramp-down time (t_{BL}) lasts for the entire WL enable period with a certain ramp-down slope (S_{BL} = -voltage/t_{BL}). S_{BL} of -2 V/ns is assumed in this work to represent an SRAM macro design of 2GHz operating frequency for write operation in a 2nm node technology. Note that 2GHz is applied by taking [2, 15] as reference. The write margin is defined as the maximum write driver voltage (V_{WD}) which confirms data flip when node '0' reaches 90% of its full swing, with the bitcell located furthest away from both WL driver and write driver (Fig. 3).

Both process and mismatch variations are carried out by Monte Carlo simulation in Cadence tools. Since the run time could be too time-consuming under complete memory and logic circuits, a dedicated circuit for write margin extraction is designed. The simulation circuit includes timing control, the last stage buffer of row decoder, transmission gate, write driver, WL and BL parasitic circuits, and precharge circuit. Furthermore, the device characteristics and BEOL parasitic circuits used in this work have been calibrated to ensure simulation accuracy [17]. The simulation of the mean minus 6-sigma (μ - 6σ) points is performed at the temperature of 80°C to ensure the worst-case condition for write operation.

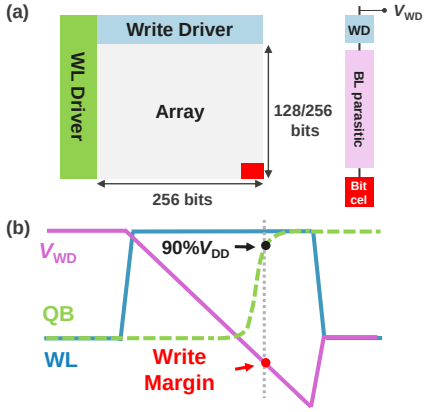

Fig. 3. Schematic view of (a) the locations of V_{WD} and the worst-case bitcell under test, and (b) write margin definition.

III. Results And Discussion

Since the highly increased R_{BL} creates a significant voltage drop for write current, the V_{BL} cannot be fully discharged to zero voltage. Hence, the effects of BL parasitic resistance (R_{BL}) must be considered. To compare the impacts of different BL parasitic elements on write margin, the combinations of resistor (R), PG transistor, and capacitor (C) are categorized into four configurations including "w/ R", "w/ R & PG", "w/ R & C", and "w/ R & PG & C". Fig.4 illustrates the schematic view of BL parasitic circuits consist of BL resistance per bitcell ($R_{BL\ PER\ CELL}$), PG transistor, BL capacitance per bitcell ($C_{BL\ PER\ CELL}$). The complete BL parasitic circuits are 128 and 256 segments in total for HP and HD design, respectively. Note that the worst-case source voltage of PG transistors is set as V_{DD} to have the largest leakage current from the internal node to BL if PG transistors are enabled unintentionally.

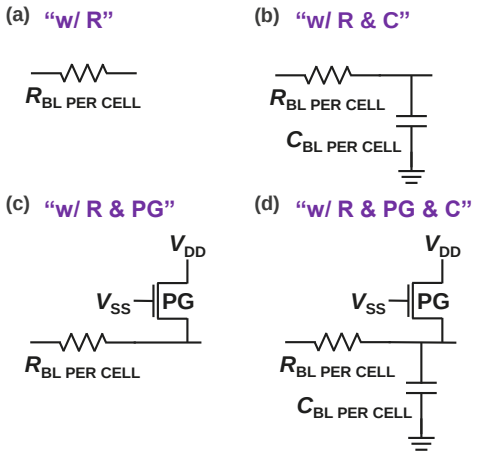

Fig. 4. Schematic view of BL parasitic circuits including (a) "w/ R", (b) "w/ R & C", (c) "w/ R & PG", and (d) "w/ R & PG & C". To ensure a worst-case analysis, the source voltage of PG transistors is set as V_{DD}.

A. *Impact of BL Parasitic Pass-Gate*

Applying a negative bias on falling BL can strengthen PG transistors connected to the internal node Q storing high voltage [1-4]. The write ability is further improved due to faster discharging speed. However, a larger R_{BL} leads to more negative V_{WD} to achieve successful data flipping. The parasitic PG transistors of half-selected bitcells along the same row of the BL will be turned on unintentionally even their WL is inactivated, once the V_{GS} becomes larger than their threshold voltage (V_T) depicted in Fig. 5. Thus, the current flowing from the internal node of the half-selected bitcells to the BL interferes with the discharging process.

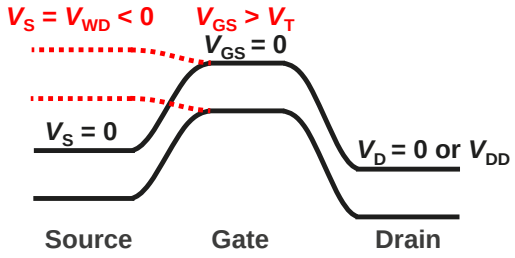

Fig. 5. Band diagrams of parasitic NMOS PG transistors of BL in the initial off states at V_{GS} = 0 V (solid black lines) and after applying an over-boosted negative V_{WD} (dashed red lines). If $V_{GS} > V_T$, the PG transistors will be turned on and cause current flow from drain to source.

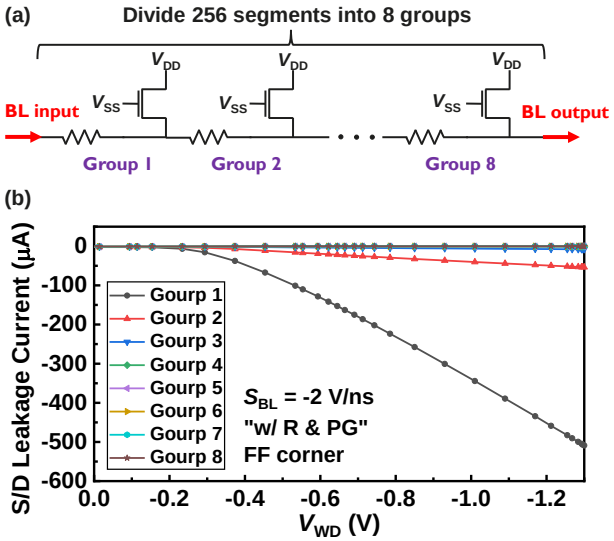

Fig. 6. HD design test circuit of PG leakage. (a) Schematic view of BL parasitic circuits considering "w/ R & PG" using 8 groups to represent 256-bit BL. (b) S/D leakage current from PG with ramping down V_{WD} at S_{BL} of -2 V/t_{BL} with t_{BL} of 1 ns.

An HD design test of PG leakage at fast NMOS and fast PMOS (FF) corner is simulated by dividing 256 segments BL parasitic circuits "w/ R & PG" into 8 groups (Fig. 6 (a)). The source to drain (S/D) leakage currents of PG transistors are increasing with negatively ramping down V_{WD} shown in Fig. 6 (b). The amount of leakage current is gradually reduced from group 1 to group 8 since the negative voltage input from the BL drops along the BL. Fig. 7 illustrates the influence of PG transistors on write margin with varying $R_{BL\ PER\ CELL}$ and BL parasitics in 2nm NS SRAM at t_{BL} of 1 ns in both HD and HP designs. Fig. 7(b) shows the write margins of "w/ R & PG" are 13% and 10% worse than "w/ R" for HD and HP designs, respectively, since V_{BL} no longer keeps discharging linearly with V_{WD}. Therefore, the PG transistors are suggested to be included in the BL parasitic circuits to prevent underestimating the write failure when $|V_{WD}| > |V_T|$.

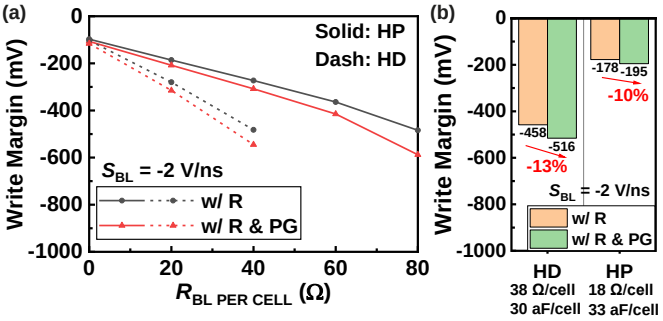

Fig. 7. Write margin with (a) varying $R_{BL\ PER\ CELL}$ and (b) BL parasitics in 2nm NS SRAM of HD and HP designs considering "w/ R" and "w/ R & PG" BL parasitic circuits at S_{BL} of -2 V/t_{BL} with t_{BL} of 1 ns.

B. *Impact of BL Parasitic Capacitors*

The parasitic capacitors which are not fully charged in transient states behave like short circuits. The current flow from write driver to bitcell thus also flows through these capacitors causing a voltage drop on BL in a transient state. Accordingly, BL parasitic capacitance (C_{BL}) should also be considered for a high-frequency operation. With increasing $R_{BL\ PER\ CELL}$ and $C_{BL\ PER\ CELL}$, the internal node needs more negative V_{WD} to write data successfully at t_{BL} of 1 ns (Fig. 8 (a)). With the BL parasitics in 2nm NS SRAM, the write margin variation of HD design (10%) is larger than HP design (4%) due to its smaller write current and larger total R_{BL} (Fig. 8 (b)). Note that the $C_{BL\ PER\ CELL}$ is reduced to less than 50 aF with scaling bitcell area [18], thus, 50 aF is used to be as an upper limit in the figure.

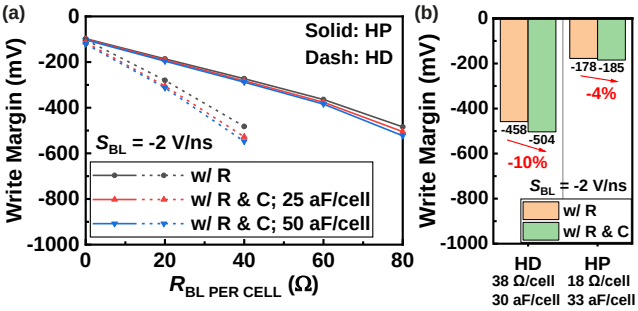

Fig. 8. Write margin with (a) varying $R_{BL\ PER\ CELL}$ and $C_{BL\ PER\ CELL}$, and (b) BL parasitics in 2nm NS SRAM of HD and HP designs considering "w/ R" and "w/ R & C" BL parasitic circuits at S_{BL} of -2 V/t_{BL} with t_{BL} of 1 ns.

Within a long enough t_{BL}, the parasitic capacitor's terminal voltage rises to meet the bias voltage and the current can no longer be drawn to the capacitors acting as an open circuit. Fig. 9 shows that the write margins in both HD and HP designs are the same with varying $R_{BL\ PER\ CELL}$ and $C_{BL\ PER\ CELL}$, and BL parasitics in 2nm NS SRAM at t_{BL} of 10 μs. Therefore, the parasitic capacitance should be considered only if the t_{BL} is short enough to make it stay in a transient state and when R_{BL} is large enough to bring out the effect of capacitors. In the

following section, the condition of requisite parasitic capacitance is verified in 2 nm NS SRAM design.

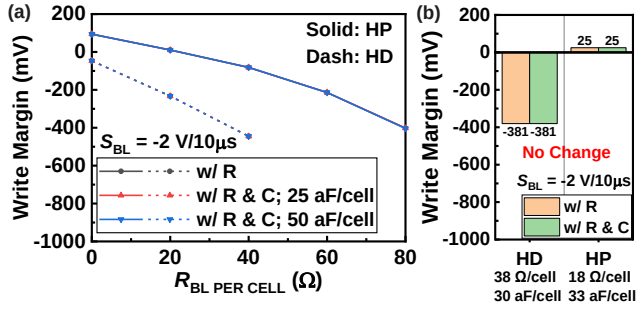

Fig. 9. Write margin with (a) varying $R_{BL\ PER\ CELL}$ and $C_{BL\ PER\ CELL}$, and (b) BL parasitics in 2nm NS SRAM of HD and HP designs considering "w/ R" and "w/ R & C" BL parasitic circuits at S_{BL} of -2 V/t_{BL} with t_{BL} of 10 µs.

C. Impact of Overall BL Parasitic circuits

The overall impacts of BL parasitics in both HD and HP SRAM designs at t_{BL} of 1 ns are shown in Fig. 10. The write margins are 0V for both HP and HD design simulated by conventional BLWM. It is too optimistic compared to the new method since it ignores all the time-dependent BL parasitics effects. The 6σ write margins of "w/ R & PG & C" are degraded by 17% and 16% compared to "w/ R" for 2nm NS SRAM HD and HP design, respectively.

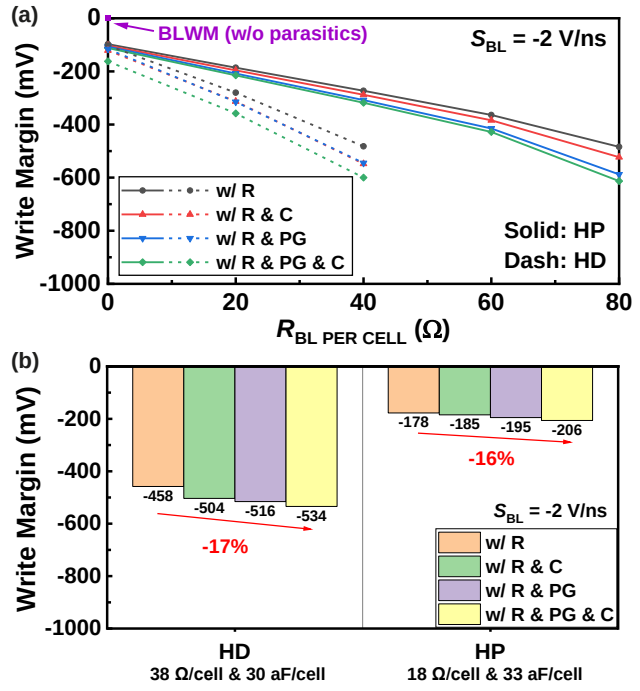

Fig. 10. Write margin with (a) varying $R_{BL\ PER\ CELL}$, and (b) BL parasitics in 2nm NS SRAM of HD and HP designs considering all the BL parasitic circuits (50 aF/cell) at S_{BL} of -2 V/t_{BL} with t_{BL} of 1 ns.

To verify the impact of BL parasitics on a real write operation related to the write margin setting, BL discharging to a zero voltage is set referring to the write margin of 0V given by BLWM. In Fig. 11, the yield is 100% for a successful data flipping without including any BL parasitics for HP design. However, the yield is decreased to only 70% if we consider all the BL parasitics into the 2nm NS SRAM HP design at S_{BL} = -2V/ns. To avoid overestimating the yield, it is crucial to analyze the impact of BL parasitics on write margin by our extended methodology.

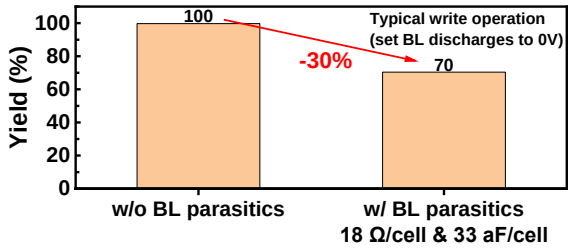

Fig. 11. Yield verification simulated in a typical write operation of 2nm NS SRAM HP design (left column: without BL parasitics; right column: with all the BL parasitics in 2nm NS SRAM). Yield loss of 30% is obtained when considering the BL parasitics in the simulation.

D. Impact of Different Operating Frequencies

The setting of S_{BL} depends on different operating frequencies, which will carry out different time-dependent effects of BL parasitic circuits. Fig. 12 shows the impacts of S_{BL} at t_{BL} of 1 ns (solid line) and 10 µs (dash line) with varying $R_{BL\ PER\ CELL}$ and $C_{BL\ PER\ CELL}$. With increasing $|S_{BL}|$ at the frequency of 1 GHz to 3 GHz, the impact from R_{BL} and C_{BL} on write margin is increased. Thus, the write margin is decreased by larger $|S_{BL}|$. With a slower frequency from 100 KHz to 300 KHz, the increased R_{BL} will still decrease the write margin, but S_{BL} and C_{BL} do not affect the results. It is important to consider the BL parasitic under a specific discharging speed in SRAM design.

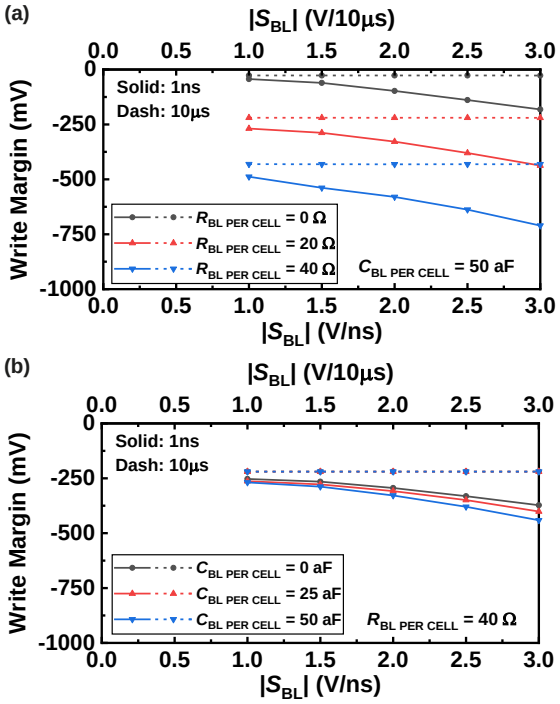

Fig. 12. Write margin with varying (a) $R_{BL\ PER\ CELL}$ (at fixed 50 aF/cell) and (b) $C_{BL\ PER\ CELL}$ (at fixed 40 Ω/cell) of HD SRAM designs considering "w/ R & PG & C" BL parasitic circuits at S_{BL} from 0 to -3 V/t_{BL} with t_{BL} of 1 ns and 10 µs.

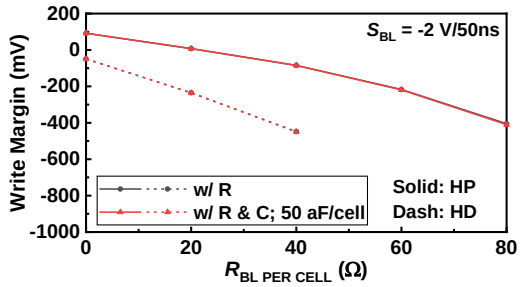

Fig. 13. Write margin with varying $R_{BL\ PER\ CELL}$ of HD and HP SRAM designs considering "w/ R" and "w/ R & C (50 aF/cell)" BL parasitic circuits at S_{BL} of -2 V/t_{BL} with t_{BL} of 50 ns.

It is proved that the parasitic capacitance should be considered only if the frequency is high enough in section III. B. To further determine the range of S_{BL} that needs to include parasitic capacitor into the BL parasitic circuits, the write margins with varying $R_{BL\ PER\ CELL}$ at $C_{BL\ PER\ CELL}$ of 50 aF and t_{BL} of 50 ns in HD and HP design are shown in Fig. 13. With decreasing t_{BL} from 10 µs to 1 ns, the write margin is reduced and the variation between "w/ R" and "w/ R & C" is enlarged. Although reduced S_{BL} can improve data flipping speed, the write margin is degraded. The write margin variation can be ignored when t_{BL} is larger than 50 ns because the difference between "w/ R" and "w/ R & C" is up to 1% at each $R_{BL\ PER\ CELL}$. Thus, parasitic C_{BL} can be neglected to reduce the simulation time in SRAM macro design if S_{BL} is above -2 V/50ns. In sub-10 nm nodes, the increased R_{BL} would amplify the effect of C_{BL}. Furthermore, a typical access time for SRAM in L1 and L2 cache is below 1 ns [2-5]. The maximum S_{BL} is therefore around -V_{DD} V/ns without NBL, which implies that the parasitic capacitance needs to be considered for write margin calculation in sub-10 nm nodes.

E. Comparison between Extended and Conventional BLWM

In Fig. 14, the write margin simulated by conventional BLWM including the same BL parasitic circuits is compared with the extended write margin methodology at t_{BL} of 1ns with 50 aF/cell based on HP and HD designs. The results of BLWM are still too optimistic due to the neglected transient behaviors. Thus, the extended write margin methodology considering a realistic ramp-down slope setting is suggested for considering significant time-dependent BL parasitic effects in resistance-dominated nodes.

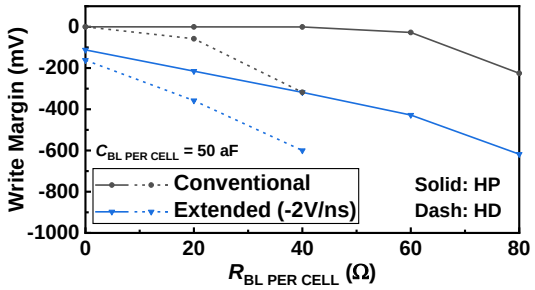

Fig. 14. Write margin comparison between conventional and extended (S_{BL} of -2 V/t_{BL} with t_{BL} of 1 ns) methods with varying $R_{BL\ PER\ CELL}$ of HD and HP SRAM designs. Note that both methods consider the same "w/ R & PG & C (50 aF/cell)" BL parasitic circuits.

IV. Conclusion

This paper proposes an extended write margin characterization methodology for SRAM design in advanced BEOL resistance-dominated technology nodes. We demonstrated that the unintentionally activated PG transistors also degrade the write margins by 13% and 10% (2nm node) at S_{BL} of -2 V/ns for HD and HP design, respectively. Furthermore, the write margin variations are 10% and 4% (2nm node) caused by the parasitic capacitors at S_{BL} of -2 V/ns for HD and HP design, respectively. The time-dependent effects of BL parasitic circuits differ with SRAM operating speeds, which can be referred to as S_{BL} settings. Our results imply that it is necessary to consider the complete BL parasitic circuits with a proper BL ramp-down speed setup for write-ability extraction in sub-10nm nodes. Otherwise, the yield would be overestimated by 30% (NS HP design in 2nm node) if the write margin is determined without time-dependent BL parasitics.

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