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Perovskite Metal-Oxide-Semiconductor structures for interface characterization

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Perovskite solar cells (PSCs) are one of the most promising photovoltaic technologies. Amongst several challenges, developing and optimizing efficient electron transport layers (ETLs) that can be up-scaled still remains a massive task. Admittance measurements on Metal-Oxide-Semiconductor (MOS) devices allow to better understand the optoelectronic properties of the interface between perovskite and the charge carrier transport layer. This work discloses a new pathway for a fundamental characterization of the oxide/semiconductor interface in PSCs. Inverted MOS structures, *i.e.*, glass/fluorine-doped tin oxide (FTO)/tin oxide (SnO_2)/perovskite were fabricated and characterized allowing to perform a comparative study on the optoelectronic characteristics of the interface between the perovskite and sputtered SnO_2. Admittance measurements allowed us to assess the interface fixed oxide charges (Q_f) and interface traps density (D_{it}), which are extremely relevant parameters that define interface properties of extraction layers. It is concluded that a 30 nm thick SnO_2 layer without annealing presents an additional recombination mechanism compared to the other studied layers, and a 20 nm thick SnO_2 layer without annealing presents the highest positive Q_f values. Thus, it is shown an effective method for the characterization of the charge carrier transport layer/perovskite interface using the analysis performed on perovskite-based inverted MOS devices.

1. Introduction

Perovskite solar cells (PSCs) have accomplished a remarkable evolution in the field of photovoltaics since its first publication in 2009,[1] currently reaching a light to power conversion efficiency (PCE) value of 25.5 %, which is close to the 26.7 % PCE value presented by single-crystalline silicon.[2,3] The rapid performance evolution by PSCs results from the intensive interdisciplinary research efforts in film crystal growth control, interface and device engineering, and in adapting feedback from both optical and electrical characterizations.[4] A PSC works as an

n-i-p or p-i-n solar cell, where the perovskite is, theoretically, an intrinsic semiconductor sandwiched between two carrier selective contacts: one for holes and another for electrons.[5–7] For the fabrication of a high-quality perovskite, the production of the PSC charge extraction layers requires special care concerning material properties and interfaces. A typical n-i-p (regular) planar PSC usually presents a stratified structure in the following order from the glass substrate to the metal electrode: i) a transparent conductive electrode (fluorine-doped tin oxide (FTO) or indium tin oxide (ITO)); ii) an electron carrier selective contact also called an electron transport layer (ETL); iii) a perovskite light absorption layer; iv) a hole carrier selective contact also called a hole transport layer (HTL); and v) a metal electrode, as schematically shown in **Figure 1**.

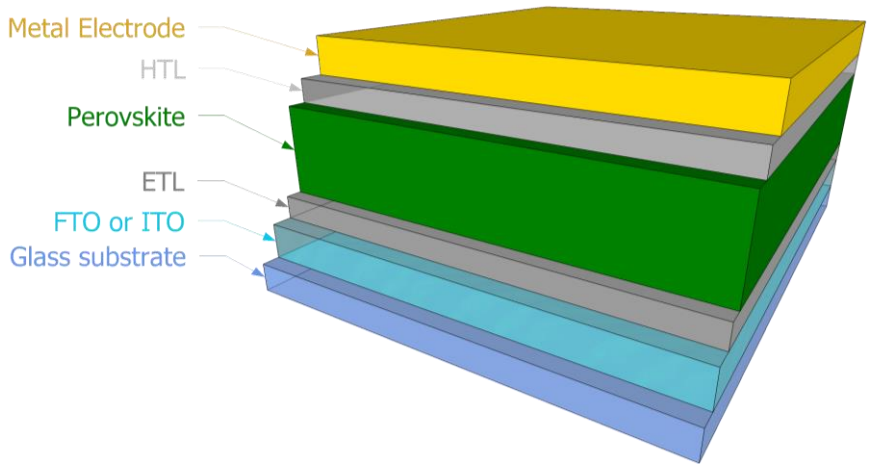


Figure 1 - Typical n-i-p (regular) planar PSC. Not at scale.

Metal oxides (MOs) are used as electron transport compact layers in planar devices, ensuring selective electron extraction and hole-blocking function.[8] Amongst the numerous MOs explored as ETLs, titanium dioxide (TiO_2) and tin oxide (SnO_2) are frequently used.[9] The SnO_2 intrinsic properties enable an effective electron extraction and transport, namely: i) deep conduction (*ca.* 4.2 to 5 eV)[8,10,11] and valence (*ca.* 8 to 9 eV)[8,10] bands; ii) in thin film it demonstrates an electron mobility value of *ca.* 10^{-3} $cm^2V^{-1}s^{-1}$;[12,13] iii) optical transparency higher than 90 %;[8,12] iv) wide bandgap of 3.3 to 4 eV;[8,10,14,15] v) excellent photo,[12,16] temporal[8] and chemical[10] stability; vi) good band alignment with the perovskite layer;[8] and vii) low temperature preparation (< 200

°C).[10,13] For planar PSCs, SnO_2 is considered the most promising alternative to overcome the shortfalls of TiO_2 ETLs, namely its insufficient electron mobility,[12] poor stability under ultraviolet (UV) illumination[9,17] and difficulties in depositing the layer in large areas using laboratorial techniques.[12,18] A recent work on planar PSCs based on SnO_2 ETLs allowed for a light to power conversion efficiency value up to 23 %.[19] Methods such as spin coating or spray pyrolysis are the most used techniques to deposit SnO_2 ETLs,[20] with atomic layer deposition, chemical bath deposition and electrodeposition also being explored.[8] However, many of these methods involve high-temperature annealing steps from 100 °C up to 550 °C,[21] which are incompatible with flexible devices and/or expensive and complex fabrication processes, which are unsuitable for large-scale application. Consequently, sputtering, which is a well-established industrial deposition technique, has recently been applied in SnO_2-based planar PSCs.[20–23] Several works are underway to better understand the impact of sputtered-deposited SnO_2 on the SnO_2/perovskite interface. It was observed a relation between the oxygen vacancy content of the sputter-deposited SnO_2 film and the substrate temperature, which lead F. Ali *et al.* to improve the energy band alignment between the ETL and the perovskite layer.[20] M. Kam *et al.* studied PSCs with SnO_2 deposited at room temperature sputtering achieving higher photovoltaic performance and stability than PSCs with solution-processed SnO_2.[21] A low sputtering power density for SnO_2 ETL deposition was found to decrease the SnO_2 surface roughness, which improved the contact interface between the perovskite layer and the ETL, leading to a reduced carrier recombination and enhanced charge transfer property of the PSC.[24] The room-temperature sputtered SnO_2 comprises nanometre-sized crystals embedded in an amorphous matrix.[25,26] Thus, it is usual to perform a post-annealing procedure to further improve its crystallinity,[10,14,26–29] and L. Qiu *et al.* reported that the SnO_2 starts to change from amorphous to crystalline at 300 °C.[26] In addition, a post-annealing procedure is usually performed in non-sputtered SnO_2 ETLs used for PSCs.[14,27–30] Thus, sputter-deposited

SnO_2 ETLs for PSCs with and without annealing were compared in the literature.[22,26] However, there is not yet an agreement for the performance of an annealing step after the SnO_2 sputter deposition, since there are works where the post-annealing treatment is performed,[31,32] and others where it is not.[21,23] Another parameter still under study on the literature is the SnO_2 ETL thickness, since depending on the deposition procedure for the SnO_2 layer, the SnO_2 optimal thickness will differ.[21–24,29,30] Fundamental works are lacking on the perovskite technology to study the optoelectronic effects induced by SnO_2 ETLs with various thickness and annealing conditions on the SnO_2/perovskite interface, which leads to a disagreement on literature regarding the ideal SnO_2 thickness and the use of post-annealing treatment. Furthermore, there is the need to further develop new ETL/HTL materials to be used in lead-free perovskite devices.[13] Thus, interface characterization is a key element to understand the correlations between PSC performance and the used ETL/HTL.[33]

In this work, electrical measurements on Metal-Oxide-Semiconductor (MOS) devices were performed to study the ETL/perovskite interface. These measurements are essential to characterize an oxide/semiconductor interface[34] as all physical effects that are part of a certain device leave their footprint in the device overall electronic response. Thus, in order to be able to isolate, even partially, a specific interface, the use of a simpler structure, such as a MOS where one of the perovskite/carrier selective layer interface from the PSC is replaced by a perovskite/metal one, becomes crucial.[35] In fact, compared to solar cells, the MOS structure simplifies the analysis and interpretation of results, and, thus, are widely used in other technologies, such as $Cu(In,Ga)Se_2$ (CIGS),[36–38] GaAs,[39,40] Silicon[41–43] and CdTe,[44,45] just to name a few examples. Therefore, MOS devices have the potential to study the interface of the perovskite with a charge transport layer (ETL or HTL). Moreover, if the MOS device replicates the fabrication of the aforementioned interface from the solar cell, the conclusions on the optoelectronic properties of the interface can

be easily transferred to the solar cells as well.[35] To study the ETL/perovskite interface of a typical n-i-p PSC architecture,[46] where the ETL is placed in between the FTO and the perovskite, an inverted MOS structure can be used,[47–51] where the ETL is also placed in between the FTO and the perovskite layer. Hence, it is possible to transfer the knowledge of the ETL/perovskite interface from the MOS measurements analysis directly to typical n-i-p PSC architectures. Such study is of utmost importance, since the charge extraction by an ETL may be compromised by recombination losses originated in traps present at the ETL/perovskite interface. One of the parameters estimated by the analysis of electrical measurements on MOS devices, is the density of interface traps (D_{it}),[34] which is crucial for the ETL/perovskite interface characterization. Moreover, another parameter estimated by electrical measurements on MOS devices is the interface fixed oxide charges (Q_f).[34] For a better understanding of the behaviour of an ETL, the estimation of the Q_f values is relevant, since according to the literature using selective contacts, the Q_f polarity values should be opposite compared to the charge carriers that are being extracted.[52–54] Since an ETL extracts electrons, positive fixed charges would be preferred. Thus, the estimation of the D_{it} and Q_f values are important to better characterize the ETL/perovskite interface under study. Moreover, the use of electrical measurements on MOS devices could be further extended for the study of perovskite/HTL interfaces as well. Perovskite MOS structures were not used to extract such parameters in the literature, but, instead, were used to study the hysteresis induced by ion movement;[50,51] to use the MOS structure as photodetector;[49] to use the MOS as a light-emitting diodes (PeLEDs)[55,56] and to use ETL-free PSCs,[57,58] just to name a few examples. In this work, electrical measurements will be performed on inverted MOS devices, as a proof of concept that allow to extract important interface parameters. Moreover, we selected SnO_2 thicknesses already studied in the literature, enabling a direct comparison with their PSCs performances, which will allow for a validation of our results.

2. Results

2.1. Inverted MOS structure

The properties of the ETL (SnO_2)/perovskite interface were studied using an inverted MOS structure replicating a typical n-i-p PSC architecture. Given the structural differences between the conventional MOS architecture (**Figure 2** a)) and the inverted MOS structure (Figure 2 b)), some considerations were made to accurately take advantage from the inverted one.

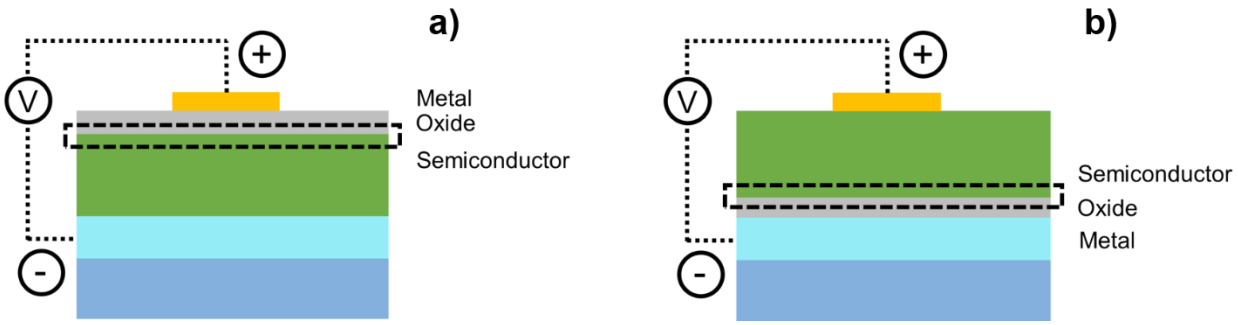


Figure 2 - Metal-Oxide-Semiconductor: a) conventional structure; and b) Inverted structure used in this work. The interface of interest is represented by a dashed line.

- The first consideration is related to the definition of the contact area. In conventional MOS devices, the metal area definition is performed on top of the oxide (yellow metal of Figure 2 a)), while in the inverted structure, the only possibility to define the contact area is to assume the area on top of the semiconductor (yellow metal of Figure 2 b)). If the area is defined correctly, then, the measured capacitance values should increase proportionally to the contact area.[59] Therefore, to validate if the inverted architecture can still use the gold top contact for area definition, capacitance values measured on inverted MOS devices with different contact areas will be compared.

- The second consideration is related with the device bias, *i.e.*, in the conventional MOS structure, by applying a positive bias on the yellow metal contact (Figure 2 a)), the MOS structure will be positively biased. However, in the inverted architecture (Figure 2 b)), by applying the same positive bias, the MOS device will be inversely biased, since the bias applied to the FTO metal (blue) of the MOS device is effectively negative.

- The third consideration refers to the expected band alignment for the inverted MOS device of this work. The band diagram of an ideal MOS device with an n-type semiconductor is shown in **Figure 3** a).[34] When a positive bias is applied, an accumulation of majority carriers (electrons) in the interface is expected to occur, as depicted in Figure 3 b), corresponding to the accumulation regime for an n-type semiconductor.[34] On the other hand, for negative bias, the opposite effect is expected, *i.e.*, a higher number of holes is present at the interface (Figure 3 c)), which corresponds to the inversion regime of the MOS device for an n-type semiconductor.[34] The estimated band diagram of our devices will be further shown, to correlate with the expected band diagrams shown in Figure 3.

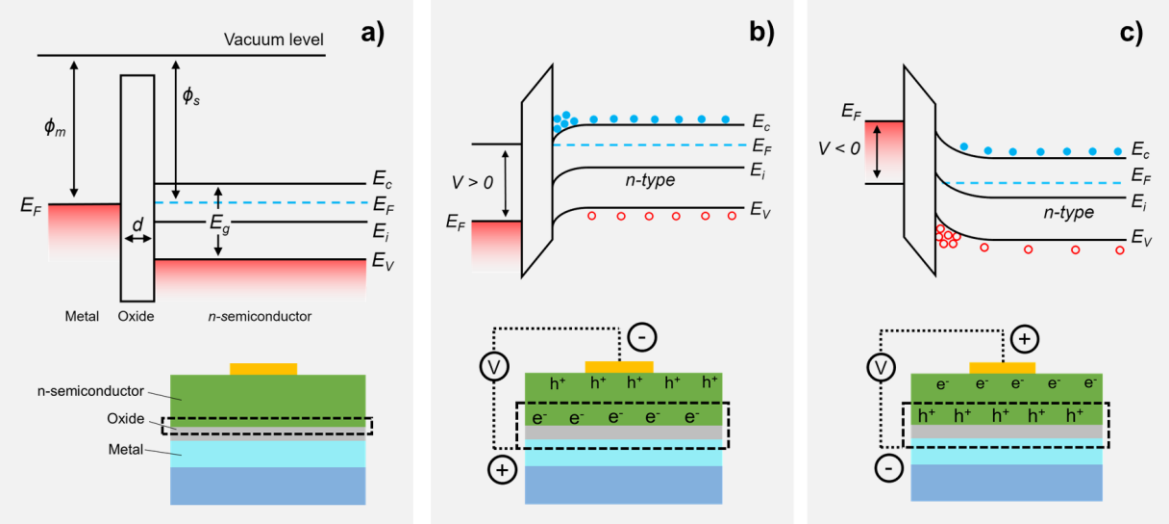


Figure 3 – Inverted MOS structure principle with the corresponding band diagram: a) ideal MOS device with n-type semiconductor; b) same as a) with positive bias applied; and c) same as a) with negative bias applied. ϕ_s is the semiconductor work function, ϕ_m is the metal work function, E_g is the semiconductor bandgap, d is the oxide thickness, E_c is the conduction band minimum, E_v is the valence band maximum, E_f is the fermi level and E_i is the intrinsic level. Adapted with permission.[34] Copyright 2006, John Wiley & Sons.

To better understand the band diagram of our working device (third consideration), UPS and REELS measurements were carried out on a sample with a 30 nm thick SnO_2 deposited by sputtering on FTO (before and after annealing). Note that the sample stack was only FTO/SnO_2. The SnO_2 E_g value, the SnO_2 work function value (ϕ_{SnO2}) and the difference between the SnO_2 valence band and the fermi level (E_v-E_f) were estimated as shown in **Figure S1** of the Supporting Information. Such values allow for an estimation of the maximum valence band and the electron

affinity values of the SnO_2 layer. Moreover, the perovskite bandgap and work function values were extracted from the literature, considering a work that studied a perovskite with identical composition used in this work.[60] **Figure 4** a) shows the estimated band diagram of the MOS device, using the aforementioned values without the SnO_2 annealing treatment, and in Figure 4 b) for the MOS device with annealed SnO_2. Based on the band diagrams of Figures 4 a) and b), the SnO_2/perovskite interface should not have accumulation of electrons after applying positive bias since the conduction band's lowest energy of the SnO_2 layer is lower than the perovskite one, contrarily to an ideal MOS device, as shown in Figure 3 b). The inversion regime of the MOS device should not be affected, since the valence bands' alignment between the perovskite and SnO_2 is in accordance with the ideal MOS device (Figure 3 c)). Such band alignment was expected, since the interface under study is projected to work as a selective contact for electrons in PSCs, *i.e.*, with the ability to extract electrons, and, at the same time, to block holes, which is exactly accomplished by the shown band diagram. MOS devices were already developed with the main objective to accomplish a low resistive selective/ohmic contact.[61–64] Thus, several works reported MOS devices with similar band diagrams as shown in Figure 4.[62–68] Nonetheless, the analysis of electrical measurements performed on MOS structures with the mentioned band diagram should be carried out with care, since it is expected an increased leakage current, considering that electrons do not have a barrier between the oxide and the semiconductor.[67,69,70] Regarding the parameters commonly estimated from the C-V curves,[34] A. G. Scheuermann *et al.* mentioned that the oxide capacitance value (henceforth named C_{in}) may be affected by the possible leakage current, whereas the flat-band voltage (V_{fb}) should not be affected.[70] Nevertheless, the use of the parameter values further estimated in this work for comparison with other studies should be done with caution, as the MOS devices studied in this work have a non-ideal band diagram. Thus, the parameters values that will further be estimated should be used mostly for comparative discussion within this work.

The main objective of this section is to show that some considerations must be addressed when using the inverted MOS devices fabricated in this work. It was possible to depict the working principle and we will show ahead a possible pathway to analyse the SnO_2/perovskite interface by using inverted MOS devices, composed by FTO/SnO_2/$FA_{0.83}Cs_{0.17}PbI_{1.8}Br_{1.2}$, as a proof of concept.

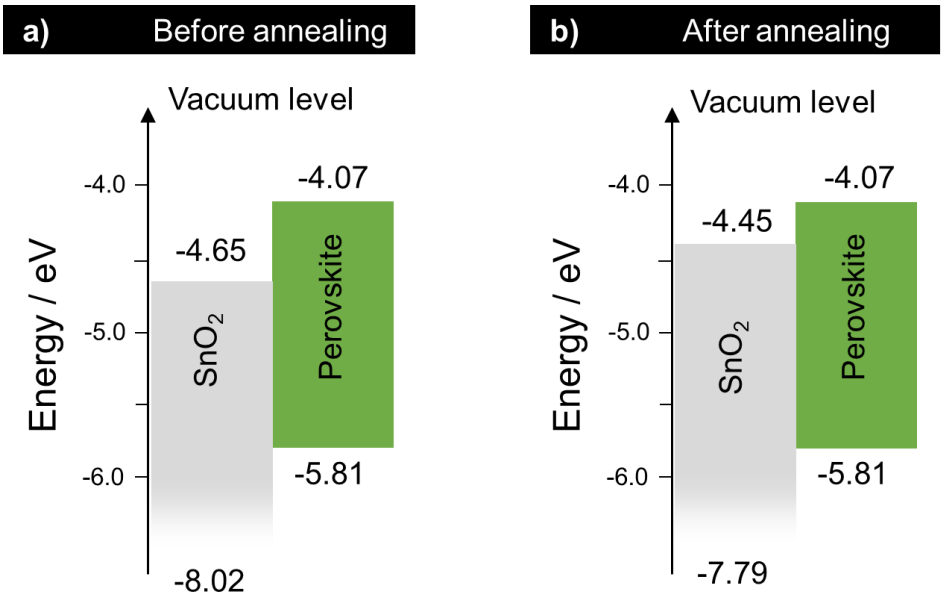


Figure 4 – Band diagram of the devices studied in this work: a) SnO_2 without annealing; and b) SnO_2 with annealing.

2.2. C-V and C-f measurements

In this section, we will investigate if typical MOS C-V curves[34,35,59] that present a clear distinction between the accumulation, depletion and inversion regimes can be obtained with the inverted MOS device FTO/SnO_2/$FA_{0.83}Cs_{0.17}PbI_{1.8}Br_{1.2}$. Moreover, we will study the possible Q_f and D_{it} values present in the SnO_2/perovskite interface. Four MOS devices were fabricated with two SnO_2 thickness values (20 and 30 nm) with and without annealing. **Table I** summarizes the preparation conditions of the devices studied in this work, with the corresponding names that will be used henceforth.

Table I – MOS devices studied in this work with two different SnO_2 thicknesses. The devices with SnO_2 that underwent annealing are also mentioned.

Device	SnO_2 thickness (nm)	Annealing (300 °C)	Top contact diameter (mm)
20NoAnneal	20	No	0.5, 1 and 2
20Anneal	20	Yes	0.5, 1 and 2
30NoAnneal	30	No	0.5, 1 and 2
30Anneal	30	Yes	0.5, 1 and 2

To study the contact area definition (consideration 1), three curves of the 20NoAnneal device are shown in **Figure 5** for three contact diameters: 0.5, 1 and 2 mm. A clear capacitance increase proportional to contact area is observed for the MOS devices. Thus, the effective impact of the contact area on the capacitance values is confirmed, validating that the area is defined in such inverted structure. Furthermore, for all devices, a typical MOS C-V behaviour was observed[34,35] – not shown – with a distinct accumulation, depletion and inversion regimes that correspond to the maximum, intermediate and minimum measured capacitance values, respectively. Since the measured C-V plots show a typical behaviour of MOS devices, we have confidence that our inverted FTO/SnO_2/Perovskite MOS device is working as intended, and, thus, we will proceed with the analysis of the inverted MOS structures.

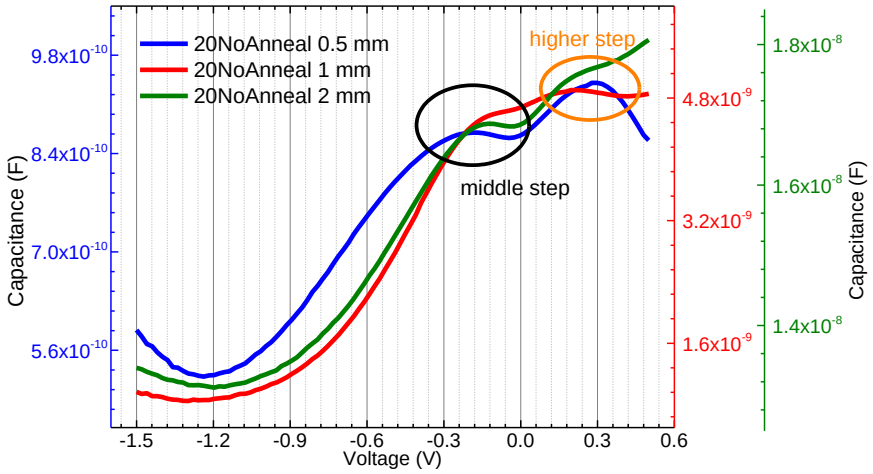


Figure 5 - Representative MOS C-V curves of 20NoAnneal device with 0.5, 1 and 2 mm diameter contacts. All MOS devices in this work had similar C-V behaviours. The black circle represents the middle step and the orange circle represents the higher step. Note that the capacitance values of the three plots have an order of magnitude difference between them.

The C-V plots of this work, as shown in Figure 5, have the higher step at positive bias (marked with an orange circle in Figure 5), corresponding to the accumulation regime, where the capacitance value of the oxide layer is typically estimated.[34] Then, with decreasing bias, the capacitance value decreases (depletion region), until it reaches a minimum capacitance that might correspond to the inversion region.[34] However, a middle step was identified in the C-V plot, marked with a black circle in Figure 5, which is not a common feature in typical MOS devices.[34,35] Although representative MOS devices are shown in Figure 5, the same behaviour was observed independently of the SnO_2 thickness, annealing or contact area. Thus, three possible hypotheses for the appearance of a middle step in the C-V plots of our devices will be presented:

- The first hypothesis considers that the middle step appearance is related with the presence of interface traps (hypothesis 1), which was already reported in the literature.[71–74] Several studies used the conductance (G_p) or G_p/ω as a function of bias to correlate the middle step appearance with interface traps.[72,74–77] In fact, the appearance of a peak in the measured G_p or G_p/ω *vs.* bias or frequency curve is an indication of loss mechanisms due to interface trap capture and/or emission of carriers.[35,59] Therefore, in order to further investigate if our devices suffer from the same effect, the capacitance curve was coupled with the G_p/ω as a function of the bias curve, as shown in **Figure 6**, where G_p/ω is given by:[34–36,59]

$$\left(\frac{G_p}{\omega}\right) = \frac{\omega G_m C_{in}^2}{G_m^2 + \omega^2 (C_{in} - C_m)^2} \quad (1)$$

where C_{in} is the oxide capacitance taken in the accumulation regime (positive bias) of the C-V curve, C_m is the measured capacitance, G_m is the measured conductance and $\omega = 2\pi f$ is the angular frequency. The middle capacitance step appears in the same region as the G_p/ω peak, shown in Figure 6 a) for the 20NoAnneal device, which was also observed for all the devices. Such observation is a possible indication that the middle step is caused by interface traps. Nonetheless,

for the 30NoAnneal device, a second peak appears at higher voltage values (Figure 6 b)). Assuming that a peak in the G_p/ω is directly related with traps, the appearance of a second peak is a possible indication that the 30NoAnneal device has an additional recombination mechanism, compared to the other studied devices.

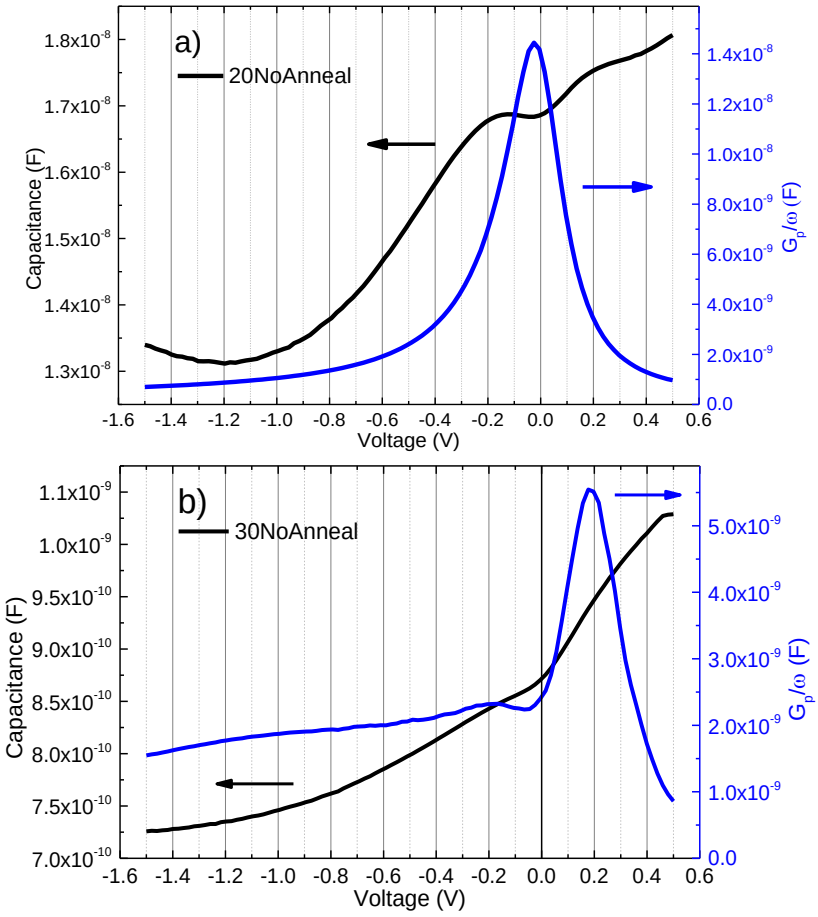


Figure 6 – Representative capacitance curve (black) coupled with the G_p/ω curve (blue) in function of bias of two devices: a) 20NoAnneal; and b) 30NoAnneal, measured at 10 kHz. Note that 20Anneal and 30Anneal devices have similar behaviour as observed for the 20NoAnneal device a)).

- The second hypothesis for the appearance of two steps in the C-V curve is related with ion movement (hypothesis 2). T. Pang *et al.* reported the possible movement of iodine ions through grain boundaries in the perovskite[51] showing that such ions are negatively charged and can accumulate at the MOS interface. Therefore, assuming the possibility that the negative ions can accumulate at the interface due to a positive bias, it may be expected that the higher step at positive

bias is caused by ions accumulation, and that the capacitance middle step is related with the oxide layer.

- The third hypothesis for the double step appearance is the possible electrons depletion behaviour of the SnO_2 layer (hypothesis 3), which was already observed for TiO_2 in a conventional MOS structure.[78] According to J. Lontchi *et al.*, the possible partial or full depletion of TiO_2 may significantly influence the measured capacitance values.[78]

Lastly, due to the measurements and techniques used in this work, it is not possible to accurately assess which of the three aforementioned hypotheses is the one that better explains the appearance of the middle step in the C-V curves. However, this does not impact the qualitative discussion of the next results. Further studies are needed, as these three hypothesis raise relevant questions for PSCs performance.

From C-V and C-f measurements, both the D_{it} and the Q_f values can be studied.[34,59] Exemplificative procedures will be shown to estimate both parameters to the four fabricated devices.

The conductance method was used for the D_{it} values estimation, using the following equation:[35,59]

$$D_{it} = \frac{2.5}{A \times q}\left(\frac{G_p}{\omega}\right)_{max} \quad (2)$$

where $(G_p/\omega)_{max}$ is the maximum value of the G_p/ω plot using equation (1) in function of the frequency, A is the area of the top contact and q is the electron charge. As previously mentioned, a peak in the measured G_p/ω curve is an indication of loss mechanisms due to interface traps. To plot G_p/ω from equation (1), the C_{in} value needs to be estimated either from the higher or middle step from the C-V curves. Considering that the C_{in} values are in the same order of magnitude for both steps (Figure 5), it is not expected a significant change in the G_p/ω plot. Moreover, conventionally, the C_{in} value is estimated from the accumulation regime (higher step) in typical MOS devices.[34,35]

Thus, the C_{in} value from the higher step was used for the G_p/ω plots. **Figure 7** a) shows a G_p/ω *vs.* frequency plot for the device 20NoAnneal, Figure 7 b) for the 20Anneal device, Figure 7 c) for the 30NoAnneal device and Figure 7 d) for the 30Anneal device. Considering the asymmetry of the plots and assuming that multiple contributions (associated with recombination mechanisms) may be present, multi-peak fitting using Gauss functions was performed for all devices' plots. The fitting of the G_p/ω plot was already described in the literature, which allowed to distinguish between different types of traps.[79] Thus, from Figures 7 a), b) and d), it becomes clear that there are two contributions for the G_p/ω response in the case of 20NoAnneal, 20Anneal and 30Anneal devices, respectively, meaning that two main recombination mechanisms are present. The 30NoAnneal device presents a different behaviour, as shown in Figure 7 c), since there are three contributions to the G_p/ω response. The red and green fitted peaks (B and C, respectively) match the same peaks observed for the other devices, and a new one appears at low frequency values (peak A). For the 30NoAnneal device, the G_p/ω *vs.* frequency behaviour agrees with the G_p/ω *vs.* bias behaviour, since in both frequency and bias, the 30NoAnneal device appears to have an additional recombination mechanism compared to the other studied devices.

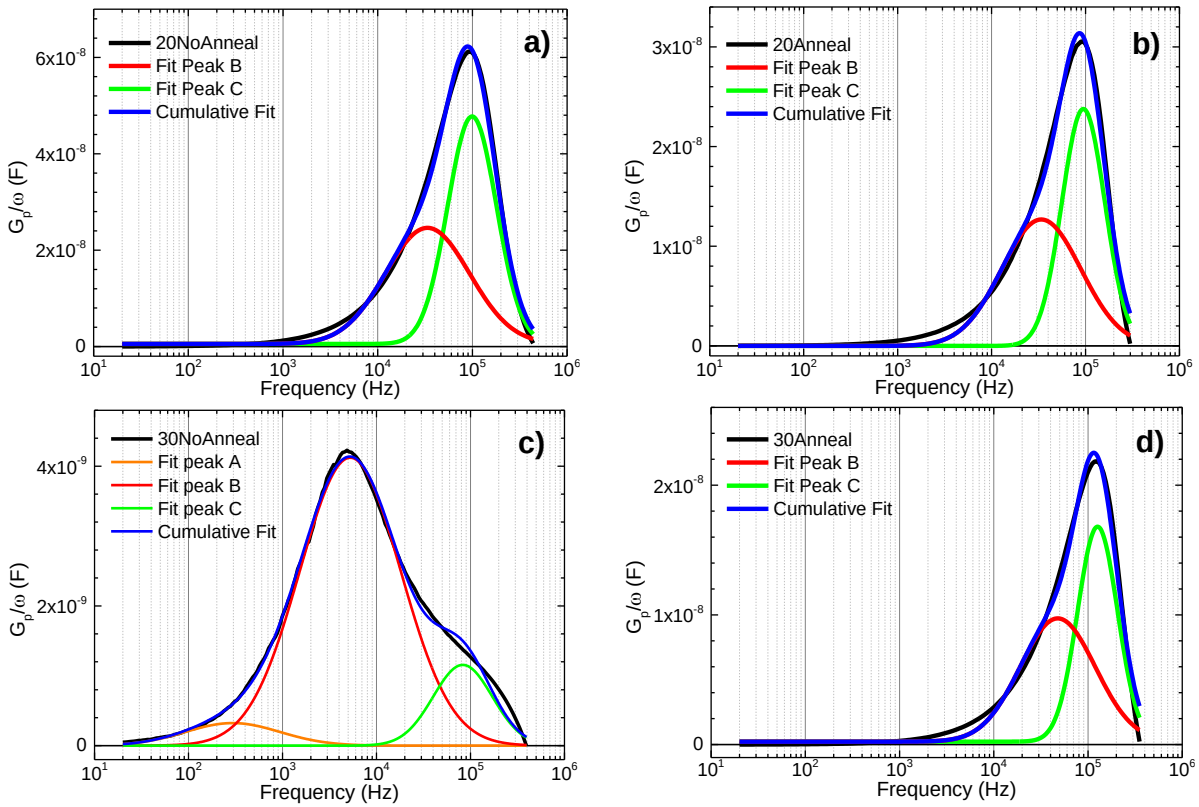


Figure 7 – G_p/ω and peak fitting plots of: a) 20NoAnneal device; b) 20Anneal device; c) 30NoAnneal device; and d) 30Anneal device. All measurements were performed at 0 V bias.

The estimated D_{it} values for all MOS structures, using equation (2), are presented in **Figure 8**. The D_{it} values of the device with a 20 nm SnO_2 layer slightly decrease after the annealing step. Nonetheless, 30NoAnneal and 30Anneal devices present similar D_{it} values compared to the 20Anneal device within the standard deviation values. Such result was unexpected, since the 30NoAnneal device may have an additional recombination mechanism compared to the other devices, according to the G_p/ω curves in function of both bias and frequency. This remark agrees with previous reports that point out the limitations of using the conductance method to estimate the D_{it} values.[80–82] When the D_{it} value is larger than $4C_{in}/q$,[80] which is the case of our devices, an underestimation of the D_{it} values may happen.[82] In Figure 8, with the exception of the slightly D_{it} value decrease from 20NoAnneal to 20Anneal device, all devices present similar D_{it} values, indicating a possible saturation of the traps density, which can be a preliminary evidence that a

significant loss of sensitivity may have occurred while using the conductance method, as described elsewhere.[81,82]

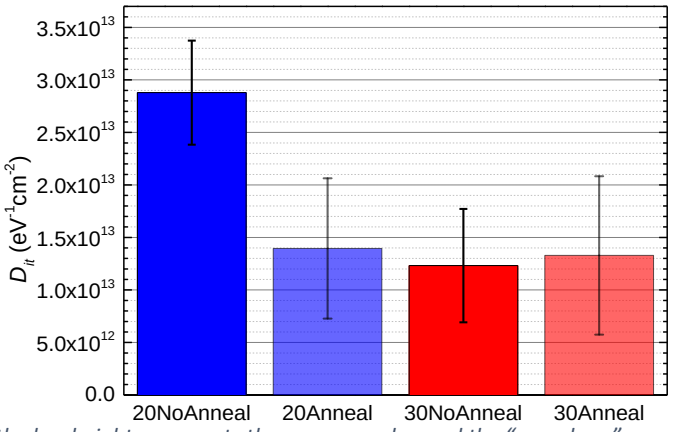


Figure 8 – D_{it} values where the bar height represents the average value and the "error bars" represent the standard deviation values.

The Q_f values are estimated by:[38,59,83,84]

$$Q_f = \frac{C_{in}\left(\phi_{MS} - V_{fb}\right)}{A \times q} \tag{3}$$

where ϕ_{MS} is the metal-semiconductor work function difference and V_{fb} is the flat-band voltage. The ϕ_{MS} value is estimated from the difference between the metal work function value of FTO (4.6 eV according to W. Zhu *et al.*[85]) and the semiconductor work function value of $FA_{0.83}Cs_{0.17}PbI_{1.8}Br_{1.2}$ (4.38 eV extrapolated from the values reported elsewhere[60]), corresponding to a ϕ_{MS} value of *ca.* 0.22 eV. The V_{fb} precise calculation for the devices in this work is difficult without a clear understanding of the cause for both steps in the C-V curves. However, considering both the higher and middle steps, it was possible to estimate the V_{fb} values, as shown in **Figure S2** of the Supporting Information, for the device 20NoAnneal, as an example.

Considering that C_{in}, A and q have positive values, the Q_f values' polarity is only dependent on the $\phi_{MS} - V_{fb}$ (equation (3)). Thus, the choice of the step for the V_{fb} estimation will influence the Q_f values, as shown in Figure S2 of the Supporting Information. As an example, considering ϕ_{MS}

equal to 0.22 eV, if V_{fb} is higher than 0.22 eV, then Q_f assumes negative values; on the other hand, if V_{fb} is lower than 0.22 eV, then Q_f will be positive.

Considering the higher step for the Q_f estimation, the observed trends for the Q_f values are shown in **Figure 9** a). The V_{fb} values estimated from the higher step of the C-V curve are close to the ϕ_{MS} value for all devices, which means that the Q_f values are close to zero. Moreover, slight variations in the V_{fb} values close to ϕ_{MS} can result in a Q_f value polarity switch, which could be a plausible explanation to the polarity switch observed between 20NoAnneal and 30NoAnneal devices.

The observed trends for the estimation of Q_f values based on the middle step are shown in Figure 9 b). Regarding devices with a 20 nm thick SnO_2 layer, a higher density of interface fixed oxide charges is observed without annealing. On the other hand, regarding devices with a 30 nm thick SnO_2 layer, the same Q_f values were obtained with and without annealing. Nevertheless, as previously mentioned, it is important to point out that the use of the Q_f absolute values of this work for comparison with other studies should be done with caution, since it is not clear which step should be used for the V_{fb} and C_{in} estimation. Thus, these values should only be used for comparative discussion within this work.

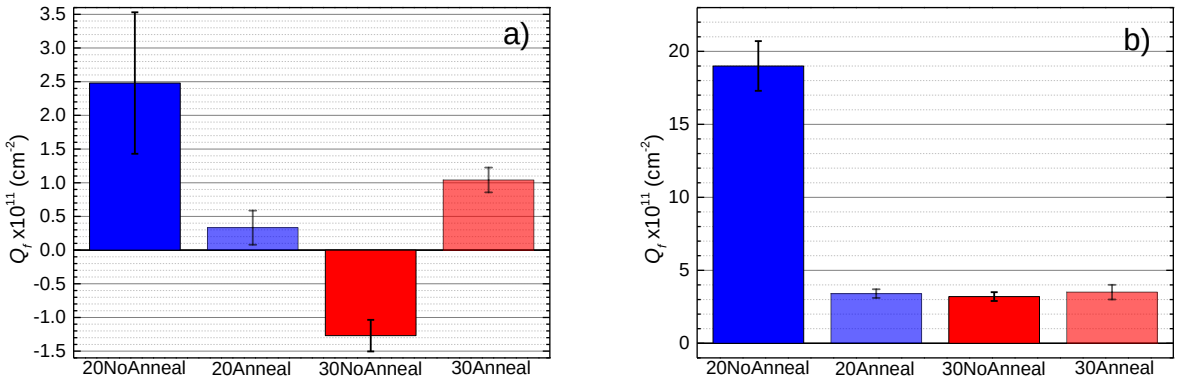


Figure 9 - Q_f values for all devices studied in this work: a) estimated using C_{in} and V_{fb} values from the higher step; and b) estimated using C_{in} and V_{fb} values from the middle step. The bar height represents the average value and the "error bars" represent the standard deviation values.

3. Discussion

Perovskite–based inverted MOS structures were successfully fabricated and its C-V curves presented a distinct accumulation, depletion and inversion regimes, reinforcing that the devices are working as intended. In this work, the (G_p/ω) *vs.* bias and frequency plots were studied in order to better comprehend the possible recombination mechanisms present in the SnO_2/perovskite interface. It was found that the 30NoAnneal device presented a distinctive behaviour both for (G_p/ω) *vs.* bias and frequency compared to the other three studied devices. The (G_p/ω) *vs.* bias plot of the 30NoAnneal device presented two peaks instead of one for the other devices, and the (G_p/ω) *vs.* frequency plot of the 30NoAnneal device presented three recombination mechanisms compared to the two recombination mechanisms present in the other devices. Such result evidences that either a 20 nm SnO_2 layer or a 30 nm SnO_2 layer with annealing would be preferred to be used as ETL in PSCs. To further understand which one should be used, the Q_f values were also taken into account. On one hand, analysing the Q_f values in the case of the higher C-V step, the Q_f values polarity switch between the 20NoAnneal and 30NoAnneal devices could be explained by the ϕ_{MS} and V_{fb} values proximity. Nonetheless, the 20NoAnneal device presents the highest positive Q_f values. On the other hand, considering the middle step for the Q_f estimation, the 20NoAnneal device presents, again, the highest positive Q_f values, whereas the 20Anneal, 30NoAnneal and 30Anneal have similar Q_f values. One possible hypothesis that explains such Q_f results is to assume that the deposition time has the same effect as the annealing step, *i.e.*, the annealing step reduces the Q_f values of the 20 nm device, which could have the same effect as the deposition time, and, thus, the 30NoAnneal device has the same Q_f value as the 20Anneal device. Since the 30NoAnneal device has its Q_f values already decreased due to longer deposition time, the annealing step did not have any effect, and, thus, the 30Anneal device has a similar Q_f value as 30NoAnneal and 20Anneal devices. The 20 nm thick SnO_2 layer without annealing has the highest positive Q_f values of this work (considering either the middle or higher steps for its estimation), as desired for an ETL. Such

result is in agreement with the previous G_p/ω *vs.* bias and frequency analyses, which also supports the use of 20 nm thick SnO_2 layers, and with the input from the Q_f values estimation, it is evidenced that an annealing treatment is not needed. Considering the devices without SnO_2 annealing (20NoAnneal and 30NoAnneal), the cause for differences between them remain unclear, as both devices underwent similar fabrication procedures. However, the differences between them may be related with the different sputtering deposition times, since it has been reported in the literature that a prolonged exposure to the sputtering plasma may affect the surface properties of the SnO_2 layer.[26] Moreover, the observation of different PSCs performances due to the sputtering deposition of different SnO_2 thicknesses was already observed[21–23,26] with a decrease of open-circuit voltage (V_{oc}) values with increasing SnO_2 thickness values. Moreover, several works reported solar cells' results where the *ca.* 20 nm thick SnO_2 layer without annealing was found to achieve higher PSCs' performances compared to other studied thicknesses and with annealing.[22–24,26] Thus, such reports are in accordance with our work, since the additional recombination mechanism at the interface SnO_2/perovskite observed in the 30NoAnneal device compared to the 20NoAnneal device in addition to the high positive Q_f values of the 20NoAnneal device, are a clear indication that the 20 nm thick SnO_2 layer without annealing treatment should be used as ETL for $FA_{0.83}Cs_{0.17}PbI_{1.8}Br_{1.2}$ PSCs. In order to further evaluate the density of SnO_2/perovskite interface traps, D_{it} values for all devices were estimated. However, the conductance method used in this work for the D_{it} estimation revealed a possible loss of sensitivity to accurately extract the D_{it} values, which is an indication that metal contacts with a larger diameter should be used to further increase capacitance values and move away from the condition that the D_{it} values are higher than $4C_{in}/q$. Despite of the impossibility to precisely extract the D_{it} values, the presented analysis shows that all devices have D_{it} values possibly larger than 10^{13} $eV^{-1}cm^{-2}$ indicating that the SnO_2/perovskite is highly recombinative independently of SnO_2 thickness or annealing step. Thus, the

SnO_2/perovskite interface still has room for further improvement in order to reach significantly lower D_{it} values, which would reduce interface recombination losses.

4. Conclusions

We successfully fabricated functional inverted MOS devices based on metal/SnO_2/perovskite. The high sensitivity of MOS devices for the characterization of the ETL/perovskite interface was clearly evidenced by the detection of differences between the 20 and 30 nm thick SnO_2 layers. According to the (G_p/ω) *vs.* frequency measurements, the 30NoAnneal device presented three dominant recombination mechanisms, while the three remaining devices have two dominant recombination mechanisms. All devices present high values of interface traps above 10^{13} $eV^{-1}cm^{-2}$ and possibly even higher due to the limitations of the conduction method. Therefore, in terms of chemical passivation it is evidenced that the SnO_2/perovskite interface still has room for further improvement to reduce interface recombination losses. The device with the 20 nm thick SnO_2 layer without annealing displayed the highest positive Q_f values amongst the studied devices, which is a desired result for ETLs, as positive Q_f charges are needed over negative Q_f charges. Considering that the fabricated inverted MOS devices have the same structure as a typical n-i-p PSC architecture, the obtained results suggest that the 20 nm thick SnO_2 layer without annealing is more suitable to be used as ETL for $FA_{0.83}Cs_{0.17}PbI_{1.8}Br_{1.2}$ PSCs compared to the 30 nm thick SnO_2 layer. It is noted that different perovskite layers or ETLs may induce differences in the interface under study, and, thus, MOS devices should be fabricated for each desired perovskite and/or ETL interface to extract the respective Q_f and D_{it} values. In order to extract the maximum information from the perovskite interfaces, future perovskite-based MOS devices should take into account the following: i) to acquire more robust D_{it} values it would be needed to fabricate devices with a top contact with a diameter of 3 mm or higher, in order to increase the capacitance values, moving away from the condition that D_{it} is larger than $4C_{in}/q$; ii) it should be conducted forward and reverse

bias C-V measurements in order to study a hysteresis effect due to the possible presence of ions in the perovskite; and iii) (G_p/ω) *vs.* frequency measurements should be conducted at different bias and temperatures, in order to further study the recombination mechanisms present in each device. In short, this work presents a novel strategy and indications to characterize PSCs based on MOS devices, aiming to extract more information on the perovskite/(ETL or HTL) interface. The use of MOS devices for optoelectronic studies is of the utmost importance, enabling the further development of already existing ETL/HTL materials for PSCs. Additionally, this work shows that the use of MOS devices is essential for developing new ETL/HTL materials, allowing for a better understanding of their optoelectronic properties, which remains critical for the successful integration of PSCs in the energy market.

5. Methods

5.1. Materials and Perovskite Precursor Solution

The perovskite layer was prepared with Cesium iodide (CsI, 99.9 %), lead (II) bromide ($PbBr_2$, 98 %), lead (II) iodide (PbI_2, 99 %), and hydrobromic acid (HBr, 48 wt %), all from Sigma-Aldrich, and hydriodic acid (HI, 57 wt %) from Alfa Aesar. The chemicals were used without further purification. The perovskite precursor solution (0.95 M) with nominal composition of $FA_{0.83}Cs_{0.17}PbI(_{0.6}Br_{0.4})_3$ was prepared by dissolving FAI (272 mg), CsI (83.4 mg), PbI_2 (350 mg), and $PbBr_2$ (418 mg) in N,N-dimethylformamide (2 mL). HI (109.4 μL) and HBr (54.6 μL) and the solution was stirred for 48 h at room temperature, according with the experimental procedure described elsewhere.[86]

5.2. Metal-Oxide-Semiconductor fabrication

For the MOS structures fabrication, radio frequency (RF) sputtering (room temperature, SnO_2 target with a diameter of 2 '' (*ca.* 5 cm), bias voltage of 228 V, chamber pressure of 6.9 $x10^{-3}$ mBar at 60 W with a deposition rate of 1.30 nm/min on a Kenosistec multitarget UHV sputtering system)

was used to deposit a compact SnO_2 layer with a thickness of 20 and 30 nm. The SnO_2 layer was deposited onto a fluorine-doped SnO_2 (FTO, Pilkington, TEC8), previously cleaned following a stepwise procedure with detergent, deionized water, acetone and isopropanol (IPA). The SnO_2 films were annealed following a multistep temperature ramp, up to 300 °C (room temperature, 10 °C·min^{-1}; 100 °C, 10 min, 10 °C·min^{-1}; 200 °C, 10 min, 10 °C·min^{-1}; 300 °C, 30 min). Prior to the perovskite deposition, the FTO/SnO_2 substrate was exposed to UV light for 15 min aiming to improve the surface wettability and the SnO_2 thickness was confirmed by contact profilometer. Subsequently, the perovskite precursor solutions were filtered with 0.20 μm PTFE filters and spin-coated at 2000 rpm for 45 s on a FTO/SnO_2 substrate preheated at 70 °C. The films were dried on a hot plate at 70 °C for 5 min, and then annealed in a conventional oven in air following a multistep temperature ramp up to 185 °C (room temperature, 10 °C·min^{-1}; 100 °C, 10 min, 10 °C·min^{-1}; 185 °C, 30 min). The resulting MOS stack consisted of FTO/SnO_2/Perovskite. Gold electrodes with three different diameters were then deposited by sputter-coating under vacuum through a hard mask. The final MOS structure is schematized in **Figure S3** of the Supporting Information.

For the capacitance-voltage-frequency (C-V-f or C-V) and capacitance-conductance-frequency (C-G-f or C-f) measurements, a precision LCR meter Keysight E4980 A was used. The C-V-f measurements were performed in dark with a DC voltage bias range from 0.5 V to -1.5 V, with a frequency of 10 kHz and a root mean square AC voltage signal (V_{RMS}) of 25 mV. The C-G-f measurements were performed in the dark from 20 Hz to 1 MHz, with a bias of 0 V and a V_{RMS} value of 25 mV. The LCR equipment considers a circuit consisting of a capacitance (C_m) in parallel with a conductance (G_m), which are the output parameters of the LCR measurements, as described elsewhere.[87] Ultraviolet Photoelectron Spectroscopy (UPS) and Reflection Electron Energy Loss Spectroscopy (REELS) measurements were performed in the ESCALAB 250Xi from Thermo Scientific, using a helium discharge lamp (He I = 21.2 eV) and 1 keV electron energy. UPS was

used to obtain the SnO_2 work function (ϕ_{SnO2}). REELS analysis allowed to obtain the SnO_2 electronic bandgap (E_g). The base pressure of the system was below 5×10^{-9} mbar. For the UPS and REELS measurements, a glass/FTO substrate was used with a 30 nm thick SnO_2 layer deposited by sputtering with the same conditions as previously described. Measurements performed with this sample were carried out with and without the same annealing conditions as previously mentioned.

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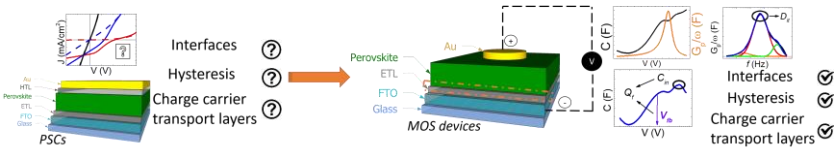
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ToC

A new pathway to characterize the charge carrier transport layer/perovskite interface is shown through the use of inverted Metal-Oxide-Semiconductor (MOS) devices. Admittance measurements performed on the MOS devices allow for the study of important optoelectronic properties of the charge carrier transport layer/perovskite interface, which will help to further improve perovskite solar cells (PSCs).

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Perovskite Metal-Oxide-Semiconductor structures for interface characterization



Supporting Information

Perovskite Metal-Oxide-Semiconductor structures for interface characterization

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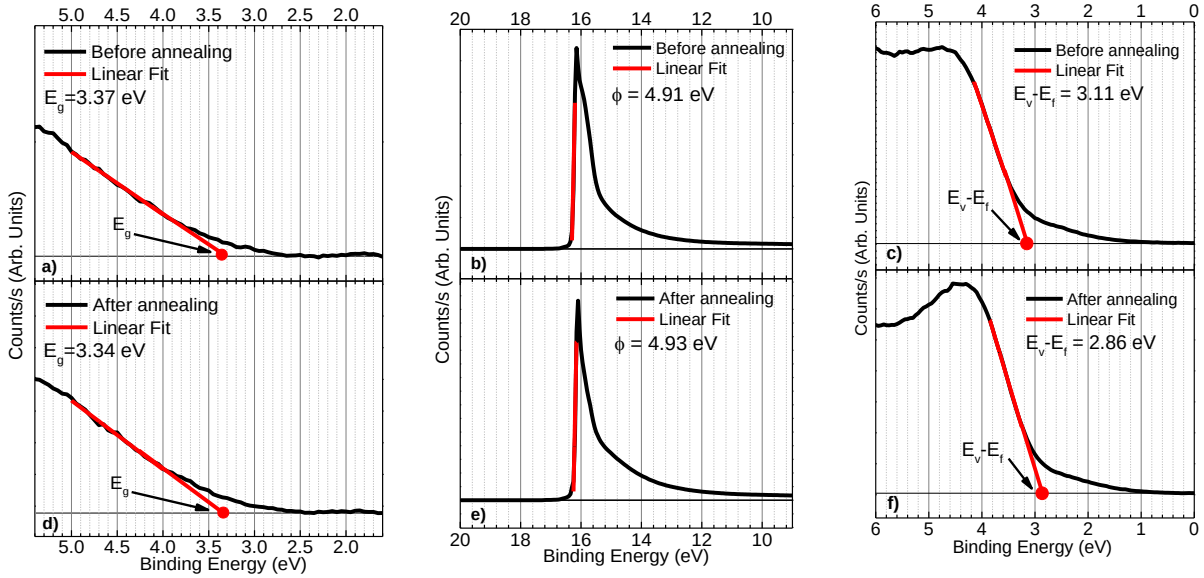


Figure S1 – REELS and UPS measurements performed on a 30 nm thick SnO_2 layer: a) REELS before annealing for SnO_2 E_g estimation; b) UPS before annealing for ϕ_{SnO2} estimation; c) UPS before annealing for SnO_2 E_v-E_f estimation; d) REELS after annealing for SnO_2 E_g estimation; e) UPS after annealing for ϕ_{SnO2} estimation; and f) UPS after annealing for SnO_2 E_v-E_f estimation.

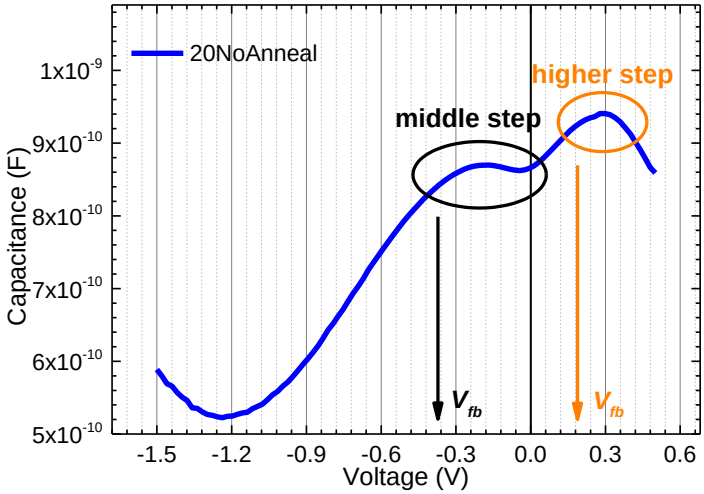


Figure S2 – Example of V_{fb} estimation for the device 20NoAnneal. In black it is represented the middle step and in orange, the higher step.

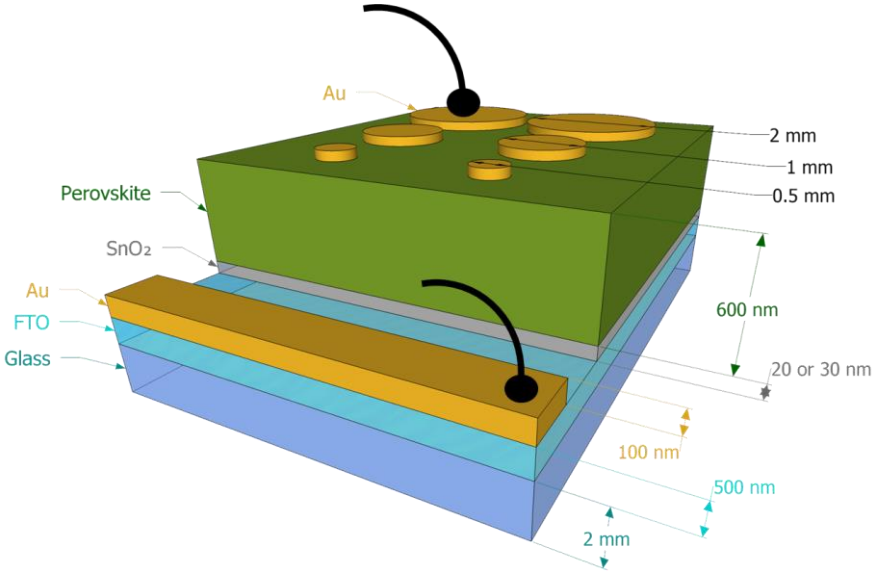


Figure S3 – Metal-Oxide-Semiconductor (MOS) inverted structure. SnO_2 thicknesses of 20 and 30 nm were used. MOS devices with contact diameters of 0.5 mm, 1 mm and 2 mm were used. The layers' thicknesses are also shown. Not at scale.