Evidence of Heat-Assisted Atomic Migration in GeSe Self-Selecting Memory at High Operating Current Density

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In this work we study the operation of a GeSe ovonic threshold switch (OTS) as a self-selecting memory cell based on the polarity effect. From the observed operating current (I_{op}) dependence and area scaling behavior we confirm the critical role of Joule heating in ensuring exceptionally large memory window in this material. The underlying mechanism is further investigated by means of chemical analysis and is confirmed to be caused by polarity-dependent atomic migration under high-I_{op} regime, consistent with elemental segregation due to electronegativity contrast. More specifically, we observe selective diffusion of Ge atoms through the TiN layer into negatively-biased top electrode stack. At the same time, there is no sign of a similar process for Se atoms under opposite voltage polarity. Based on these observations, we propose a novel memory concept utilizing a selective diffusion barrier. Furthermore, under low-I_{op} regime no major composition change was observed, leaving room for alternative interpretation of the polarity effect under such conditions. Finally, we demonstrate functional GeSe OTS-only memory fabricated with atomic layer deposition (ALD), making it suitable for vertical 3D integration to enable low-cost applications.

1. Introduction

Ovonic threshold switches (OTS) are commonly considered for the role of selector devices in cross-point memory arrays, typically in combination with a phase-change memory (PCM). [1–3] However, integration of dissimilar materials in selector and memory elements is challenging, prompting the development of self-selective memory technology.[4] We have previously reported a polarity effect in amorphous chalcogenides, where the threshold voltage (V_{th}) of an OTS can be reliably modulated by the polarity of the previously applied Write pulse.[5] This effect is sufficiently pronounced in Se-based SiGeAsSe material, resulting in successful demonstration of memory functionality.[6,7] Recent works further confirm the promising performance of this novel memory concept.[4,8,9] We have also shown that under certain conditions GeSe can exhibit an exceptionally large memory window (MW).[10]

In order to enable further device and material optimization necessary for successful adoption of this technology a thorough understanding of the mechanism behind the polarity effect is necessary. This work aims at testing one of the hypotheses proposed in the literature, namely field-driven atomic segregation within the chalcogenide film.[4,8,9] Here, we focus on a simple binary Ge_xSe_{1-x} composition. In addition, we investigate the impact of operating current and device area. From the performed physical analysis we confirm substantial atomic migration only at high current density regime and propose a novel memory concept based on the observed phenomenon.

2. Polarity-induced V_{th} shift in GeSe

2.1. Bipolar operation of the OTS selectors

We have previously reported on the possibility of utilizing an OTS selector as a self-selective memory cell, thanks to the polarity effect observed in certain chalcogenide materials. We have identified Se-based compositions as the most promising candidates for this role. In particular, binary GeSe was shown to experience anomaly large memory window (MW) under high-I_{op} conditions.[10]

An example of the bipolar operation of GeSe is shown in **Figure 1**a. A clear memory window can be observed, depending on the polarity of the Write pulse. The extracted V_{th} values and calculated *polarity-induced V_{th} shift* (ΔV_{th}) are reported in Figure 1b. Here we adopt the following convention for ΔV_{th}:

$$\Delta V_{th} = |V_{th}^{opp}| - |V_{th}^{same}| \quad (1)$$

where V_{th}^{opp} is the threshold voltage extracted in the *opposite* polarity with respect to the previously applied Write pulse, while V_{th}^{same} is Vth for same Read and Write pulse polarities. Note, that here absolute value of the Write polarity determines the resulting V_{th} state. Namely, positive ("P") pulse results in the low-V_{th} state for both POS and NEG read-out polarity, while negative ("N") yields high-V_{th} state, also irrespective of the Read direction. According to the Equation (1), this results in a negative value of the extracted ΔV_{th} in the negative branch ($\Delta V_{th}^{NEG} < 0$). This is in contrast to the previously reported behavior in SiGeAsSe material, where Vth is sensitive to the relative polarities of Read and Write pulses.[7]

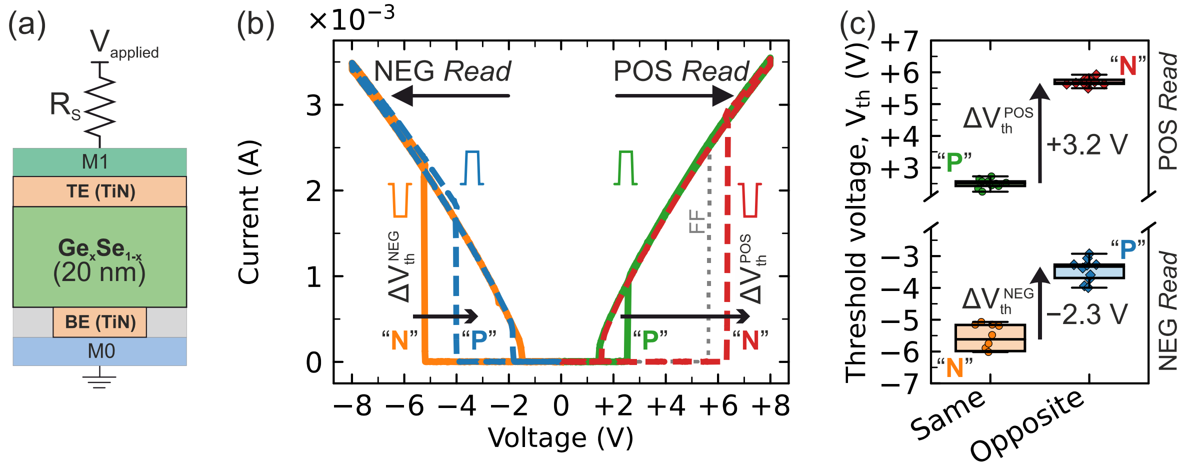

Figure 1. (a) Schematic of an investigated GeSe OTS device. (b) I-V characteristics of GeSe OTS measured after different polarity of the previous (Write) pulse and (c) distribution of the extracted V_{th} values, showing strong polarity dependence with exceptionally large memory window ($MW^{POS} > 3V$).

Note, that the V_{th} shift is so large that in the "N" state V_{th} becomes larger than the first-fire value (V_{FF}). Moreover, we find that in addition to V_{th} shift, the sub-threshold characteristics are also very sensitive to the Write polarity, as illustrated in **Figure 2**a, which shows the DC I-V characteristics (overlayed with AC switching data). One can see that leakage current (I_{leak}) is drastically reduced in the "N" state, whereas device exhibits noticeably higher I_{leak} in the "P" state. In fact, under certain conditions, the I_{leak} in the "N" state can be made smaller than the sub-threshold current of the pristine film before the forming pulse. Importantly, such a pronounced change is recoverable and the same device can be cycled repeatedly between the two states.

2.2. PVD vs ALD GeSe

One of the benefits of the GeSe material compared to SiGeAsSe is the fact that it is a simple binary composition. This implies that it is relatively easy to synthesize using atomic layer deposition (ALD) process, which is crucial to enable true vertical 3D integration.[11] We have developed an ALD process for GeSe deposition and successfully integrated it in working device. The resulting AC and DC characteristics of ALD GeSe are shown in Figure 2b. The observed behavior is qualitatively similar to physical vapor deposition (PVD) GeSe, while there are some quantitative differences.

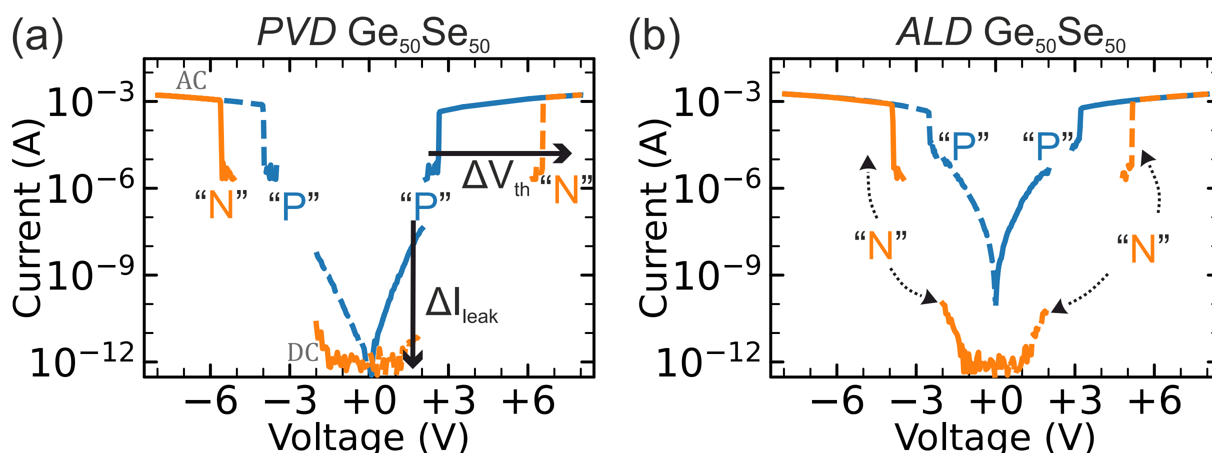

Figure 2. (a) DC I-V characteristics overlayed with AC switching data of a PVD GeSe sample, showing a dramatic modulation of the sub-threshold conduction, in addition to V_{th} shift. (b) Same for ALD GeSe with the same *nominal* composition and thickness (a).

Namely, under similar operating conditions, ALD sample shows higher sub-threshold leakage, as well as reduced magnitude of the polarity effect. Both of these can be attributed to the differences in as-fabricated layer thickness and composition of the two samples. While the nominal thickness of both films was targeted to be 20nm, the ALD-deposited GeSe turned out to be thinner (t≈15nm) compared to that fabricated with PVD (t≈22nm), as demonstrated in **Figure S3**. This is in line with lower V_{th} in ALD device, due to smaller actual thickness. Additionally, we noticed that the composition of the PVD sample deviated slightly from the target Ge/Se ratio of $Ge_{0.5}Se_{0.5}$ towards Se-rich Ge_xSe_{1-x} (x<0.5), as observed by EDS analysis in **Figure S4**. Se-rich Ge_xSe_{1-x} is known to be more insulating (therefore, higher V_{th}), which is also in line above-described data. Throughout this work, both PVD and ALD films will be investigated, assuming that both experience similar behavior (as confirmed in **Figure S6**).

3. Dependence on operating conditions

3.1. Impact of operating current (I_{op})

We have reported previously that such a strong memory window in GeSe is only present under high-I_{op} regime.[10] Here, we present an extensive study of the impact of I_{op} on memory behavior. The results are summarized in **Figure 3**.

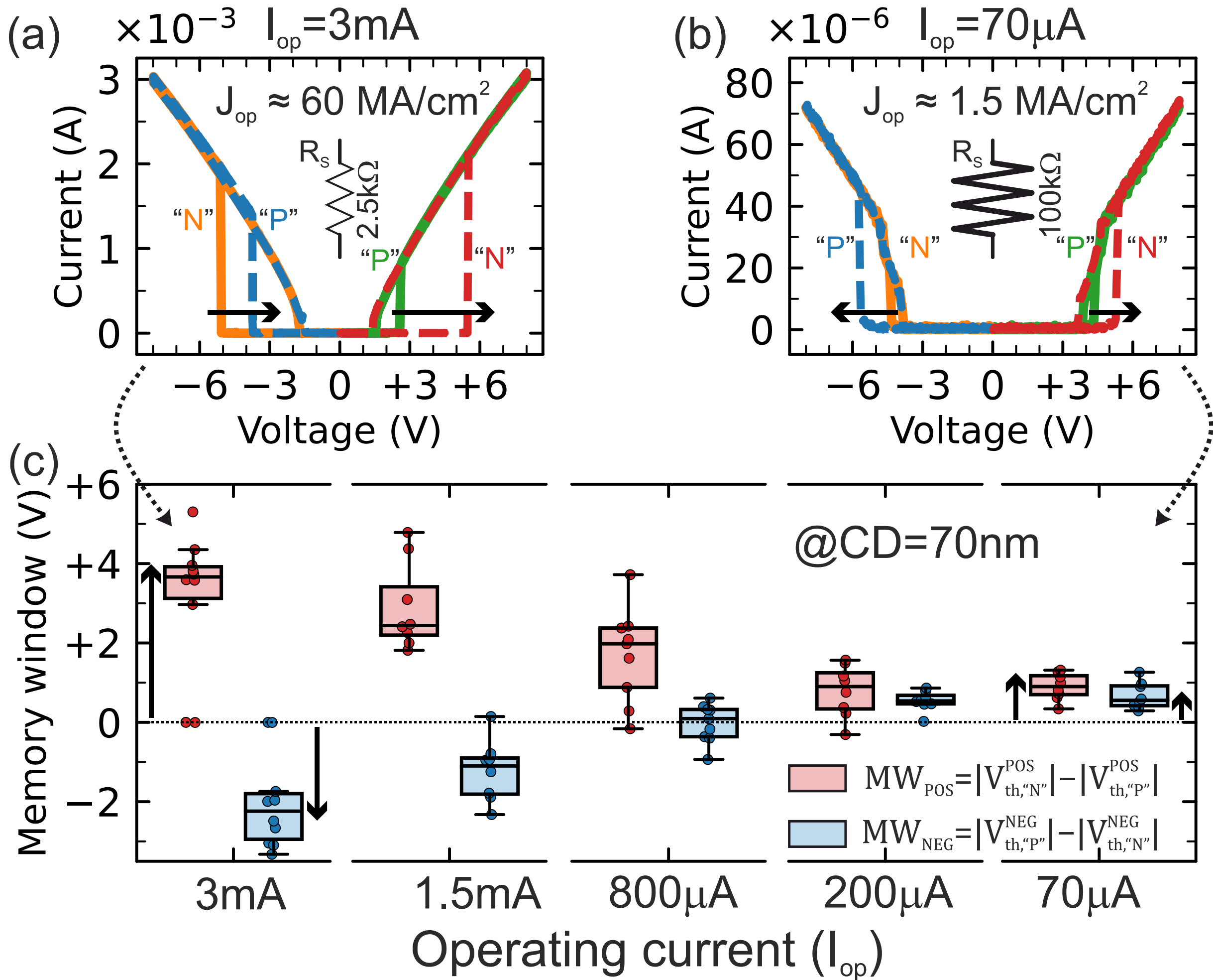

Figure 3. Impact of operating current (I_{op}). Example of an I-V at (a) high-I_{op} and (b) low-I_{op} regimes. (c) Extracted memory window for various I_{op} conditions. Notice, the qualitative difference in behavior (in terms of the direction of the V_{th} shift) upon the reduction in I_{op}. Additionally, the anomaly large ΔV_{th} only present under high-I_{op} regime.

It is clear that there are both qualitative and quantitative differences in behavior, depending on the I_{op} value. First, MW is much larger at high-I_{op}, especially in the positive read-out direction (MW^{POS}). At the same time, the direction of the V_{th} shift in negative read-out direction changes. As can be seen from Figure 3c, the reversal of MW^{NEG} sign happens around I_{op}~1mA. This may suggest that there two competing mechanism, with one of them being dominant at a given I_{op}

condition. For example, it is reasonable to assume that increased I_{op} will favor atomic migration due to Joule heating and subsequent internal temperature rise. The nature of this process in this particular device will be examined in **Section 4.2** in detail.

On the other hand, we have proposed previously that under low-I_{op} condition the polarity effect may be caused by a purely-electronic phenomenon.[5] In this respect, it is important to point out that under low-I_{op} regime, the behavior of GeSe qualitatively resembles that of SiGeAsSe, with relative Read & Write polarity controlling the V_{th} state.[7] This is also manifested in a similar polarity dependence of sub-threshold current (see **Figure S9**). Alternatively, the low-I_{op} behavior may also be attributed to a atomic rearrangement, but on a very local scale (hence not requiring a lot of energy to activate this process), as will be discussed in **Section 4.4**.

3.2. Impact of device size and the link with operating current density (J_{op})

In this work we complement the study of I_{op} dependence with the investigation of the impact of active area of the device (determined by the diameter of the bottom electrode, i.e., critical dimension - CD) to assess the impact of *current density*. **Figure 4** shows the area scaling of MW. Here, we focus on the high-I_{op} regime by keeping constant $I_{op} \approx 2mA$. A clear size dependence can be observed, with larger devices experiencing a decrease in MW. Moreover, increasing area also leads to a reversal of the direction of MW^{NEG} shift. It is in line with I_{op} dependence in Figure 3, suggesting that MW is controlled by current density (J_{op}). This is likely caused by the increased Joule heating under high-J_{op} conditions.

4. Investigation of the switching mechanism via chemical analysis

4.1. Characterization procedure

One of the possible hypotheses suggested in the literature associates the polarity effect to a field-driven atomic migration, with different species segregating at opposite interfaces due to the differences in electronegativity.[12] In order to test it, we have performed a TEM analysis, combined with EDS elemental analysis. For this, two samples have been used, each programmed with different pulse polarity prior to TEM specimen preparation. Note, both samples also underwent the same series of bipolar switching pulses (40 in total) to confirm the memory functionality, followed by the final programming pulse (positive for sample "P", and negative for sample "N"). **Figure 5**a shows the structure of the investigated device. Figure 5b presents a combined EDS elemental mapping of a pristine (non-switched) device.

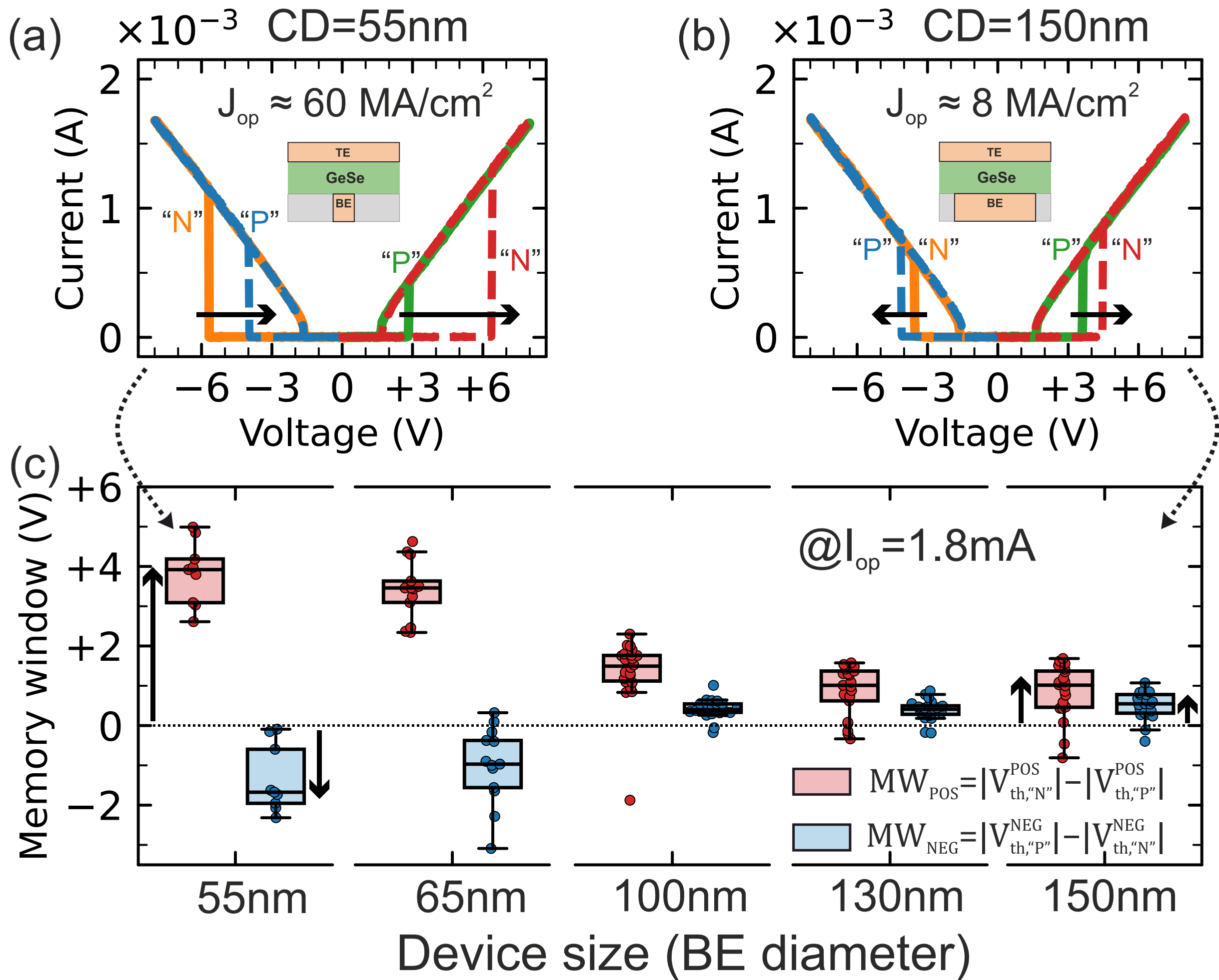

Figure 4. Impact of device size (bottom electrode diameter) at high I_{op}. Representative I-V characteristics for (a) small-area CD=55nm and (b) large-area CD=150nm devices. (c) Extracted MW for various CDs. Similar trends compared to the I_{op} dependence can be observed, suggesting that the type of behavior is determined by the operating *current density*.

4.2. High-J_{op} regime

First, we consider the sample programmed with high current I_{op}=1.8mA (and small area) to investigate the high-J_{op} mechanism. For this experiment, a device with ALD GeSe is used.

Figure 5c shows the spatial distribution of the relevant atomic species after positive Write, and Figure 5d – same for sample programmed with negative pulse. Corresponding vertical line scans are shown in Figure 5e,f. In the case of sample "P", the Ge/Se ratio of Ge_xSe_{1-x} film is maintained close to x=0.5 (i.e., target $Ge_{0.5}Se_{0.5}$ composition of the pristine film, see Figure S4a) throughout the full thickness of the chalcogenide film. In contrast, the "N" sample experiences a dramatic compositional change. Most notably, the bulk of the Ge_xSe_{1-x} film (close

to the BE interface) is noticeably enriched with Se (x < 0.5). This helps explain the electrical properties of the device after negative Write polarity (high V_{th} & low I_{leak}), since Se-rich GeSe is known to be more insulating due to larger mobility gap.

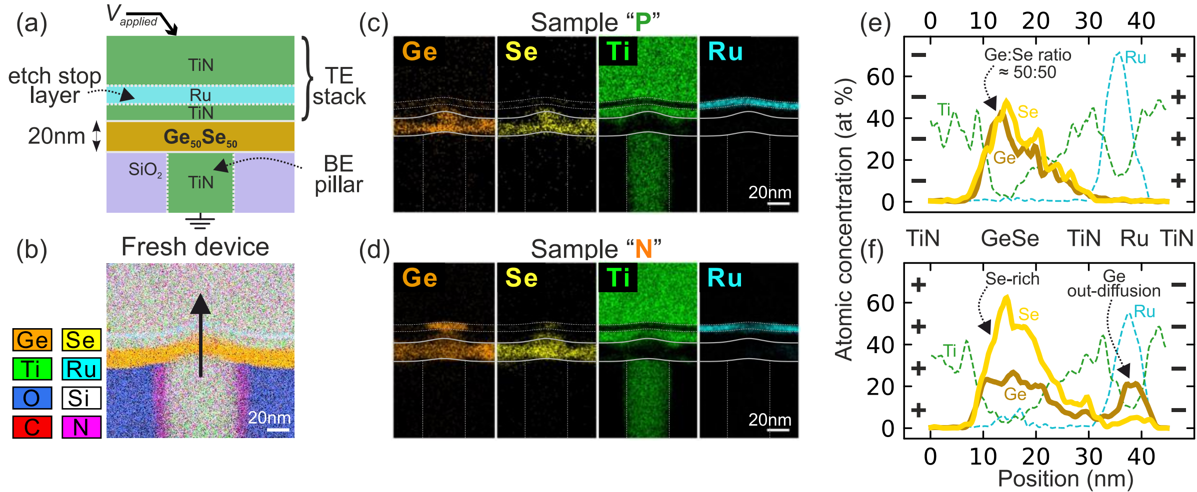

Figure 5. Chemical analysis performed on the samples programmed with different pulse polarities in the high-I_{op} regime. (a) Schematic of investigated device (ALD GeSe, CD=55nm). (b) EDS elemental map of a pristine device for reference. (c) and (d) show in-depth distribution of the relevant species in the samples programmed with positive and negative pulse polarities, respectively. (e) and (f) show the corresponding vertical EDS line scans. Under positive Write (sample "P") the composition is close to the target 0.5/0.5 Ge/Se ratio. On the other hand, sample "N" exhibits noticeably Se-rich GeSe bulk, with excess Ge accumulating in the TE stack (namely, within Ru layer).

Perhaps more interesting is the reason for the Ge deficiency of the GeSe film. We observe that negative polarity (as applied to the TE) induces a migration of Ge atoms *out* of the GeSe layer and into the TE stack. Figure 5f shows that Ge accumulates within the Ru layer (which is used here as an etch stop layer during TE patterning). The direction of Ge migration is consistent with the electronegativity-dependent atomic migration hypothesis[4,12] – Ge has lower electronegativity compared to Se, and therefore tends to move towards negatively biased electrode (TE in the case of sample "N").

Note, that in the process Ge seems to diffuse through the relatively thin (~6nm) TiN layer (which acts as a direct TE contact to GeSe). Interestingly, this is not the case for Se atoms under a positive bias polarity – there is no Se detected in TE stack in sample "P" (Figure 5e). This suggests that TiN acts as a *selective diffusion barrier*, allowing the movement of Ge while

effectively blocking Se. Indeed, the use of TiN as a Se diffusion barrier has been reported in the literature.[13] Following the above discussion, the diffusion of Ge through TiN barrier may be assisted by the increased temperature due to Joule heating. Also interesting is a preferential accumulation of Ge within the Ru layer, which may be due to a favorable thermodynamic driving force to form stable Ru_2Ge_3 binary compound,[14] while there is no stable Ti-N-Ge compound.[15,16] It has also been reported that Ge exhibits limited solubility in TiN[17] and tends to segregate at the surface of the TiN grain boundaries.[18] This is in line with the apparent lack of interaction between diffusing Ge atoms and TiN barrier layer.

It is also important to stress that this process is reversible, and under the application of subsequent positive pulse Ge can be expelled from the Ru "reservoir" back into the bulk of GeSe film. This is supported by electrical data, since polarity-induced V_{th} shift is reversible. Moreover, as mentioned above, both samples studied with TEM/EDS analysis have been subjected a bipolar cycling, prior to applying the final programming pulse. This means that also in sample "P" (Figure 5c,e) at some point Ge have been present in the TE stack (after negative pulses, see **Figure S7**), but there is no sign of it after the last applied positive programming pulse. It also implies that a single pulse (8V/10us) is sufficient to induce such a dramatic composition change. Finally, it is worth mentioning the potential role of interaction between TiN electrodes and OTS film, as reported previously.[19,20] While some Ti may diffuse into GeSe during programming, it is unlikely to be responsible for the dramatic changes in V_{th} and I_{leak} (see **Figure S10**).

4.3. Low-J_{op} regime

Next, we perform a similar analysis on the samples programmed with lower operating current (I_{op}=150μA). This experiment has been performed with PVD GeSe.

The results are shown in **Figure 6**. First of all, we see no Ge out-diffusion into the TE stack after negative programming pulse. Moreover, there seems to be no visible composition change due to voltage polarity at low-J_{op} regime, as demonstrated in Figure 6e,f. For a direct comparison between Ge/Se ratio in the two samples see **Figure S5**. While there are some minor differences in the composition between the two sample, they may be caused by the experimental error of the EDS technique.

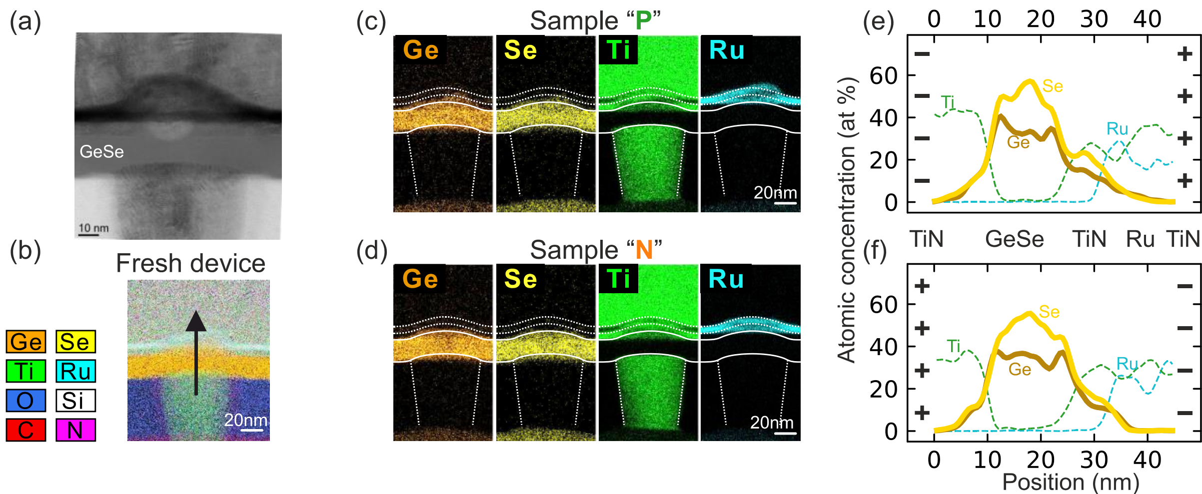

Figure 6. Chemical analysis performed on the samples programmed with different pulse polarities in the low-I_{op} regime (PVD GeSe). No Ge out-diffusion is observed. Also, no significant composition change within the GeSe occurs.

Additionally, the analysis is further complicated by the irregular shape of the GeSe film. It is caused due to the dome-like topography of the bottom TiN electrode (after the CMP step) which is then transferred to the layers deposited on top of it (see Figure 6a). This results in an apparent overlap between GeSe and TE layers, which is in fact just a projection effect due to the EDS signal coming from different depths of the lamella. Therefore, in the current device it is not possible to accurately probe the composition of GeSe close to the interfaces (where one would expect the strongest segregation, if such is present). Note, that while there is no noticeable composition between the two sample, electrically they do exhibit different V_{th}.

4.4. Discussion of the mechanism

We observe strong atomic migration under high-J_{op} regime, as schematically depicted in **Figure 7**b. Here, TiN TE layer acts as a selective diffusion barrier. In this case, the Ge diffusion is driven by electric field and/or current. The fact that such a pronounced material change is only observed at high current density, while no major atomic rearrangement is observed under low-J_{op} conditions, seems to confirm that the underlying diffusion process is accelerated by the temperature increase due to self-heating.

As for the low-J_{op} regime, we did not find conclusive evidence of elemental segregation. Nevertheless, it is still plausible that some atomic migration is happening on a local scale (i.e., below the sensitivity of EDS). Considering that OTS conduction mechanism itself is a (volatile) filamentary process, one may expect to have high current density, promoting a composition

gradient locally around the conduction cluster as depicted in Figure 7a. If this is the case, a more sophisticated characterization technique would be required to observe it (e.g. atom probe tomography).

Alternatively, the observation in Figure 6 may indicate that at low-J_{op} there is indeed no atomic migration. Instead, the mechanism at such conditions would be purely electronic in nature.[21] For example, we have developed a model capable of explaining the polarity effect via field-sensitive defect states (unpublished).

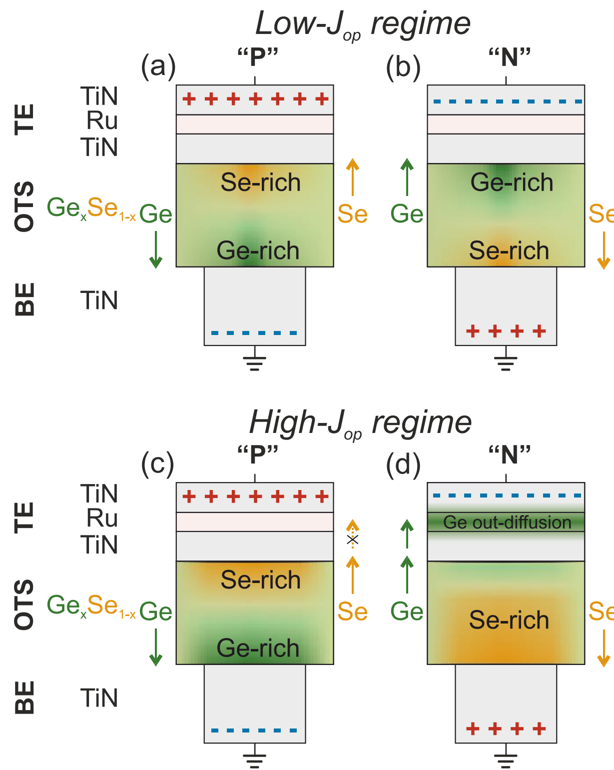

Figure 7. Hypotheses of the physical mechanisms behind polarity effect under (a,b) low-J_{op} and (c,d) high-J_{op} regimes.

5. Memory cell with selective diffusion barrier

Finally, the proposed concept, exemplified by the GeSe device discussed above, can be generalized, using schematics shown in **Figure 8**. It includes the following essential parts: (i) a specific OTS material, (ii) atomically selective diffusion barrier. These components are selected based on the following considerations. First, OTS composition must contain species with different electronegativities, so as to enable field-driven elemental segregation of these species under bipolar operation. Second, the barrier material must allow the diffusion of one type of the

species, while blocking the other. This way, the composition of the active bulk of the OTS material can be controlled to dynamically tune its properties.

Optionally, to further improve the proposed device, it may be beneficial to include an additional "reservoir" layer to store the species that diffuse through the selective barrier. Additionally, it may be used to promote such migration, e.g. by introducing favorable thermodynamic reactions. Importantly, this reservoir material must remain conductive even when a significant amount of species A are stored within it.

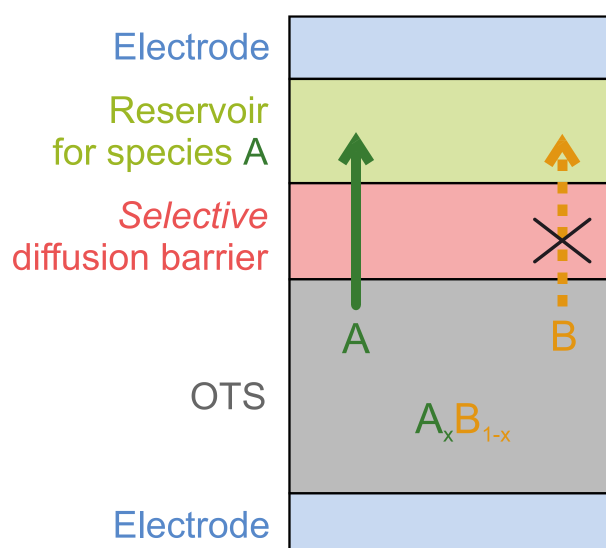

Figure 8. Generalized proposal for a novel memory cell based on the *selective diffusion barrier*.

Note, that both barrier and reservoir properties may be temperature-dependent. Considering the Joule heating generated during the device operation, it may be possible that the above-specified condition may be fulfilled at elevated temperature to enable the proposed device. In the implementation described above, the role of OTS material is played by Ge_xSe_{1-x}, TiN acts as selective diffusion barrier (blocking Se) and Ru layer is a reservoir for Ge atoms.

It is worth mentioning, that the proposed concept resembles the electrochemical random access memory (ECRAM),[22,23] with a two-terminal device structure.[24,25] But thanks to the threshold switching chalcogenide active layer it also introduces a built-in non-linearity, resulting in a self-selective cell. Moreover, a design with a diffusion barrier can ensure sufficiently long retention. However, this would come at the cost of rather high energy required to activate the diffusion process, and the associated increase in power consumption. Further stack optimization may be

necessary to achieve desirable characteristics. For example, by introducing a thinner barrier layer, as well as finding a more suitable combination of barrier and OTS materials. With this work we would like to encourage future research in this direction.

5. Conclusion

In this work we perform an in-depth analysis of the polarity effect in Ge_xSe_{1-x} threshold switches under different operating condition. By means of TEM/EDS analysis we establish the origin of the abnormally large memory window under high-J_{op} regime. It is shown to be caused by the reversible polarity-dependent migration of atoms from the chalcogenide film into the top electrode stack. In particular, we observe selective diffusion of Ge through a thin TiN top electrode layer, into the wider TE stack, when it is biased with negative polarity. This movement is consistent with the field-driven atomic migration due to the relative difference in electronegativity of the constituent species of the GeSe. Interestingly, no Se out-diffusion is observed, resulting in highly Se-rich compositions in one of the states. Therefore, resulting in a strong modulation of the threshold voltage and sub-threshold conduction, depending on the polarity of the Write pulse. We propose a way of generalizing this phenomenon with a novel memory cell based on the selective diffusion barrier.

The underlying elemental segregation process is believed to be assisted by the internal temperature rise to significant Joule heating under high-J_{op} conditions, as evidenced by the I_{op} and area dependence. At the same time, we did not found any indication of atomic migration under low-J_{op} conditions. This is despite the fact that, although smaller, polarity-induced V_{th} shift is also present under such conditions. This suggests that in this case the atomic rearrangement, if present at all, only happens locally. Further analysis with a more sensitive characterization technique with 3D resolution (e.g., atom probe tomography) would be needed to test this hypothesis. Alternatively, this may point to the fact that the mechanism under low-J_{op} is due to an electronic effect. An extensive simulation work is currently underway to corroborate this possibility.

6. Experimental Section/Methods

Device fabrication: To measure the experimental parameters, a set of devices different OTS material compositions was fabricated. Device architectures investigated consisted of a mushroom cell. The device consisted of an OTS film sandwiched between the top (TE) and bottom (BE) electrodes. In a mushroom cell the BE (TiN) was etched into a pillar with critical dimension (CD) defined down to 55nm. A 20nm (nominal) thick OTS film together with TE metal (TiN) was deposited on top of BE, resulting in a mushroom-type cell structure. Investigated composition consisted of a binary Ge_xSe_{1-x} material systems (with nominal x=0.5), deposited by means of physical vapor deposition (PVD)[26] or atomic layer deposition (ALD) technique.

Electrical characterization: The devices were electrically characterized using a series of triangular ac pulses with a rise time of t_{rise}=5 μs with alternating voltage polarity. From these measurements the threshold voltage (V_{th}) and the corresponding memory window (MW) values were extracted. Additionally, sub-threshold leakage was characterized by means of a dc measurement. Structures with nominal CD ranging from 55nm to 150nm were tested (CD=70nm assumed if not specified explicitly). An integrated series resistor (R_s) was used to limit the operating current in the ON-state (I_{op}).

TEM/EDS analysis: Device structure and chemical composition has been studied by means of transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS), as detailed in Supporting Information (**Figure S2**). 2D elemental mapping as well as vertical EDS line scans have been used to study the spatial distribution of the relevant atomic species. For each of the operating conditions, three different TEM samples have been prepared. One was a pristine device used as a reference. The other two have been electrically programmed with opposite pulse polarities (see Figure S7 for details).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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This work investigates the polarity effect in Ge_xSe_{1-x} threshold switches under various operating conditions. The mechanism behind the high-current behavior is elaborated by means of elemental mapping and is shown to be caused by atomic migration within device structure. At the same time, no major composition change is observed at low operating current.

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Evidence of Heat-Assisted Atomic Migration in GeSe Self-Selecting Memory at High Operating Current Density