

An All-Silicon 4x56 Gbit/s NRZ, 1pJ/bit Optical Receiver with Ge-on-Si PDs and 28nm CMOS TIA Array

Bruno Govaerts⁽¹⁾, Xin Wang⁽¹⁾, Axl Bomhals⁽¹⁾, Jakob Declercq⁽¹⁾, Arijit Karmakar⁽¹⁾,
Geert Van Steenberge⁽²⁾, Jeroen Missinne⁽²⁾, Cedric Bruynsteen⁽¹⁾, Nishant Singh⁽¹⁾,
Guy Torfs⁽¹⁾, Johan Bauwelinck⁽¹⁾, Xin Yin⁽¹⁾, Peter Ossieur⁽¹⁾

⁽¹⁾ IDLab, INTEC, imec-Ghent University, 9052 Ghent, Belgium, bruno.govaerts@imec.be

⁽²⁾ CMST, imec-Ghent University, 9052 Ghent, Belgium

Abstract We demonstrate a low-power (1 pJ/bit), C-band 4x56 Gbit/s NRZ optical receiver constructed from a 28nm CMOS transimpedance amplifier and a Silicon PIC containing a Ge photodetector array. The receiver showcases low-complexity, and low-latency performance for use with one-hop optical switching in optical IO applications.

Introduction

Today's predominant networking architectures rely on multi-hop systems with electrical switches and utilize transceivers with very large bandwidths that require multi-level modulation such as PAM4 and digital signal processing (DSP) using advanced CMOS nodes^{[1],[2]}. This results in network latency which is hard to predict and changes over small timescales depending on load. In contrast, there is a growing need for time-sensitive applications such as radio access networks, industrial automation, and disaggregated resources^[3]. Time-sensitive networks require a different approach compared to datacenter networks in order to meet latency requirements where optical switching has emerged as a solution to reduce switching latency. Further, such machine type communications do not need extreme bandwidths but prefer simpler and lower cost solutions. Simple modulation such as NRZ can easily be received and processed^[4] while lower rates can alleviate DSP and equalization overheads.

The study of low-complexity receivers remains active for low-latency time-sensitive operations in various CMOS nodes, all employing simple NRZ modulation^{[4]–[7]}. A 50-Gb/s NRZ receiver targeting low-latency operation in 45-nm SOI CMOS was demonstrated, although optical assembly and measurements were not presented^[4]. A 60-Gb/s NRZ optical receiver with low-latency digital CDR in 14-nm CMOS FinFET was also presented where they demonstrate optical assembly and measurements although only a short 7m link was demonstrated^[5]. For both previous papers only single-channel assemblies were demonstrated which have fewer impairments from crosstalk. A 16-channel optical receiver in a 65-nm CMOS chip has recently been demonstrated, which considers channel crosstalk, although only up to 25 Gb/s per channel^[6].

This paper presents a 4x56 Gb/s all-silicon op-

tical receiver as a solution for time-deterministic and time-sensitive networks. It focuses on photonic components and interface electronics, integration, assembly and packaging technologies, to be used for one-hop optical switching in radio access networks, machine type communications and in disaggregated resources as shown in Fig. 1. The paper starts with a description of the receiver architecture, the photonic and electronic integrated circuits, and the assembly of these. Following that, the experimental setup is described, and experimental results are presented. Finally, a conclusion is drawn and the main achievements highlighted.

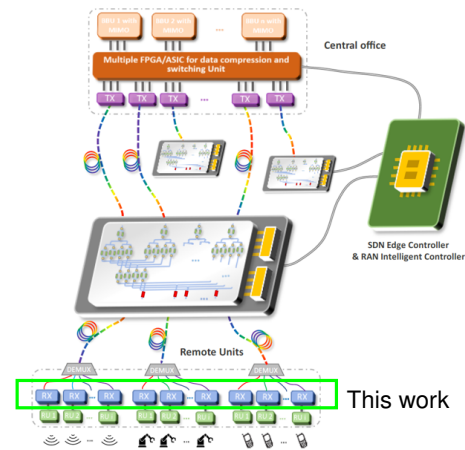


Fig. 1: System concept for one-hop optical switching in time-deterministic and time-sensitive networks such as radio access networks, machine-type networks and disaggregated resources.

Optical Receiver Architecture and Assembly

The four-channel receiver architecture is presented in Fig. 2. This architecture comprises a photonic integrated circuit (PIC) and an electronic integrated circuit (EIC) interconnected via wirebonds. The PIC is manufactured in imec's iSiPP200 silicon photonics platform. The PIC contains one grating coupler and one photodiode (PD) per EIC channel. The PD has a bandwidth of

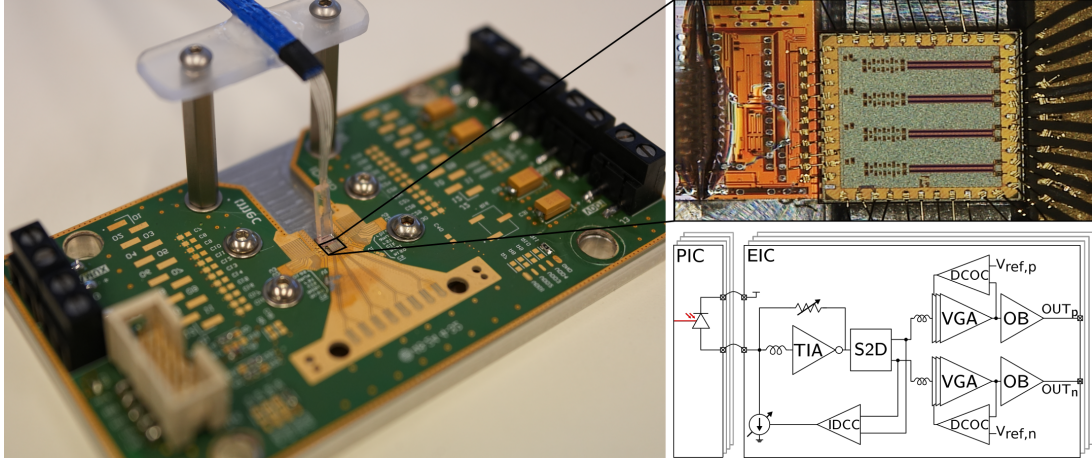


Fig. 2: The optical receiver assembly showing both a PIC and an EIC mounted on a heatsink with a glued fiber array. A diagram of the EIC architecture shows the working of the chips.

60 GHz and a responsivity of 0.89 A/W in the C-band^[8].

The EIC features a single-ended inverter-based shunt-feedback transimpedance amplifier (TIA) with inductive peaking^[9]. The feedback resistance is digitally programmable, enabling adjustments of both gain and bandwidth. The single-ended output signal of the TIA is converted to a pseudo-differential signal in the single-ended-to-pseudo-differential (S2D) block. This voltage signal is then amplified by three digitally programmable inverter-based Cherry-Hooper^[10] variable gain amplifier (VGA) stages. An output buffer (OB) matched to 50 Ω facilitates off-chip signal transfer. Additionally, an input DC current cancellation (IDCC) loop is incorporated to sink the DC current of the PD by minimizing the differential DC voltage between both differential branches. Across the VGA stages a DC offset cancellation (DCOC) ensures the inverters stay biased at half the supply voltage. The reference voltage for the loop is programmable to accommodate for any process, voltage, and temperature variations.

The assembly of the PIC and the EIC is depicted in Fig. 2. Both chips are attached to an aluminum base plate using silver epoxy. The aluminum base plate is precisely milled to compensate for any height difference between the PCB, PIC and EIC. Extra care was taken to ensure the dicing street was close to the high-speed pads, and by using wedge-wedge wirebonds with minimal loop height

the parasitic inductance is kept minimal. A fiber array was aligned with the grating coupler array on the PIC and attached with UV-curable epoxy. Additionally, a strain relief for the fiber array was added to enhance the mechanical stability of the fiber array.

Electro-Optical Experiments

The measurement setup used to characterize the optical receiver is presented in Fig. 3. An arbitrary waveform generator (AWG) (Keysight M9502A) generates a NRZ waveform based on a $2^{13} - 1$ pseudo-random bit sequence (PRBS) bitstream. An amplifier (SHF S807 C) is connected after the AWG to compensate the reduced signal swing of the single-ended mach-zehnder modulator (MZM) (Sumitomo Osaka Cement co T.MXH1.5-75-ADC-LV). The MZM modulates a 1550 nm laser while being biased at the quadrature point. The output of the MZM is fed to an erbium-doped fiber amplifier, to compensate for the losses of splitting the signal at the transmitter side. The signal is transmitted through a 2 km standard single-mode fiber (SSMF) and connected to a variable optical attenuator (VOA) which controls the optical power. To determine the optical modulation amplitude (OMA) received at the PD, the photocurrent of the PDs is measured. The VOA is connected to an optical switch which directs the signal either to the device under test (DUT) or to a reference PD. The reference PD (Finisar XPD3120R) is connected to a

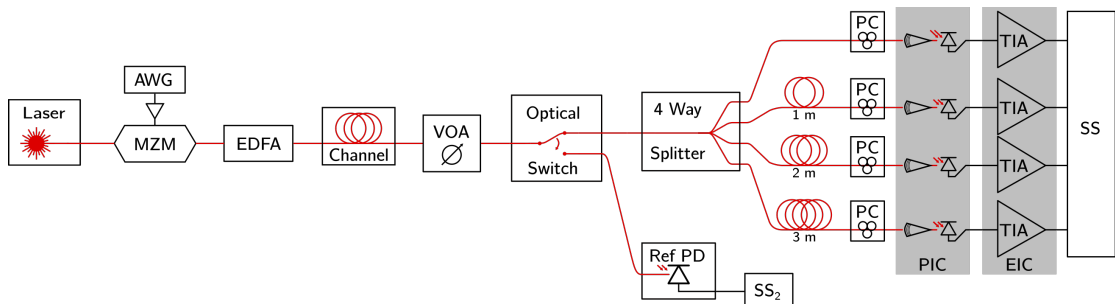


Fig. 3: Measurement setup consisting of a four-channel transmitter, a reference receiver and a four-channel optical receiver.

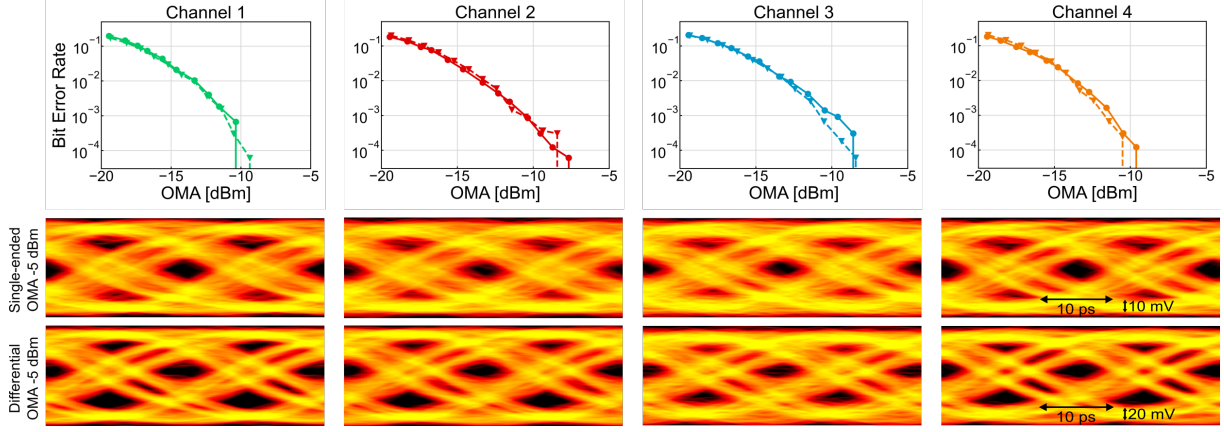


Fig. 4: The BER and eye diagram results for 4-channel simultaneous transmission of 56 Gb/s are shown. Single-ended and differential BER results are represented by dashed and solid lines, respectively. Channels 1 to 4 are depicted from left to right.

sampling oscilloscope (Keysight 86100D) to measure the extinction ratio (ER) of the optical signal. The signal directed to the DUT is split using a four-way splitter with the outputs connected to different fiber lengths to decorrelate the PRBS13 signals between channels. Fiber lengths of 1, 2 and 3 meters were used while the remaining channel was connected directly. A polarization controller (PC) is added to each channel to optimize the polarization for the grating couplers on the PIC. The four-channel outputs of the TIA are connected via a TR70 connector to a second sampling oscilloscope (Keysight N1000A), which captures the eye diagrams of the optical receiver.

Channel noise is measured while the VOA is turned off and no signal is applied. The input referred noise is calculated using the simulated transimpedance gain and the output noise voltages. The bit error rate (BER) is obtained by performing offline error counting on the captured waveform data. The equalization function of the AWG compensates for the limited bandwidth of the transmitter and the output traces of the PCB traces with the TR70 connector. This function was calibrated on the reference link.

The TIA shows a simulated bandwidth of 25 GHz and a gain of 67 dB Ω . An input-referred noise of 1.25 μ A RMS is found. At a data rate of 56 Gb/s, each channel consumes 63 mA from a 900 mV supply resulting in a power efficiency of 1.01 pJ/bit. Fig. 4 presents single-ended and differential BER curves for each channel during simultaneous transmission of 56 Gb/s data. Note that for the differential output signals only two channels could be measured simultaneously, due to the limited input channels of the sampling oscilloscope. Each point of the BER includes at least 10 errors to ensure statistical relevance. The BER curves of the different channels indicate that for an optical input power above -9, -7, -8 and -9 dBm no errors were found for channels 1, 2, 3 and 4, respectively. All the channels perform similarly, with channel 4 exhibiting slightly better performance.

This is attributed to channel 4 having a separate power supply, while the other three channels share a supply, resulting in less crosstalk induced on this channel by the other channels. This test was intentional by design as three channels were placed on the same supply and one on its own supply to evaluate the impact of power integrity which in the end seems to exist but is minimal and does not have a significant effect.

Eye diagrams for both single-ended and differential output signals for each channel obtained during these BER measurements are presented in Fig. 4. These results are obtained without any form of equalization. Both single-ended and differential operation show similar performance.

Tab. 1: Normalized crosstalk coupling between channels.

Victim \ Aggressor	Aggressor			
	CH1	CH2	CH3	CH4
CH1 [dB]	0	-17.7	-19.03	-20.96
CH2 [dB]	-20.27	0	-14.86	-17.51
CH3 [dB]	-23.87	-17.55	0	-15.04
CH4 [dB]	-29.05	-23.55	-18.53	0

The effect of crosstalk between the different channels is investigated by modulating a sinusoidal input signal with a frequency of 10 GHz to the optical carrier of one channel (aggressor) and observing the coupling to the other channels to which no input signal is applied (victims). This crosstalk experiment is summarized in Table 1. The effect of crosstalk is more pronounced for channels located closer to the aggressor.

Conclusions

In this paper we proposed and demonstrated a low-power (1 pJ/bit) four-channel optical receiver compatible with NRZ signals for use in one-hop time-sensitive networks with optical switching for distributed radio access networks, machine type communications and disaggregated resources. Link experiments were conducted with a 2-km SSMF fiber with all channels operating at the same time, showing crosstalk resilience and signal integrity.

Acknowledgements

This work is partly funded by European Union's Horizon Europe Research and Innovation Programmes under Grant Agreement Numbers 101070560 PUNCH and 101070009 Octopus. The authors would like to thank Jasper Jans for wire-bonding.

References

- [1] E.-H. Chen, H. Park, M. Abdullatif, M. Gandara, A. ElShater, A. Khashaba, S.-H. Huang, T.-B. Liu, A. Atharav, J. Lee, Q. Nehal, M. Megahed, Y. Chun, C.-E. Shieh, V. Jolly, S. Kwon, H.-T. Chien, K.-C. Wu, C.-E. Liu, P. Yan, P.-J. Li, C.-H. Chen, T.-S. Lin, P.-C. Liu, and T. Ali, "A 121.5Gb/s DSP-Based PAM-4 Transceiver with 50dB Loss Compensation for Large AI System Interconnects in 4nm FinFET", in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 68, 2025, pp. 1–3. DOI: 10.1109/ISSCC49661.2025.10904601.
- [2] G. de Valicourt, P. Pupalais, R. Giles, M. Lamponi, L. Elsing, S. Liu, B. Sawyer, J. Proesel, S. T. Le, E. Ho, K. Liu, Z. Zhu, S. Corteselli, L. Alloine, C. Daunt, M. Ferriss, B. Rahmani, F. Warning, A. Bruno, S. Abbaslou, M. Zaman, Z. Pan, G. Fischer, G. Reichert, J. George, U. Alakusu, J. Binkley, I. Martinez, K. van Acoleyen, F. Fesharaki, S. Paul, V. Karra, T. Nguyen, N. Machineni, A. Sullivan, D. Assumpcao, and P. Winzer, "1.6-Tbps low-power linear-drive high-density optical interface for machine learning/artificial intelligence", *Opt. Express*, vol. 33, no. 7, pp. 15338–15354, Apr. 2025. DOI: 10.1364/OE.555476.
- [3] G. Van Steenberge, G. Roelkens, P. Ossieur, J. Missinne, J. Van Asch, J. Zhang, S. Qin, J. Van Campenhout, J. Van Kerkhof, M. M. Milosevic, P. Bakopoulos, D. Syrivelis, E. Mentovich, K. Morozov, S. Stracca, A. Bigongiari, T. Joerg, D. Schlick, T. Braun, M. Wöhrmann, R. Gernhardt, Q. Cheng, T. Li, and R. Penty, "Packaging of Ultra-dynamic Photonic Switches and Transceivers for Integration into 5G Radio Access Network and Datacenter Sub-systems", in *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, 2023, pp. 742–747. DOI: 10.1109/ECTC51909.2023.00129.
- [4] Y. Li, S. Chen, Y. Yang, Q. Ma, M. Zhong, Z. Lin, L. Li, G. Li, Z. Zhang, L. Liu, J. Liu, N. Wu, Y. Chen, Q. Peng, and N. Qi, "A 50-Gb/s NRZ Receiver Targeting Low-Latency Multi-Chip Module Optical I/O in 45-nm SOI CMOS", in *2022 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2022, pp. 360–363. DOI: 10.1109/APCCAS55924.2022.10090261.
- [5] I. Ozkaya, A. Cevrero, P. A. Francese, C. Menolfi, T. Morf, M. Brändli, D. M. Kuchta, L. Kull, C. W. Baks, J. E. Proesel, M. Kossel, D. Luu, B. G. Lee, F. E. Doany, M. Meghelli, Y. Leblebici, and T. Toifl, "A 60-Gb/s 1.9-pJ/bit NRZ Optical Receiver With Low-Latency Digital CDR in 14-nm CMOS FinFET", *IEEE Journal of Solid-State Circuits*, vol. 53, no. 4, pp. 1227–1237, 2018. DOI: 10.1109/JSSC.2017.2778286.
- [6] T. Inoue, A. Tsuchiya, K. Kishine, Y. Takahashi, D. Ito, and M. Nakamura, "A 16-Channel Optical Receiver Circuit for a Multicore Fiber-Based Co-Packaged Optics Module in a 65-nm CMOS Chip", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 5, pp. 2514–2518, 2024. DOI: 10.1109/TCSII.2024.3376200.
- [7] P. Davies, "A Reference-Less 24-28 Gb/s NRZ Clock and Data Recovery Macro for Optical Communications Based on a Hybrid Dual-Loop PLL plus DLL in 28nm CMOS", *To be published*, Apr. 2025. DOI: 10.36227/techrxiv.174494649.99903511/v1.
- [8] J. Declercq, B. Moeneclaey, J. Lambrecht, C. Bruynsteens, N. Singh, S. Niu, P. Ossieur, and X. Yin, "A 64-GHz Optical Receiver for 128-GBd Links Using a 55-nm SiGe BiCMOS Traveling-Wave Linear Transimpedance Amplifier", *Journal of Lightwave Technology*, vol. 43, no. 9, pp. 4139–4148, 2025. DOI: 10.1109/JLT.2025.3533200.
- [9] S. Daneshgar, H. Li, T. Kim, and G. Balamurugan, "A 128 Gb/s, 11.2 mW Single-Ended PAM4 Linear TIA With 2.7 Arms Input Noise in 22 nm FinFET CMOS", *IEEE Journal of Solid-State Circuits*, vol. 57, no. 5, pp. 1397–1408, 2022. DOI: 10.1109/JSSC.2022.3147467.
- [10] T. Maekawa, S. Amakawa, N. Ishihara, and K. Masu, "Design of CMOS inverter-based output buffers adapting the cherry-hooper broadbanding technique", in *2009 European Conference on Circuit Theory and Design*, 2009, pp. 511–514. DOI: 10.1109/ECCTD.2009.5275025.