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Optimization of 3D-DRAM Architecture With Oxide-Semiconductor Channel Through Process and Device Simulation

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ABSTRACT Scaling of conventional $6F^2$ 1T-1C DRAM is increasingly constrained as the buried-channel array transistor approaches its physical limits below the 10-nm node. Monolithic three-dimensional (3D) DRAM improves density through vertical stacking, while oxide semiconductor (OSC) channels promise low leakage. In this work we investigate a monolithically stackable OSC-based 3D-DRAM cell using an integrated framework combining process emulation, TCAD device simulation, parasitic extraction, and analytical modeling. Key geometric parameters are analyzed together with storage-node and parasitic capacitances extracted from process-emulated 3D structures. The optimized device achieves an on-current of $14.5 \mu A/cell$ and a storage capacitance of $1.34 fF$. The proposed architecture exhibits favorable intrinsic-cell retention, delay, and energy characteristics, while highlighting remaining challenges in process integration and reliability.

INDEX TERMS 3D-DRAM, oxide semiconductor, IGZO, TCAD simulation, process emulation, parasitic extraction, analytical modeling, monolithic integration.

I. INTRODUCTION

Scaling of the conventional $6F^2$ 1T-1C silicon-based DRAM cell is increasingly constrained as the buried-channel array transistor (BCAT) architecture approaches fundamental physical limits below the 10-nm technology node [1], [2]. These challenges have motivated the exploration of alternative device architectures and channel materials to sustain density and performance scaling [3], [4], [5]. Among the proposed approaches, monolithic 3D-DRAM has attracted significant interest by exploiting the vertical dimension while maintaining a horizontal cell configuration. In such architectures, multiple device layers are fabricated sequentially on a single wafer, and vertical bit-line (VBL) routing is typically employed to reduce effective bit-line capacitance, allowing

also a lower storage capacitor C_s while still fulfilling the sensing margin requirement [6], [7]. The choice of channel material plays a critical role in enabling monolithic stacking. Conventional monocrystalline silicon channels require epitaxial Si/SiGe multilayer stacks, which introduce substantial challenges in defect control as well as in junction and extension formation, both of which are essential for suppressing leakage current (I_{OFF}) and floating-body effects [8], [9]. In contrast, deposited oxide semiconductors (OSCs), such as indium-gallium-zinc-oxide (IGZO), offer intrinsically low off-state leakage and are free from floating-body effects, making them attractive candidates for back-end-of-line-compatible 3D integration [10], [11], [12], [13]. While prior studies have demonstrated the feasibility of OSC-

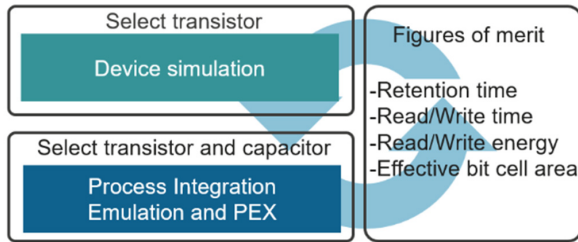


FIGURE 1. Architecture evaluation framework.

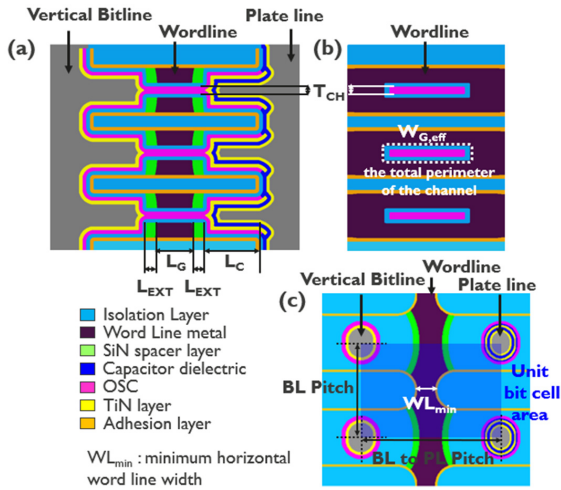


FIGURE 2. 3D Process emulation of the proposed architecture. (a) Cross-section perpendicular to the WL, (b) cross-section parallel to the WL, (c) top view (the shaded region highlights one unit bit cell).

channel-based transistors and capacitorless DRAM concepts, a systematic evaluation of their applicability to monolithically stacked 3D-DRAM remains lacking. The objective of this work is not to predict retention distributions or worst-case array behavior, but rather to provide a first-order evaluation of the relationship between device characteristics, parasitic coupling, and cell-level DRAM performance. To this end, we establish an end-to-end evaluation framework that links device-level optimization with process-aware parasitic extraction (PEX) and analytical DRAM modeling (Fig. 1).

II. ARCHITECTURE DESCRIPTION

A. PROPOSED MONOLITHIC 3D-DRAM ARCHITECTURE

Fig. 2. illustrates the proposed monolithic oxide-semiconductor 3D-DRAM architecture. A full process flow for this structure is developed using SEMulator3D [14], including the vertically routed bit line (BL), stacked horizontal word lines (WLs), and shared plate line (PL). Fig. 2(a) shows the cross-section along the BL-PL direction, while Fig. 2(b) presents the cross-section perpendicular to the WL, highlighting the GAA access transistor and the effective gate width definition. Figure 2(c) provides the corresponding top-view layout and pitch definitions. In the top view, the BL-PL cavities are symmetrically defined and determine the WL position at the center. The unit bit-cell area for a single layer is defined as $A_{\text{cell}} = P_{\text{BL}} \times P_{\text{BL-PL}}$, where P_{BL} is the bit-line pitch and $P_{\text{BL-PL}}$ is the spacing between the bit line and plate line. The

BL pitch is primarily constrained by vertical integration and coupling considerations, including high-aspect-ratio etching and inter-bit-line spacing, whereas the BL-PL pitch is determined by transistor and capacitor geometry requirements. In monolithic 3D-DRAM, density scaling is achieved through vertical stacking rather than lateral shrinkage. The effective bit-cell area is therefore expressed as $A_{\text{eff}} = A_{\text{cell}}/N_{\text{stack}}$, where N_{stack} denotes the number of vertically stacked cell layers. For the geometry considered here, a unit cell area (A_{cell}) is approximately $6.5 \times 10^4 \text{ nm}^2$, which corresponds to an effective area (A_{eff}) of $\sim 600 \text{ nm}^2$ for $N \approx 110$. In this context, the effective bit-cell area of 600 nm^2 should be interpreted as a forward-looking density reference rather than a direct indication of near-term manufacturability. The objective of this work is to evaluate architectural feasibility and scaling trends under realistic process and integration constraints.

The process-integration flow resulting in the monolithic 3D-DRAM architecture of Fig. 2 starts with alternating oxide/nitride multilayer deposition, followed by grid-patterning to define active and isolation regions. Vertical holes are subsequently etched, and the sacrificial nitride layers are selectively removed through these openings to create the transistor regions. An adhesion layer, gate metal, spacer, gate dielectric, and IGZO channel are then sequentially formed using a replacement-gate scheme. Finally, the vertical bit-line (VBL) and capacitor/plate-line (Cap/PL) structures are formed to provide the source/drain contacts and complete the memory cell.

B. DEVICE SIMULATION IMPLEMENTATION

In this work, the oxide-semiconductor channel is assumed to be amorphous indium–gallium–zinc-oxide (a-IGZO), which represents a widely studied and technologically relevant class of deposited oxide semiconductors for thin-film transistor applications. The material parameters adopted in the device simulations are based on a calibrated TCAD model for single-channel a-IGZO planar transistors, as reported in a recent device process- and architecture-aware study [15]. This ensures a physically realistic representation of key electrical characteristics such as carrier transport, threshold voltage, subthreshold behavior, and low off-state leakage current. Building on this calibrated planar a-IGZO transistor model, the present study extends the parameter set to a three-dimensional gate-all-around (GAA) version to evaluate its applicability to monolithically stacked 3D-DRAM access transistors.

Fig. 3. illustrates the three-dimensional TCAD simulation structure of the OSC GAA access transistor, including the channel, extension regions, spacer configuration, and contact geometry. While direct experimental calibration of fully stacked 3D GAA IGZO devices is not yet demonstrated, the present approach aims to establish trend-level and architecture-consistent insights, rather than absolute performance prediction.

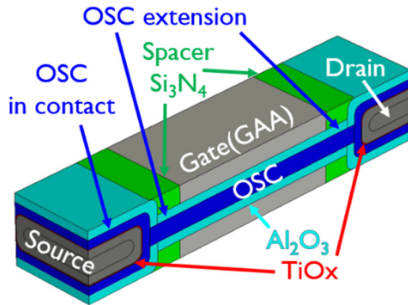


FIGURE 3. Three-dimensional TCAD simulation structure of the oxide-semiconductor gate-all-around (GAA) access transistor used in this work. The a-IGZO channel, spacer-defined extension regions, source/drain contacts, and Al_2O_3 gate dielectric are explicitly modeled in Sentaurus device. The device geometry is consistent with the process emulation flow shown in Fig. 2.

All device simulations are performed using the Synopsys Sentaurus Device solver within a drift-diffusion framework [16]. Electron transport in the a-IGZO channel is modeled using a constant mobility model based on a calibrated planar transistor setup [17], while non-local tunneling models are applied to the source and drain contacts to account for carrier injection. In particular, the TiOx interlayer is included as part of the $\text{TiN}/\text{TiOx}/\text{IGZO}$ source/drain contact stack [18]. Carrier injection at through the TiOx layer is modeled using nonlocal Schottky barrier tunneling. The gate stack consists of a 5-nm-thick Al_2O_3 dielectric (equivalent oxide thickness of 2.44 nm) and a metal gate with a work function of 4.7 eV. The channel baseline doping concentration is set to 10^{18} cm^{-3} , with a locally enhanced doping profile of $5 \times 10^{19} \text{ cm}^{-3}$ introduced at the TiOx -IGZO interface using a Gaussian distribution oriented normal to the interface, consistent with the calibrated reference model. All simulations are carried out at room temperature (300 K). Several non-ideal effects, such as gate leakage current and interface trap states (Dit), are intentionally not included in the present simulations. These effects are known to influence long-term reliability, leakage-current variability, and stability in oxide-semiconductor devices [19]; however, their omission is consistent with the scope of this study, which focuses on early-stage architectural feasibility, geometric scaling behavior, and parasitic-driven performance trade-offs rather than lifetime prediction, retention variability, or degradation analysis.

Before presenting the simulation results, it is useful to position the proposed architecture within the broader DRAM technology landscape. Table 1 summarizes the key architectural characteristics of representative DRAM access-transistor approaches. While conventional Si-based architectures are primarily constrained by leakage-related scaling challenges, the proposed OSC-based monolithic 3D-DRAM relaxes these limitations through the use of a low-leakage oxide-semiconductor channel. Consequently, the interplay between leakage and parasitic effects must be re-examined, motivating the device-, process-, and architecture-level analyses presented in the following sections.

TABLE 1. Architectural comparison of representative DRAM access-transistor approaches, including BCAT-based 2D DRAM [1], [2], Si-based Vertical Channel Transistor (VCT) [20], Si-based monolithic 3D DRAM [3], [6], [7], [22] and OSC-based DRAM concepts [4], [5], [10], [11], [12], [13], [21].

Metric	2D DRAM	VCT	3D DRAM	3D DRAM
Channel Material	Si	Si	Si	IGZO
Cell Architecture	BCAT	Vertical	Stacked	Stacked
Monolithic Integration Compatibility	No	No	High	High
GIDL Constraint	High	High	High	Low
Dominant Scaling Limitation	Area, Leakage	Integration, Leakage	Leakage	Parasitic Coupling

III. DEVICE SIMULATION RESULTS

This section presents the device-level simulation results of the oxide-semiconductor access transistor, focusing on the on-state current (I_{ON}), off-state current (I_{OFF}), and threshold voltage (V_{T}), which are the primary electrical figures of merit for DRAM operation. In the present study, all simulated structures satisfy the target median-cell I_{OFF} specification with sufficient margin, and therefore the analysis focuses on the variation of I_{ON} and V_{T} . The results are obtained using the TCAD simulation framework described in Section II-B.

A. DEFINITION OF BIAS CONDITIONS AND REFERENCE DEVICE CHARACTERISTICS

Fig. 4. shows the transfer characteristics ($I_{\text{D}}\text{-}V_{\text{G}}$) of a representative OSC GAA access transistor at $V_{\text{DS}} = 1 \text{ V}$. This biasing scheme ensures consistency with DRAM-oriented access transistor targets and enables direct verification that the simulated device satisfies the required current window for sensing [22]. The target criterion of $I_{\text{ON}} = 4 \mu\text{A}/\text{cell}$ is adopted from array-level sensing requirements rather than a specific technology-node target. This value corresponds to the minimum drive current required to establish a sensing margin of approximately 0.1 V within a target sensing time below 10 ns for the considered bit-line capacitance.

B. IMPACT OF GEOMETRICAL PARAMETERS ON DEVICE CHARACTERISTICS

The dependence of I_{ON} and V_{T} on key geometrical parameters is summarized in Figs. 5. In particular, gate length (L_{G}), extension length (L_{EXT}), effective gate width ($W_{\text{G,eff}}$), and channel thickness (T_{CH}) are varied alternately while all other parameters are kept constant. These parameters represent the primary geometrical knobs that govern current drive, electrostatic control, and layout scaling in the proposed GAA access transistor. Reducing L_{G} from 100 nm to 50 nm (see Fig. 5(a), (b)) results in a moderate increase in I_{ON} while maintaining rather stable V_{T} , indicating that electrostatic integrity is preserved and that short-channel effects remain well controlled within this range. The limited variation in V_{T} suggests that the GAA structure provides sufficient gate control even at reduced channel lengths, preventing significant threshold voltage roll-off. Decreasing L_{EXT} leads to a monotonic increase in I_{ON} due to reduced series resistance in the access path, while V_{T} remains largely

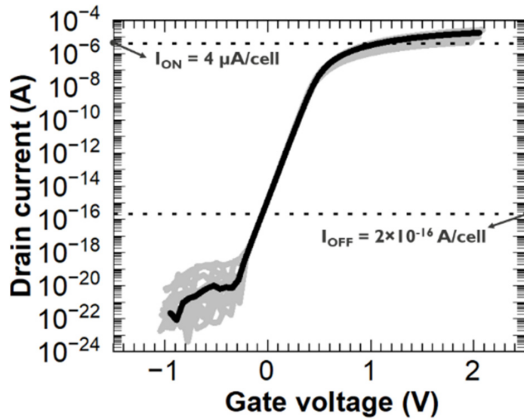


FIGURE 4. Transfer characteristics of the representative a-IGZO GAA access transistor used in this study (black). The on-current target is evaluated at $V_G = V_{G,IOFF} + 1.8V$, where $V_{G,IOFF}$ is defined as the gate voltage at which $I_{OFF} = 2 \times 10^{-16} A/cell$. The dashed horizontal lines indicate the DRAM-relevant on-current target ($I_{ON} = 4 \mu A/cell$) and the off-state leakage criterion. To enable consistent comparison, all transfer characteristics are aligned with respect to $V_{G,IOFF}$ by applying a horizontal shift, and the on-current is evaluated at a fixed overdrive relative to this reference point.

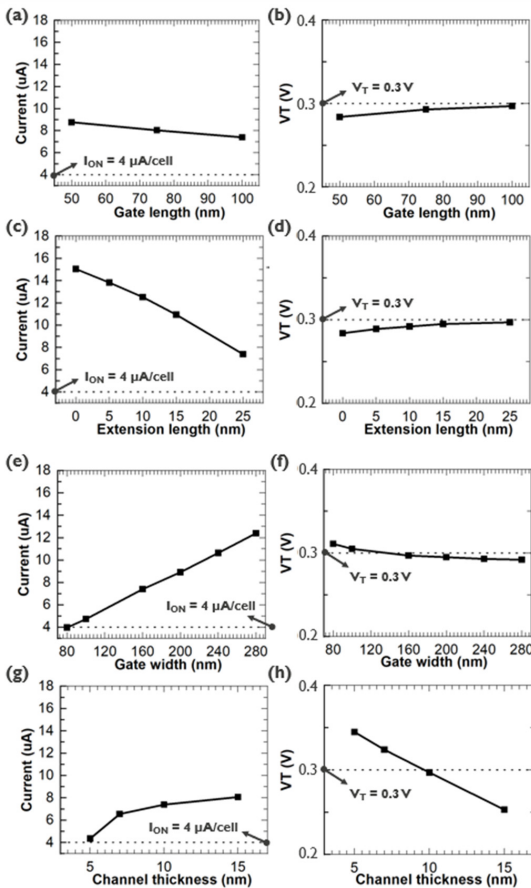


FIGURE 5. Dependence of on-current (I_{ON}) and threshold voltage (V_T) on key geometrical parameters of the a-IGZO GAA access transistor: (a)-(b) gate length (L_G), (c)-(d) extension length (L_{EXT}), (e)-(f) effective gate width ($W_{G,eff}$), (g)-(h) channel thickness (T_{CH}). Dashed lines indicate the DRAM-relevant targets of $I_{ON} = 4 \mu A/cell$ and $V_T = 0.3 V$.

unchanged (see Fig. 5(c), (d)). This behavior reflects the absence of leakage-driven constraints in OSC devices, in

contrast to Si-channel transistors, where extension scaling is limited by GIDL under negative word-line bias [23]. From a transport perspective, shortening L_{EXT} reduces the resistive access region between the channel and the contact, thereby improving carrier injection efficiency without significantly altering the channel electrostatics [24].

Increasing $W_{G,eff}$ enhances I_{ON} by enlarging the effective conduction perimeter, with minimal impact on V_T (see Fig. 5(e), (f)). This trend is consistent with the GAA geometry, where current scales with the total gated channel perimeter. However, this benefit is counteracted by an increase in lateral cell footprint and associated parasitic capacitances, limiting its applicability for high-density DRAM integration.

Increasing T_{CH} improves carrier transport by increasing the conducting volume, leading to higher I_{ON} , while V_T decreases due to reduced electrostatic control in thicker channels (see Fig. 5(g), (h)) [25]. As the channel becomes thicker, the gate control over the channel potential weakens, resulting in a lower threshold voltage. When T_{CH} is reduced below approximately 10 nm, limited carrier availability results in reduced current, indicating a transition to volume-limited conduction in ultra-thin channels. Because mobility is kept constant in the simulations, the reduction in I_{ON} is attributed to the reduced conducting volume and carrier density as T_{CH} decreases.

C. DEVICE-LEVEL SCALING LIMITS AND BASELINE SELECTION

These results indicate that scaling down to $L_G = 50$ nm is feasible at the device level. Further reduction is limited not by electrostatics, but by layout and process constraints, in particular the minimum single-patterning lithography (e.g., ArF immersion) step word line width of about 50 nm shown in Fig. 2(c), required to ensure structural integrity and reliable patterning. From a transistor perspective, L_{EXT} can be aggressively reduced without introducing leakage penalties. However, at the cell level, reduced L_{EXT} increases WL-BL coupling, degrading the sensing margin. As demonstrated in the subsequent parasitic and memory-level analysis, a minimum L_{EXT} of approximately 15 nm is required to balance drive-current improvement and parasitic-induced degradation. Considering the trade-offs among current drive, electrostatic control, layout footprint, and parasitic interactions, the baseline device geometry is defined as $L_G = 50$ nm, $L_{EXT} = 15$ nm, $W_{G,eff} = 160$ nm, and $T_{CH} = 10$ nm. This configuration satisfies the I_{ON} target while maintaining V_T stability and compatibility with monolithic 3D integration constraints.

IV. PROCESS EMULATION AND PARASITIC EXTRACTION

This section presents the process emulation and parasitic extraction results for the proposed monolithic 3D-DRAM cell. All geometrical assumptions regarding vertical stacking, bit-line pitch, and unit cell area follow the definitions established in Section II. The objective here is to quantify how process-defined geometry translates into parasitic capacitances and to assess their implications for DRAM sensing and timing at the cell level. The parasitic extraction is

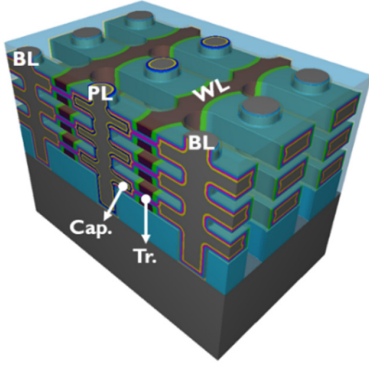


FIGURE 6. Three-dimensional process-emulated geometry of the proposed monolithic OSC-based 3D-DRAM cell obtained using SEMulator3D.

limited to device-level and local cell parasitics, while global interconnect routing is not included in the PEX.

A. PROCESS EMULATION FRAMEWORK AND GEOMETRY DEFINITION

Three-dimensional process emulation is performed using SEMulator3D to construct the full monolithic 3D-DRAM cell geometry corresponding to the baseline access-transistor design identified in Section III. Fig. 6 shows the process-emulated 3D geometry of the stacked cell. All memory layers are processed simultaneously in a monolithic manner, resulting in a vertically continuous BL string shared across stacked cells, while individual horizontal WLs remain electrically isolated in the vertical direction. This vertical connectivity is explicitly accounted for in the subsequent parasitic extraction.

B. EXTRACTED PARASITIC CAPACITANCE COMPONENTS

Based on the emulated three-dimensional geometry, parasitic capacitances are extracted using SEMulator3D-based PEX. The resulting capacitance network, shown in Fig. 7, includes the storage-node capacitance C_S , the per-layer contribution to the bit-line capacitance, and the coupling capacitances among the word line, bit line, storage node (SN), and plate line. The total effective bit-line capacitance $C_{BL,tot}$ is obtained by aggregating the vertically connected BL segments across the stacked layers, consistent with the vertical BL routing scheme of the proposed architecture. By relying on geometry-based extraction rather than idealized lumped assumptions, this approach establishes a physically grounded capacitance network for the subsequent sensing-margin evaluation and performance analysis presented in Section V.

C. PARASITIC CAPACITANCE DEPENDENCE ON BL PITCH AND EXTENSION LENGTH

The unit bit-cell area scales with the bit-line pitch (P_{BL}). Before evaluating the parasitic capacitances, realistic fabrication limits must be determined. The minimum BL diameter is defined by the cavity used for vertical BL integration (Fig. 2(c)), i.e., the etched circular opening through which the gate, dielectric and channel are introduced conformally. The cavity diameter is therefore constrained by the surrounding material stack, including twice the adhesion layer (5 nm),

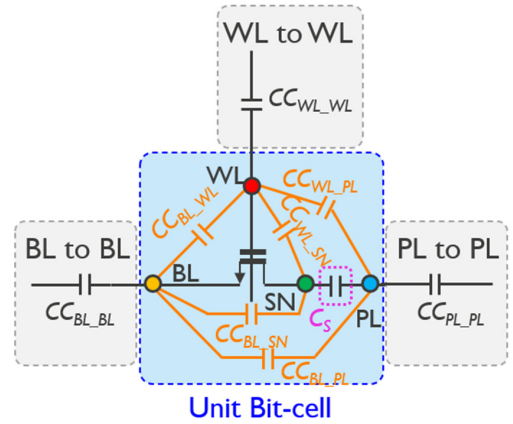


FIGURE 7. PEX network of the monolithic 3D-DRAM cell.

TABLE 2. Extracted per-layer BL-WL coupling capacitance, per-layer bit-line capacitance, and sensing-margin evaluation for different extension lengths L_{EXT} , where $C_{BL,tot} = N_{stack} \times C_{BL}(\text{per layer})$.

L_{EXT}	BL-WL Coupling (per layer)	CBL (per layer)	$C_{BL,tot}/4$	C_S ($k=34$)
5 nm	4.31×10^{-17} F	6.16×10^{-17} F	1.67×10^{-15} F	1.46×10^{-15} F
10 nm	3.48×10^{-17} F	5.30×10^{-17} F	1.43×10^{-15} F	1.39×10^{-15} F
15 nm	3.01×10^{-17} F	4.83×10^{-17} F	1.31×10^{-15} F	1.34×10^{-15} F

gate metal (20 nm), gate dielectric (5 nm), and IGZO channel (5 nm), resulting in a minimum diameter of ~ 70 nm. Considering high-aspect-ratio etching effects such as top-bottom critical dimension (CD) variation and bottom narrowing, a practical top cavity size of 90 nm is adopted. With an additional lateral margin of 7.5 nm per side to ensure reliable vertical landing, the effective minimum BL diameter becomes approximately 75 nm. This corresponds to a minimum BL pitch of about 150 nm, assuming a spacing comparable to the BL diameter. A nominal BL pitch of 210 nm is used to ensure process margin. The pitch is swept from 150 nm to 230 nm, and capacitances are extracted from a 3-stack structure and normalized per layer.

As shown in Fig. 8(a), BL-BL coupling varies significantly with pitch, while the total bit-line capacitance remains within $\pm 1\%$ of its nominal value, indicating that pitch scaling mainly affects local coupling without significantly changing the overall sensing-relevant capacitance. In contrast, extension-length scaling imposes a stronger constraint at the DRAM level. In Si-channel devices, wider extension regions suppress GIDL driven by band-to-band tunneling under negative gate bias, limiting scaling and increasing series resistance [26]. In oxide semiconductors, such leakage is suppressed, allowing more aggressive scaling of L_{EXT} from a transistor perspective. However, DRAM operation requires sensing condition of $C_S \geq C_{BL,tot}/4$, where $C_{BL,tot}$ is the total effective bit-line capacitance, ensuring a sensing margin larger than 0.1 V. As shown in Fig. 8(b), reducing L_{EXT} sharply increases BL-WL coupling due to reduced separation from the vertical BL, making C_{BL-WL} the dominant contributor to $C_{BL,tot}$.

Table 2 summarizes the extracted capacitances and sensing margin. Because the total horizontal cell length is fixed, reducing L_{EXT} increases capacitor length and slightly

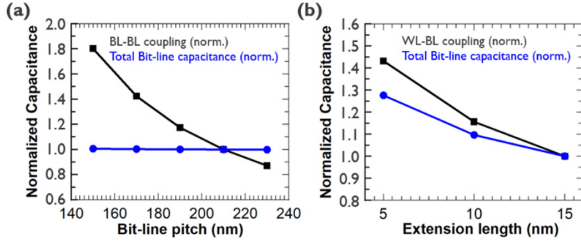


FIGURE 8. Normalized per-layer parasitic capacitances versus bit-line pitch (a) and extension length (b). BL-BL coupling, BL-WL coupling, and total bit-line capacitance are included. Values are normalized to 210 nm for pitch and 15 nm for extension length.

increases C_S . However, excessive reduction of L_{EXT} violates the sensing condition, as the increase in $C_{BL,tot}$ outweighs the gain in C_S . Under the assumed spacer dielectric, the minimum acceptable extension length is ~ 15 nm. These results show that, although OSC devices remove leakage-driven limits, the practical scaling bound is set by parasitic coupling rather than transistor leakage.

V. ANALYTICAL EVALUATION OF DRAM PERFORMANCE

The device-optimized parameters and PEX network are used to evaluate DRAM-level performance through a first-order analytical framework. The storage-node capacitance C_S , total bit-line capacitance $C_{BL,tot}$, coupling components, and simulated on/off currents are combined to estimate retention time, delay, and energy. All capacitances except $C_{BL,tot}$ are defined per cell, while $C_{BL,tot}$ represents the total capacitance of the vertical bit-line with multiple bit cells including the selected cell. Peripheral circuit elements are not included, as the analysis focuses on intrinsic cell-level behavior. All parasitic terms are directly taken from the PEX network in Fig. 7 without additional fitting. The supply voltage is set to 1.0 V, where the voltage denotes the array-level operation voltage used for cell-level analysis. The bit line is precharged to $V_{supply}/2$, and a 50-mV detection limit is used. The on-current is obtained from TCAD simulation under defined as a gate overdrive of 1.8 V above $V_{G,IOFF}$, where $V_{G,IOFF}$ is defined as the gate voltage at which $I_{OFF} = 2 \times 10^{-16}$ A. Two off-current levels are considered: a spec-aligned value of 2×10^{-16} A and an intrinsic OSC leakage floor of $\sim 10^{-20}$ A.

A. RETENTION TIME

The retention time is expressed as:

$$t_{retention} = \frac{C_S}{I_{OFF}} \left\{ V_{supply} - V_{BL,precharge} - \left(1 + \frac{C_{BL,tot}}{C_S} \right) \Delta V_{detection\ limit} \right\}$$

The resulting retention times are summarized in Table 3.

With the sensing-aligned leakage current, the retention time is 1.70 s, exceeding the 1 s DRAM specification [27]. In practical arrays, the effective refresh interval is often limited by worst-case cells and retention-time distributions rather than median-cell behavior [28]. Therefore, the reported retention value should be interpreted as an intrinsic cell-level estimate rather than an array-level retention limit. When

TABLE 3. Retention time calculated using two off-current conditions: spec-aligned and intrinsic OSC leakage.

I_{OFF}	Retention time	Interpretation
2×10^{-16} A	1.70 s	Practical lower bound
1×10^{-20} A	3.41×10^4 s	Intrinsic upper bound

the intrinsic leakage level is used, the retention increases by several orders of magnitude. This behavior is consistent with the low-leakage characteristic of OSC channels and shifts the dominant design constraint from leakage to capacitive coupling.

B. WRITE AND READ DELAY

The write delay is expressed as:

$$t_{write} = \frac{(C_S + C_{para,write})V_{supply} \times 0.9}{I_{ON}}$$

where $C_{para,write} = CC_{WL_SN} + CC_{BL_SN}$, and 0.9 represents the fraction of the storage-node voltage required for write completion.

The read delay is given by:

$$t_{read} = \frac{(C_S + C_{para,write})(C_{BL,tot} + C_{para,read}) V_{supply}}{C_S + C_{para,write} + C_{BL,tot} + C_{para,read} \ 2I_{ON}}$$

where $C_{para,read} = CC_{BL_WL} + CC_{BL_PL}$.

Using the spec-aligned on-current of 4 μ A/cell, the write and read delays are 307 ps and 136 ps, respectively. With the simulated on-current of 14.5 μ A/cell, they reduce to 84.6 ps and 37.4 ps. In all cases, the delays remain within the sub-nanosecond range, indicating sufficient drive capability. These values represent intrinsic cell-level estimates derived from the analytical model and do not include peripheral-circuit, sensing-amplifier, or global interconnect delays.

C. WRITE AND READ ENERGY

The write and read energies are given by:

$$E_{write} = (C_S + C_{para,write}) \frac{V_{supply}^2}{2}$$

$$E_{read} = \frac{(C_S + C_{para,write})(C_{BL,tot} + C_{para,read}) V_{supply}^2}{C_S + C_{para,write} + C_{BL,tot} + C_{para,read} \ 8}$$

Using the extracted capacitances, the write and read energies are 0.682 fJ and 0.135 fJ, respectively. These values represent intrinsic cell-level energy and exclude peripheral contributions.

D. CONSOLIDATED PERFORMANCE

Table 4 summarizes the calculated delay and energy metrics. The delays range from 37 ps to 307 ps depending on the drive current, while the energies remain in the sub-femtojoule regime. Even under conservative on-current conditions, the access transistor satisfies intrinsic timing requirements [27]. Combined with the retention results, the optimized OSC-based access transistor meets DRAM-relevant operating conditions at the intrinsic cell level. However, it should be noted that array-level performance is typically constrained

TABLE 4. Calculated DRAM delay and energy metrics.

Metric	Spec I_{ON} (4 μ A/cell)	Simulated I_{ON} (14.5 μ A/cell)	Intrinsic Reference Range
Write time	307 ps	84.6 ps	0.1-1 ns
Read time	136 ps	37.4 ps	0.1-1 ns
Write energy	0.682 fJ	0.682 fJ	0.1-1 fJ
Read energy	0.135 fJ	0.135 fJ	0.1-1 fJ

by worst-case (tail-bit) behavior, which is not captured in the present analysis.

VI. CONCLUSION

This work presents a unified evaluation framework for OSC-based monolithic 3D-DRAM, linking device simulation, process emulation, parasitic extraction, and analytical modeling. The results show that WL-BL coupling dominates the total bit-line capacitance, making extension length a key design parameter. Although OSC channels remove GIDL-driven scaling limits, a minimum L_{EXT} of ~ 15 nm is required to satisfy the sensing condition $C_S \geq C_{BL,tot}/4$. The optimized structure achieves sub-nanosecond delay, sub-femtojoule energy, and intrinsic-cell retention estimate of 1.70 s. These results indicate that performance is governed primarily by parasitic coupling rather than channel properties, highlighting coupling management as the main scaling challenge in monolithic OSC based 3D-DRAM. The retention analysis presented in this work is based on deterministic device simulations and should therefore be interpreted as an intrinsic median-cell evaluation. Retention variability and worst-case cell behavior remain important topics for future investigation.

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