Journal of Applied Physics

TUTORIAL | NOVEMBER 01 2024

Selecting alternative metals for advanced interconnects

Jean-Philippe Soulié ; Kiroubanand Sankaran ; Benoit Van Troeye ; Alicja Leśniewska ; Olalla Varela Pedreira ; Herman Oprins ; Gilles Delie ; Claudia Fleischmann ; Lizzie Boakes ; Cédric Rolin ; Lars-Åke Ragnarsson ; Kristof Croes ; Seongho Park ; Johan Swerts ; Geoffrey Pourtois ; Zsolt Tőkei ; Christoph Adelmann

J. Appl. Phys. 136, 171101 (2024)
https://doi.org/10.1063/5.0224027

View Online
Export Citation

Articles You May Be Interested In

Roughness-generation mechanism of Ru etching using Cl_2/O_2-based plasma for advanced interconnect
J. Vac. Sci. Technol. B (July 2024)

A survey on the latest FET technology for samsung industry
AIP Conf. Proc. (December 2023)

04 November 2024 08:02:31

Challenge us.
What are your needs for periodic signal detection?

Find out more

Journal of Applied Physics TUTORIAL pubs.aip.org/aip/jap

Selecting alternative metals for advanced interconnects

Cite as: J. Appl. Phys. 136, 171101 (2024); doi: 10.1063/5.0224027
Submitted: 18 June 2024 · Accepted: 3 October 2024 ·
Published Online: 1 November 2024

View Online

Export Citation

CrossMark

Jean-Philippe Soulié,[1] Kiroubanand Sankaran,[1] Benoit Van Troeye,[1] Alicja Leśniewska,[1] Olalla Varela Pedreira,[1] Herman Oprins,[1] Gilles Delie,[1] Claudia Fleischmann,[1,2] Lizzie Boakes,[1] Cédric Rolin,[1] Lars-Åke Ragnarsson,[1] Kristof Croes,[1] Seongho Park,[1] Johan Swerts,[1] Geoffrey Pourtois,[1] Zsolt Tőkei,[1] and Christoph Adelmann[1,a)]

AFFILIATIONS

[1]imec, 3001 Leuven, Belgium
[2]Department of Physics and Astronomy, KU Leuven, 3001 Leuven, Belgium

[a)]**Author to whom correspondence should be addressed:** Christoph.Adelmann@imec.be

ABSTRACT

Interconnect resistance and reliability have emerged as critical factors limiting the performance of advanced CMOS circuits. With the slowdown of transistor scaling, interconnect scaling has become the primary driver of continued circuit miniaturization. The associated scaling challenges for interconnects are expected to further intensify in future CMOS technology nodes. As interconnect dimensions approach the 10 nm scale, the limitations of conventional Cu dual-damascene metallization are becoming increasingly difficult to overcome, spurring over a decade of focused research into alternative metallization schemes. The selection of alternative metals is a highly complex process, requiring consideration of multiple criteria, including resistivity at reduced dimensions, reliability, thermal performance, process technology readiness, and sustainability. This Tutorial introduces the fundamental criteria for benchmarking and selecting alternative metals and reviews the current state of the art in this field. It covers materials nearing adoption in high-volume manufacturing, materials currently under active research, and potential future directions for fundamental study. While early alternatives to Cu metallization have recently been introduced in commercial CMOS devices, the search for the optimal interconnect metal remains ongoing.

© 2024 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution-NonCommercial 4.0 International (CC BY-NC) license (https://creativecommons.org/licenses/by-nc/4.0/). https://doi.org/10.1063/5.0224027

04 November 2024 08:02:31

I. INTRODUCTION

Microelectronic circuits are central elements in myriads of electronic appliances in almost every aspect of today's life. Logic circuits, memory cells, and sensors are used to process, store, and detect information in diverse applications, ranging from computers and smartphones to automobiles and medical equipment. The success of microelectronics relies on the relentless miniaturization of the underlying building blocks, which, in the case of logic circuits based on transistors, has been epitomized by the famed Moore's law.[1] Similar scaling trends also apply to other devices, for example, to memory cells. The reduction of device dimensions in combination with the enormous increase of device density[2] has led to large performance benefits, but also to lower energy consumption per operation and, at least for older generations, much reduced cost per function. For instance, the cost to fabricate one transistor has been reduced by a factor of 10^9 since 1970.[3]

In the public perception, Moore's law has been historically connected to scaling transistors or memory cells. However, scaling interconnects is of equal importance to uphold Moore's law. Interconnect lines and vias provide signal, power, and clock to the active components of the circuits, such as complementary metal–oxide–semiconductor (CMOS) transistors or memory elements, and, thus, are central in microelectronic circuits and systems with advanced functionality [Fig. 1(a)]. As an example, the area of a static random-access memory (SRAM) cell, used as cache memory in logic processors, is determined in one direction by the gate pitch (also termed "contacted poly pitch") of the transistors (the transistor size), but by the pitch of the metal lines (the interconnect pitch) in the orthogonal direction [Fig. 1(b)]. Hence, to reduce the cell area, both transistor and interconnect dimensions should be scaled.

In earlier technology nodes, transistor performance traditionally improved as dimensions were scaled down, yielding the

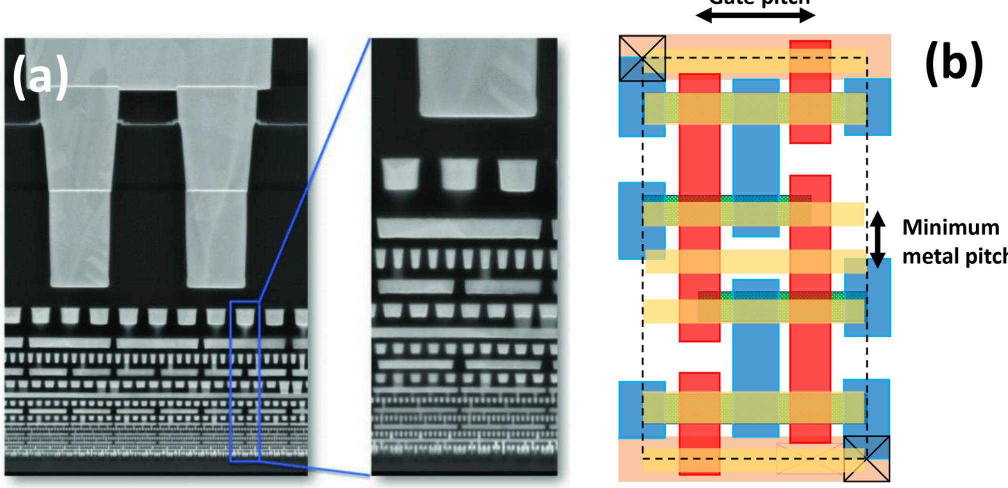


FIG. 1. (a) Cross-sectional transmission-electron micrograph of the 16-level interconnect stack in Intel 4 technology.[4] Reproduced with permission from Sell *et al.*, in *2022 IEEE Symposium on VLSI Technology and Circuits*, Digest of Technical Papers, pp. 282–283 (2022). Copyright 2022 IEEE. (b) Layout of a static random-access memory (SRAM) cell in imec 3 nm technology, illustrating that the cell size is equally determined by the transistor and metal pitch. For further details, see Refs. 5 and 6.

performance benefits described above. However, this trend does not extend to interconnects. Reducing the cross-sectional area of a wire inevitably increases its resistance per unit length, resulting in greater energy dissipation and higher resistive–capacitive delay (*RC*-delay). At current interconnect line widths, ranging from 12 to 15 nm (see Sec. I A), interconnect performance has become a primary constraint on the overall performance of advanced microelectronic circuits.[7–18]

For transistors, scaling has been accompanied by significant architectural innovations.[19–21] In contrast, architectural changes in interconnects are limited, and thus, performance enhancements mainly need to occur through materials and process innovation. One approach to reducing interconnect capacitance involves the use of dielectrics with lower permittivity (low-κ dielectrics)[10] or the introduction of air gaps.[22,23] However, these advancements have been hampered by the reduced mechanical stability of the resulting interconnect structures, leading to reliability issues during packaging.

Consequently, optimizing the metallization scheme has emerged as a critical focus of interconnect research in recent years.[12,18,24–33] The current Cu dual-damascene metallization scheme (Fig. 2), which replaced Al-based metallization post-1999,[10,34–36] is facing growing issues for several reasons. First, Cu requires diffusion barriers and adhesion liners to ensure the interconnect reliability. Without diffusion barriers (typically TaN-based), Cu migration into surrounding dielectrics leads to dielectric breakdown and shorting between adjacent lines (see Sec. III). Moreover, Cu electromigration becomes an increasing issue at scaled dimensions (see Sec. III). This is mitigated by incorporating adhesion liner layers (typically Co/Ru) between the TaN barrier and Cu as well as by capping layers.[10,36–38] However, the combined thickness of barrier and liner layers cannot be reduced below 2 to 3 nm without compromising functionality. Hence, in narrow lines, the high-resistivity barrier and liner layers occupy an increasingly significant fraction of the total metallization volume, reducing the available space for Cu, while contributing minimally to the wire's conductance.

Furthermore, as elucidated in Sec. II, the resistivity of Cu increases sharply at reduced dimensions due to the more pronounced effects of grain boundary and surface scattering. Both the increased resistivity and the decreasing volume fraction of Cu contribute to a rapid increase in the line and via resistances per unit length as interconnect dimensions are scaled down. This results in a significant deterioration of interconnect performance, even for relatively short lines. Additionally, the dual-damascene metallization integration process necessitates increasingly disruptive modifications to ensure void- and defect-free interconnects with robust mechanical stability.

These issues can be mitigated by selecting alternative metals that ideally do not require barrier and liner layers while exhibiting lower sensitivity of resistivity to nanoscale dimensions. Although this approach cannot reverse the increase in line resistance per unit length, we will demonstrate below that alternative metals and metallization schemes can outperform Cu at sufficiently small line widths. In this Tutorial, we will discuss the various aspects relevant for the selection of potential alternative metals for advanced interconnects. The selection process is multifaceted and must address the challenge from different angles. To this end, we have developed a multistage framework to identify, downselect, and benchmark alternative metals for interconnect applications (Fig. 3).

This Tutorial is organized as follows. We first examine the sensitivity of resistivity to nanoscale dimensions and introduce a material screening process. Next, we discuss reliability aspects, focusing on time-dependent dielectric breakdown as well as on electromigration. We then apply this selection process to elemental, binary, and ternary metals, highlighting current and future research

04 November 2024 08:02:31

© Author(s) 2024

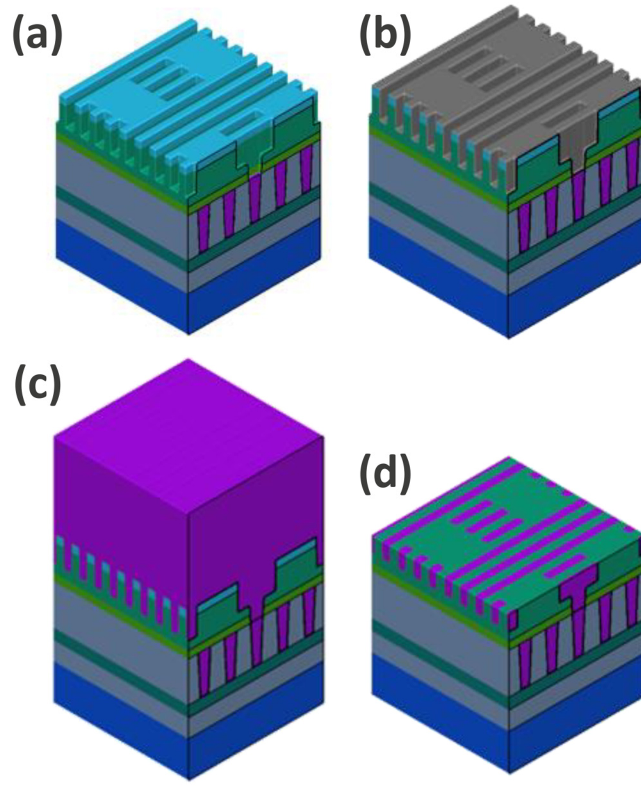


FIG. 2. Schematic of the Cu dual-damascene interconnect process integration flow: (a) via and trench patterning in low-κ dielectric (green) using a hardmask (turquoise); (b) conformal barrier and liner deposition (gray); (c) Cu (over-)filling of vias and lines (purple); and (d) chemical–mechanical polishing for line isolation and planarization, revealing Cu lines (purple) embedded in low-κ dielectric (green).

directions. Given the strong connection between metal selection and future integration schemes, we will also briefly discuss integration and process considerations for alternative metals in upcoming technology nodes. Finally, with sustainability becoming increasingly crucial to minimizing the ecological footprint of the microelectronics industry, we introduce a life cycle assessment framework for interconnect metals and apply it to various promising candidates identified through our selection criteria.

A. Technology targets for future interconnects

Historically, interconnect scaling has been guided by industry roadmaps, such as the International Technology Roadmap for Semiconductors (ITRS),[39] presently called the International Roadmap for Devices and Systems (IRDS).[40] However, today, no industry-wide roadmap exists, and also, technology node nomenclature has become ambiguous. At present, commercial microelectronic chips feature minimum interconnect pitches around 25 nm, with further scaling anticipated to reach sub-20 nm metal pitches in the near future (see Table I). This implies that line widths, which are equivalent to half the metal pitch, will soon reach sub-10 nm dimensions. This is especially significant as the contacted poly pitch (transistor gate pitch) has become close to physical limits and is not expected to be scaled much further. Therefore, future area gains for CMOS circuits must primarily stem from transistor architecture innovation (e.g., CFET) as well as continued interconnect pitch scaling.

As previously noted, such small line widths may not be compatible with the Cu dual-damascene metallization scheme employed today in scaled interconnects (Fig. 2). While ongoing efforts to optimize Cu dual-damascene processing may yield incremental improvements, achieving the minimum interconnect dimensions in Table I will require disruptive approaches, potentially involving novel materials, processes, and integration schemes. As indicated in the table, the target critical dimensions for interconnect lines and vias, equivalent to half the metal pitch, fall within the range between 5 and 10 nm, providing guidelines for both metal selection and process development.

II. SIZE EFFECTS ON THE METAL RESISTIVITY AT NANOSCALE DIMENSIONS

For decades, it has been well-established that the resistivity of metallic nanostructures, such as thin films and nanowires, is typically much higher than that of their bulk counterparts.[44–49] This presents a significant challenge for interconnect scaling, as the increase in line and via resistance occurs at a much faster rate than what would be predicted solely by the reduction in geometrical dimensions, particularly for critical dimensions below 10 nm.

The resistivity increase can be primarily attributed to the combined effects of scattering at rough surfaces or interfaces[44,45] and scattering at grain boundaries.[47,48] To quantitatively describe this behavior, several transport models have been developed for thin films, accounting for top and bottom surface/interface scattering.[48,50–59] However, it should be noted that no comprehensive one-dimensional transport model currently exists to describe nanowires, which are bounded by four surrounding surfaces. Despite this, the qualitative behavior of nanowires is expected to be similar to that of thin films, and thus, “thin-film-derived” resistivity models have been applied to understand the scaling behavior of nanowires as well.[60–68]

In this section, we introduce the basic physics governing the resistivity of metal nanostructures. We will demonstrate that the mean free path of charge carriers in bulk metals is a critical parameter to characterize how resistivity depends on nanostructure dimensions. Following this, we discuss additional scattering mechanisms present in compound metals. Finally, we introduce *ab initio* screening methods to calculate the mean free path and identify promising metals that may exhibit lower resistivity than Cu at the nanoscale.[69–71]

A. Electron transport in metallic nanostructures

1. Semiclassical description of electron transport

The most widely used approach to understand the increase in resistivity at reduced dimensions is based on the Boltzmann transport equation. The Boltzmann transport equation describes the

04 November 2024 08:02:31

© Author(s) 2024

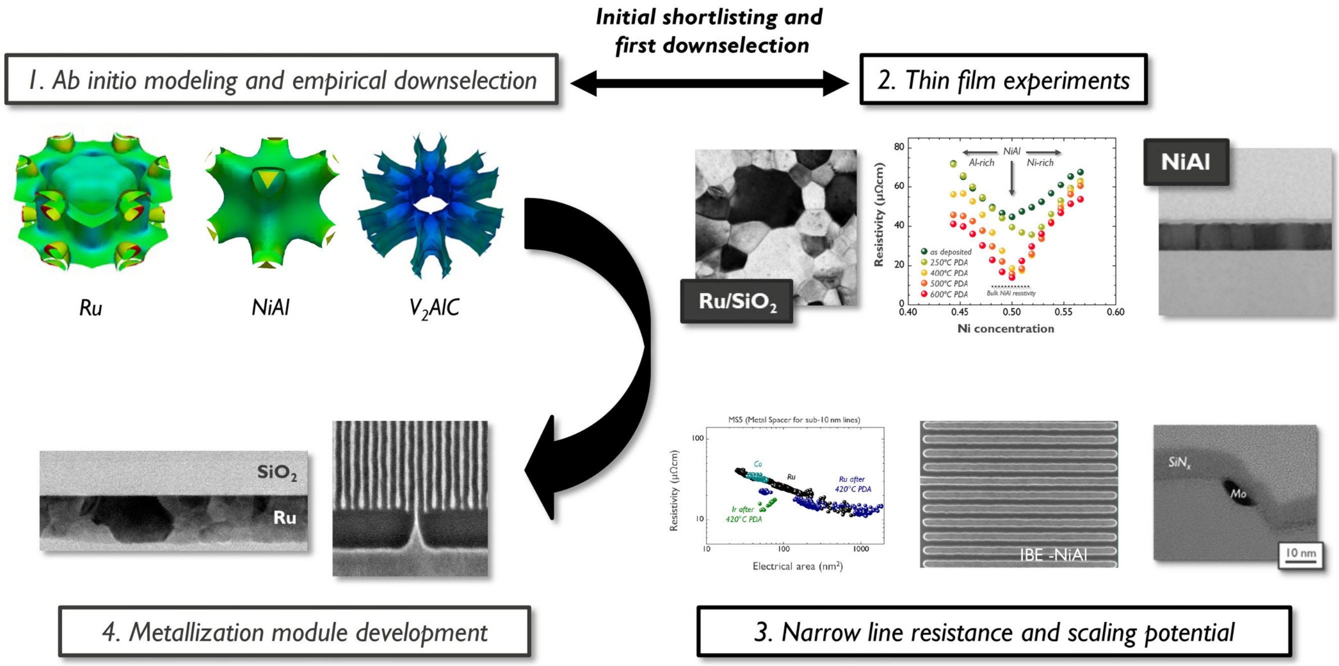


FIG. 3. imec workflow for identifying, downselecting, and benchmarking alternative interconnect metals: *Ab initio* simulations are employed to identify potential candidate metals, which are subsequently downselected using a combination of thin-film and nanowire experiments. The most promising materials are then selected for process module development and integration into scaled interconnects, followed by technology benchmarking.

04 November 2024 08:02:31

statistical distribution of charge carriers in non-equilibrium conditions, e.g., when an electric field is applied.

In the absence of temperature and composition gradients, as well as magnetic fields, the Boltzmann transport equation can be written as

$$-e\frac{\partial f^0_{n\mathbf{k}}}{\partial \epsilon_{n\mathbf{k}}}\mathbf{v}_{n\mathbf{k}}\cdot\mathbf{E} = -\frac{\partial g_{n\mathbf{k}}}{\partial t}\bigg|_{\text{scattering}} + \mathbf{v}_{n\mathbf{k}}\cdot\nabla_r g_{n\mathbf{k}}, \tag{1}$$

where e is the electron charge, $f^0_{n\mathbf{k}}$ the equilibrium Fermi–Dirac distribution for electrons of mode n, and $\mathbf{k}$ the wavevector of the electron with energy $\epsilon_{n\mathbf{k}}$ and velocity $\mathbf{v}_{n\mathbf{k}}$. $\mathbf{E}$ represents the external electric field, and $g_{n\mathbf{k}} = f_{n\mathbf{k}} - f^0_{n\mathbf{k}}$ denotes the deviation of the non-equilibrium electron distribution from the Fermi–Dirac equilibrium. $\partial g_{n\mathbf{k}}/\partial t|_{\text{scattering}}$ accounts for charge carrier scattering.

In the linearized (semiclassical) approximation, referred to as the relaxation time approximation, the scattering term can be expressed as $\partial g_{n\mathbf{k}}/\partial t|_{\text{scattering}} = -g_{n\mathbf{k}}/\tau_{n\mathbf{k}}$, where $\tau_{n\mathbf{k}}$ represents the relaxation time. For high-purity bulk metals near room temperature, electron–phonon scattering dominates, with the corresponding relaxation time $\tau^{\text{ep}}_{n\mathbf{k}}$. In polycrystalline films, grain boundaries introduce additional charge carrier scattering, characterized by the relaxation time $\tau^{\text{gb}}_{n\mathbf{k}}$. When grain sizes are sufficiently large (indicating low disorder), both relaxation times can be considered independent, and the total relaxation time follows Matthiessen's rule,

$$(\tau_{n\mathbf{k}})^{-1} = \left(\tau^{\text{gb}}_{n\mathbf{k}}\right)^{-1} + \left(\tau^{\text{ep}}_{n\mathbf{k}}\right)^{-1}. \tag{2}$$

For a bulk material with no spatial variation, the conductivity tensor $\underline{\underline{\sigma}}$ and resistivity tensor $\underline{\underline{\rho}}$ can be derived by noting that the

TABLE I. Roadmap for interconnect dimensions (minimum metal pitch) in logic circuits. Adapted from Ref. 41. For the current state of the art, see Refs. 42 and 43. HVM, high-volume manufacturing; GAA, gate all-around; and CFET, complementary field-effect transistor.

Year of HVM	2024/25	2027/28	2029	2031	2033	2035
Technology node	2 nm	14 A	10 A	7 A	5 A	3 A
Transistor technology	GAA	GAA	CFET	CFET	CFET	2D
Min. metal pitch (nm)	23	20	18	16	14	12
Gate pitch (nm)	45	42	42	39	39	36

© Author(s) 2024

current density is given by

$$\mathbf{j} = \frac{-e}{A}\sum_n \int\int g_{n\mathbf{k}} \mathbf{v}_{n\mathbf{k}} \mathrm{d}\mathbf{A}\, \mathrm{d}\mathbf{k} = \frac{-e^2}{N_\mathbf{k}\Omega}\sum_{n\mathbf{k}} \tau_{n\mathbf{k}} \frac{\partial f^0_{n\mathbf{k}}}{\partial \epsilon_{n\mathbf{k}}} \mathbf{v}_{n\mathbf{k}} \otimes \mathbf{v}_{n\mathbf{k}} \mathbf{E} = \underline{\underline{\sigma}}\mathbf{E} = \underline{\underline{\rho}}^{-1}\mathbf{E}, \tag{3}$$

where A represents the cross-sectional area through which electrons flow, $N_\mathbf{k}$ is the number of $\mathbf{k}$-points used to sample the Brillouin zone, and Ω denotes the volume of the unit cell.

Thus far, we have neglected the impact of the spatial gradient in Eq. (1), which becomes relevant when considering a finite-size material, such as a thin film with thickness h. Due to the linear nature of the Boltzmann transport equation in the relaxation time approximation, the general solution is a superposition of a particular solution that accounts for boundary conditions and the solution derived for an infinitely large material. The particular solution is determined by the scattering behavior of electrons at the material's boundaries, i.e., at the top and bottom surfaces or interfaces of a thin film. This effect is further amplified in nanowires, where electrons can also scatter at lateral boundaries. Surface scattering can be either specular, when the electron preserves its total momentum and only the out-of-plane momentum component changes sign, or diffusive, when the electron's momentum is completely randomized. In practice, this results in the renormalization of the relaxation time for a thin film of thickness h, as described by[72]

$$\frac{\tau_{n\mathbf{k}}(h,\hat{u})}{\tau^0_{n\mathbf{k}}} = 1 - (1-p)\frac{|\boldsymbol{\lambda}_{n\mathbf{k}}.\hat{u}|}{h}\frac{1-e^{-h/|\boldsymbol{\lambda}_{n\mathbf{k}}.\hat{u}|}}{1-pe^{-h/|\boldsymbol{\lambda}_{n\mathbf{k}}.\hat{u}|}}, \tag{4}$$

where $\hat{u}$ denotes the unit vector normal to the thin film surface. p is the reflection coefficient with $p = 1$ representing purely specular surfaces and $p = 0$ representing fully diffusive surfaces, and $\boldsymbol{\lambda}_{n\mathbf{k}} = \tau_{n\mathbf{k}}\mathbf{v}_{n\mathbf{k}}$ represents the mean free path of the charge carriers in the bulk metal.

From Eq. (4), it is evident that no resistivity increase occurs with decreasing film thickness h for purely specular surfaces, whereas diffusive surfaces result in a strong dependence on h. For a metallic thin film with an isotropic Fermi surface, neglecting grain boundary scattering and assuming that only electrons at the Fermi energy contribute, the conductivity can be described by the Fuchs–Sondheimer equation,[44,45,73]

$$\frac{\sigma}{\sigma_0} = 1 - \frac{3\lambda}{2h}(1-p)\int_1^\infty \left(\frac{1}{t^3}-\frac{1}{t^5}\right)\frac{1-e^{-ht/\lambda}}{1-pe^{-ht/\lambda}}dt, \tag{5}$$

where σ_0 is the bulk conductivity and λ the magnitude of the bulk mean free path.[44] Mayadas and Shatzkes subsequently extended this model to incorporate grain boundary scattering contributions,[47] which are modeled as a series of partially transparent planes oriented perpendicular to the transport direction x. The distance between neighboring planes follows a normal distribution with average d and variance s. In the regime of large variance s for the distance between grain boundaries (more precisely the linear intercept length, related to the grain size[74,75]), the relaxation time due to grain boundary scattering can be approximated by[47,48]

$$\left(\tau^{\mathrm{gb}}_\mathbf{k}\right)^{-1} = \frac{v^2_\mathbf{k}}{dv_{\mathbf{k},x}}\frac{2R}{1-R}, \tag{6}$$

where $v_\mathbf{k}$ is the magnitude of the velocity and $v_{\mathbf{k},x}$ its component along the x-direction. This expression for the relaxation time can be combined with the bulk electron–phonon relaxation time using Matthiessen's rule, Eq. (2), and the Fuchs–Sondheimer theory, Eq. (5), to derive the thickness- and grain-size dependent resistivity in thin films, given by[48]

$$\rho_{\mathrm{tf}} = \left[\frac{1}{\rho_{\mathrm{gb}}} - \frac{6}{\pi\kappa\rho_0}(1-p)\int_0^{\pi/2} d\phi \int_1^\infty dt \frac{\cos^2\phi}{H^2} \times \left(\frac{1}{t^3}-\frac{1}{t^5}\right)\frac{1-e^{-\kappa t H}}{1-pe^{-\kappa t H}}\right]^{-1}, \tag{7}$$

with $\rho_{\mathrm{gb}} = \rho_0[1-3\alpha/2+3\alpha^2-3\alpha^3\ln(1+1/\alpha)]^{-1}$, $H = 1+\alpha/\cos\phi\sqrt{(1-1/t^2)}$, $\kappa = h/\lambda$, and $\alpha = (\lambda/d)\times 2R(1-R)^{-1}$.

The derivation of Eq. (7) relies on the applicability of Matthiessen's rule for phonon and grain boundary scattering. However, this assumption may break down in nanocrystalline, nearly amorphous films with large disorder.[76–78] In such films, localization effects become prominent,[79,80] typically resulting in a notably reduced temperature coefficient of resistivity compared to bulk materials,[76,78] as well as in different transport mechanisms, which cannot be described by Eq. (7).

By contrast, the derivation of Eq. (7) does not require Matthiessen's rule to apply for surface scattering. In fact, Matthiessen's rule is typically not cromulent for surface scattering and grain boundary scattering in thin metallic films due to the renormalization of the mean free path by grain boundary scattering.[48] Consequently, the individual contributions of bulk, surface, and grain boundary scattering to the thin-film resistivity can be challenging to quantify.[70] Therefore, approximate versions of Eq. (7) that separate these contributions should be used with caution.

04 November 2024 08:02:31

2. Material-dependent scaling of thin-film resistivity

Equation (7) contains five independent material parameters: bulk single-crystal resistivity, electron mean free path, surface/interface scattering specularity, average grain size, and grain boundary reflection coefficient. In practice, the grain size often depends strongly on film thickness, introducing a secondary indirect source of thickness dependence of thin-film resistivity, in addition to surface scattering effects. The relationship between the grain size and film thickness, $d(h)$, is highly sensitive to deposition parameters and is not an intrinsic property of the material. Although a linear dependence has historically been assumed in some cases, experimental data typically do not support this assumption over a wide range of thicknesses [see Fig. 4(a)]. Post-deposition annealing can further influence grain size, promoting grain growth or recrystallization.[81,82]

As a consequence, it is not possible to quantitatively predict the resistivity of metallic nanostructures based solely on bulk properties. As previously mentioned, the relationship $d(h)$ is strongly

© Author(s) 2024

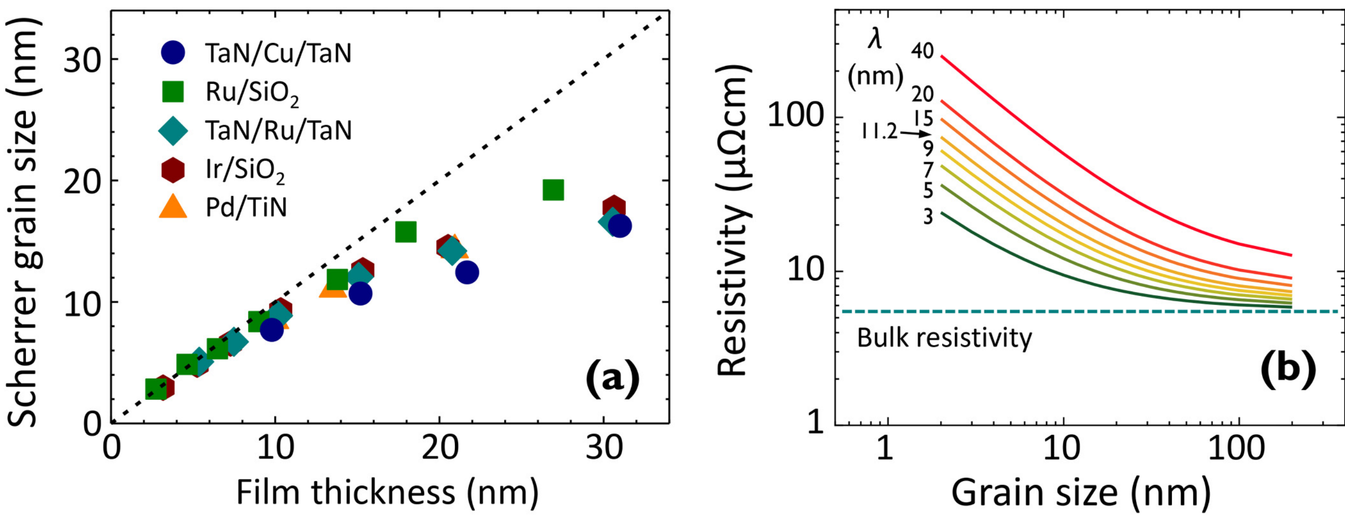


FIG. 4. (a) Experimental Scherrer grain size vs film thickness for various metals deposited by physical vapor deposition and annealed at 420 °C.[70] Reproduced with permission from Dutta *et al.*, J. Appl. Phys. **122**, 025107 (2017). Copyright AIP Publishing LLC. (b) Calculated thin-film resistivity vs grain size using Eq. (7). The parameters employed were $\rho_0 = 5.3\,\mu\Omega$ cm, $R = 0.45$, $p = 0$ (diffuse surface scattering), and film thickness $h = 20$ nm. These parameters, aside from the mean free path λ, are representative of Mo. For bulk Mo, $\lambda = 11.2$ nm.[69] Generally, a shorter mean free path λ results in a weaker dependence of the thin-film resistivity on the grain size.

influenced by deposition process parameters and thermal budget, and no predictive models currently exist for grain structures and grain sizes beyond general trends.[83,84] Given that experimental data indicate that grain boundary scattering can dominate thin-film resistivity,[70] the evaluation of metals should consider the potential for achieving large-grain films (or nanowires). However, this cannot be reliably predicted by *ab initio* calculations, requiring experimental studies on the grain size and annealing behavior to complement transport and reliability metrics for a more accurate assessment of alternative metals.

A second limitation is the difficulty in calculating or predicting realistic values for the parameters R and p. The parameter R represents the electron reflection probability at a grain boundary, which generally depends on the relative orientation of grains on either side of the boundary and the atomic configuration of the grain boundary itself. Both theoretical calculations[85–88] and experimental studies[66,89] consistently show significant variations in R between small-angle or coincidence grain boundaries (with low R) and large-angle random grain boundaries (with higher R). In polycrystalline films, the relevant value of R is an effective average across all grain boundary configurations, making it strongly dependent on the film's microstructure. While some trends suggest that larger cohesive energies lead to higher R values,[90] R should not be treated as an intrinsic property of the metal alone.

Similarly, the surface scattering specularity, p, is influenced not only by the metal itself but also by the properties of the adjacent surfaces or interfaces. The cladding material[54,91–93] and surface or interface roughness are expected to play critical roles. While theoretical[52–57,59] and experimental[51,53] studies have explored surface scattering as a function of surface roughness, quantitative agreement between theory and experiment remains elusive. Hence, predictive calculations for screening purposes are not feasible. Furthermore, because surface scattering depends on both the cladding material and surface roughness, it cannot be regarded as an inherent material property neither.

However, Sec. II A 1 demonstrates that the increase in resistivity, whether due to surface or grain boundary scattering, scales with the bulk mean free path of the charge carriers, λ. Therefore, the effects of high R, small grains, or diffuse interfaces can be mitigated by a short λ. This is illustrated in Fig. 4(b), which shows the dependence of thin-film resistivity on the grain size, calculated using Eq. (7), for $\rho_0 = 5.3\,\mu\Omega$ cm, $R = 0.45$, $p = 0$ (diffuse surface scattering), and a fixed film thickness of 20 nm as an example. The results indicate that a shorter mean free path, λ, leads to a weaker dependence of resistivity on the grain size, thereby reducing the impact of grain boundary scattering. A similar trend can be observed for the dependence of thin-film resistivity on thickness in the presence of diffuse surface scattering.

This insight has driven the search for metals with short λ as potential alternatives to Cu. At room temperature, the mean free path of Cu is as high as 40 nm,[69] which is large compared to typical state-of-the-art interconnect dimensions and grain sizes. Therefore, metals with much shorter λ promise to be less sensitive to interconnect scaling. An *ab initio* methodology for screening short-λ metals will be introduced in Sec. II C. The complete alternative metal screening process and its current status will be detailed in Sec. IV.

3. Influence of resistivity anisotropy on thin-film resistivity scaling

The thin-film resistivity models discussed above assume a spherical isotropic Fermi surface, effectively treating the metal as a

04 November 2024 08:02:31

© Author(s) 2024

free-electron gas with an effective mass. Consequently, both bulk and thin-film resistivities are independent of the crystallographic direction of the current, enabling the derivation of the Fuchs–Sondheimer and the Mayadas–Shatzkes equations in Eqs. (5) and (7), respectively. Due to the inherent complexity of the problem, no thin-film resistivity model currently exists that accounts for the detailed band structure of the metal while incorporating both surface and grain boundary scattering. While the Mayadas–Shatzkes model in Eq. (7) has been able to successfully describe experimental measurements,[67,70,94–101] the lack of a quantitative understanding of key model parameters, such as R and p, limits the ability to accurately evaluate the validity of the spherical Fermi surface approximation across different metals.

From a macroscopic perspective, the resistivity of cubic crystal systems is isotropic, making the approximation of a spherical Fermi surface potentially valid for such metals. However, in less symmetric structures (e.g., hexagonal, tetragonal, orthorhombic, monoclinic, and trigonal), the resistivity becomes anisotropic in the bulk metal. For example, hexagonal Ru exhibits lower resistivity along the hexagonal axis compared to the two perpendicular (in-plane) directions.[102,103] To address this, a semiclassical model based on the Mayadas–Shatzkes framework was developed for ellipsoidal Fermi surfaces.[104] This model can describe metals with hexagonal, tetragonal, or orthorhombic crystal symmetries. While the mathematical details are beyond the scope of this Tutorial, the model reveals a significant influence of Fermi surface anisotropy on surface scattering without affecting grain boundary scattering.

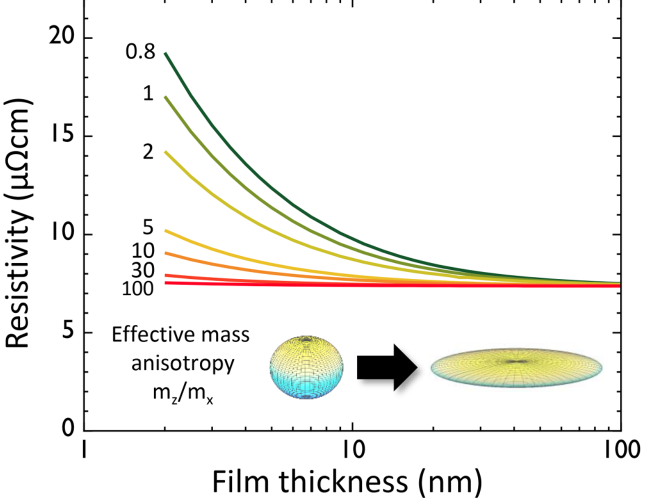


FIG. 5. Calculated thin-film resistivity vs film thickness for various conduction band effective mass anisotropies, considering surface scattering effects. The model details are provided in Ref. 104. The parameters employed were $\rho_0 = 7.4\,\mu\Omega$ cm, $\lambda = 6.8$ nm, $R = 0$ (no grain boundary scattering), and $p = 0$ (diffuse surface scattering). These parameters are representative of Ru. For bulk Ru, the intrinsic effective mass anisotropy is 0.8. The results demonstrate that an oblate anisotropy, characterized by low in-plane resistivity (a low in-plane effective mass) and high out-of-plane resistivity (a high out-of-plane effective mass), reduces surface scattering and consequently yields a weaker dependence of the thin-film resistivity on thickness.

This behavior is illustrated in Fig. 5, which shows the thin-film resistivity as a function of film thickness, with varying degrees of Fermi surface anisotropy, based on the model from Ref. 104. In these simulations, grain boundary scattering was neglected ($R = 0$), allowing surface scattering to dominate. The results demonstrate that in metals with low in-plane resistivity (corresponding to a small in-plane effective mass) and high out-of-plane resistivity (a large out-of-plane effective mass), surface scattering is progressively suppressed, leading to a reduction in the thickness dependence of the thin-film resistivity due to surface scattering.

In principle, this anisotropy effect could be exploited to reduce the resistivity of nanowires, and therefore, the use of two-dimensional and one-dimensional metals (with a single low-resistivity crystallographic direction) in interconnect applications has been proposed.[105] However, two important considerations must be noted. First, since Matthiessen's rule does not generally apply, the presence of significant grain boundary scattering—which is unaffected by reduced dimensionality—can suppress the benefits of surface scattering reduction in two- or one-dimensional metals, particularly in small-grain microstructures. Second, the application of one-dimensional metals in interconnects would necessitate single-crystal materials to ensure that the current is always aligned with the low-resistivity crystallographic direction. Currently, there is no established integration route for incorporating single-crystal lines in commercial interconnects, limiting the practical application of such materials to fundamental material science at this stage.

04 November 2024 08:02:31

B. Point defects, disorder, and alloy scattering in compound metals

Before introducing first-principles screening methodologies for identifying and selecting promising metals for interconnect applications based on the mean free path of charge carriers, λ, it is essential to briefly discuss additional sources of scattering that are particularly relevant for compound metals. In crystalline materials, any deviation from periodicity can result in electron scattering.[106] In elemental metals, such deviations include vacancy or vacancy cluster defects as well as impurities. In high-quality polycrystalline thin films of relevant metals, vacancies and impurities primarily influence the resistivity at cryogenic temperatures, but their effects are generally negligible at room temperature, where scattering by phonons, grain boundaries, and surfaces dominates.

The situation can, however, be markedly different for compound metals. Alloys are inherently disordered materials, characterized by the random distribution of different atoms on lattice sites. As a result, the crystal lacks periodicity, leading to increased resistivity due to alloy scattering. This effect is illustrated in Fig. 6 for the seminal Cu–Au system.[107] In disordered Cu_xAu_{1-x} alloys, the resistivity is considerably higher than in the pure elemental metals Cu and Au, reaching a maximum at 50% Au content, where disorder is the greatest. By contrast, the system also forms two ordered intermetallic phases, Cu_3Au and CuAu, near their respective stoichiometries. In these ordered phases, the resistivity shows a sharp minimum, significantly lower than that of the disordered alloys.

© Author(s) 2024

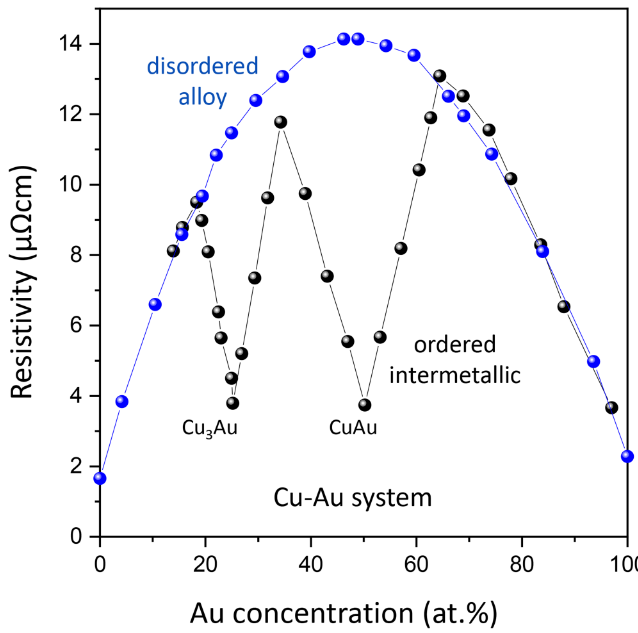


FIG. 6. Resistivity of Cu_xAu_{1-x} intermetallic compounds as a function of Au mole fraction. Randomly disordered alloys exhibit much higher resistivities due to alloy scattering, with a resistivity maximum at 50% Au. In contrast, ordered Cu_3Au and CuAu intermetallics display significantly lower resistivities near their stoichiometric compositions.[107,108]

These observations highlight the necessity of minimizing alloy scattering to achieve resistivities relevant for interconnect applications in compound metals. As a result, in addition to elemental metals, for which such issues do not arise, only ordered intermetallics are of potential interest in alternative metal screening efforts. This challenge is further compounded by the difficulty of accurately measuring and optimizing intermetallic ordering in thin films. A more detailed discussion and the current state of the art can be found in Secs. IV C and IV D.

C. *Ab initio* screening of alternative metals

The discussions in Secs. II A 2 and II A 3 emphasize that accurately predicting the resistivity of thin films or nanowires is not feasible without detailed microstructural information, which is inherently dependent on deposition process conditions. Additionally, resistivity models, such as the Mayadas–Shatzkes model in Eq. (7), rely on the assumption of a spherical Fermi surface (free-electron gas), and metal-specific scaling is represented solely by a single mean free path value. While it is possible to compute the electron–phonon-limited resistivity of metals from first principles by considering detailed band structures,[109] such calculations remain computationally intensive, restricting feasible system sizes to only a few atoms per unit cell. The primary limitation is the computational cost of calculating the electron–phonon coupling and the corresponding relaxation times. Moreover, incorporating grain boundaries into this framework is highly challenging. To date, these factors constrain the development of a fully predictive downselection methodology capable of directly identifying the most promising metal candidates for interconnect applications.

Consequently, the metal selection problem must be approached in stages, as outlined in Fig. 3. Nevertheless, screening metals of potential interest remains feasible using a $\rho_0 \times \lambda$ figure of merit, which can be computed using *ab initio* methods with relatively low computational cost, as introduced below. The application of this methodology for screening elemental and compound metals will be discussed in Sec. IV.

In the Boltzmann transport framework, the conductivity tensor for a bulk metal film is expressed by Eq. (3) as

$$\underline{\underline{\sigma}} = \frac{-e^2}{N_{\mathbf{k}}\Omega} \sum_{n,\mathbf{k}} \tau_{n\mathbf{k}} \frac{\partial f^0_{n\mathbf{k}}}{\partial \epsilon_{n\mathbf{k}}} \mathbf{v}_{n\mathbf{k}} \otimes \mathbf{v}_{n\mathbf{k}}. \tag{8}$$

As noted above, the calculation of the conductivity tensor requires the knowledge of the relaxation time $\tau_{n\mathbf{k}}$, which is costly to calculate by *ab initio* methods. In general, $\tau_{n\mathbf{k}}$ of an electron depends on its wavevector $\mathbf{k}$ and band index n; therefore, metals typically show a broad distribution of mean free paths,[72,110] as illustrated in Fig. 7(a) for Cu along two crystallographic directions.

Nevertheless, the complexity of the problem can be reduced by assuming an isotropic constant relaxation time τ, independent of the electron wavevector $\mathbf{k}$. Under this approximation, Eq. (8) can be simplified by extracting τ from the summation and evaluating the expression only at the Fermi energy, i.e., by replacing the derivative of the Fermi–Dirac distribution by a δ-function. This results in the transport tensor,[69,71]

$$\frac{1}{\underline{\underline{\rho_0 \tau}}} = \frac{e^2}{(2\pi)^3} \sum_n \left\langle \mathbf{v}^{(n)}(\mathbf{k}) \otimes \mathbf{v}^{(n)}(\mathbf{k}) \right\rangle_{\mathrm{BZ}}, \tag{9}$$

where BZ denotes that the summation is performed over the Brillouin zone. The approximation of the Fermi–Dirac distribution derivative to a δ-function has been found to be generally accurate, resulting in temperature-independent transport tensors.[71]

The key advantage of the constant relaxation time approximation is that the right-hand side of Eq. (9) depends only on the morphology of the Fermi surface, eliminating the need for detailed knowledge of electron–phonon interactions. As a result, the calculation of the $\underline{\underline{\rho_0 \tau}}$ transport tensor is computationally much less demanding, rendering it suitable for evaluating a wide range of metals.[69,71]

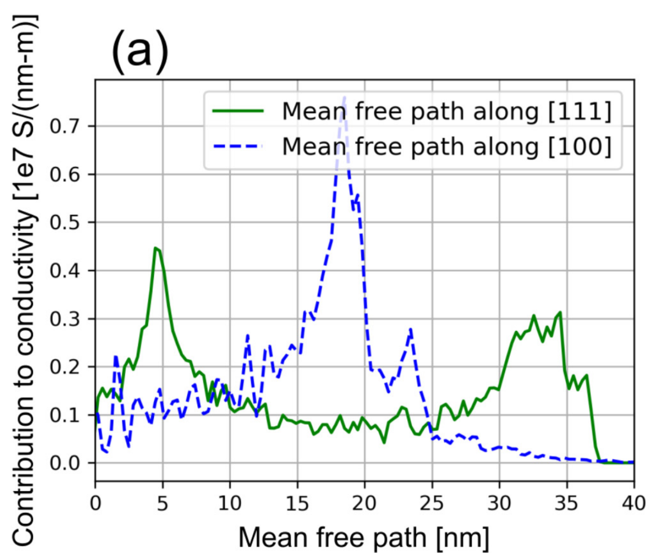
Alternatively, an equivalent transport tensor can be formulated by assuming that the mean free path of the charge carriers $\lambda(\mathbf{k}) = \mathbf{v}^{(n)} \times \tau^{(n)}(\mathbf{k})$ is isotropic and independent of $\mathbf{k}$. This approximation, the constant mean free path approximation, leads to the following transport tensor:[69,71]

$$\frac{1}{\underline{\underline{\rho_0 \lambda}}} = \frac{e^2}{(2\pi)^3} \sum_n \left\langle \frac{\mathbf{v}^{(n)}(\mathbf{k}) \otimes \mathbf{v}^{(n)}(\mathbf{k})}{|\mathbf{v}^{(n)}(\mathbf{k})|} \right\rangle_{\mathrm{BZ}}. \tag{10}$$

It is worth noting that a $\underline{\underline{\rho_0 \lambda}}$ tensor can also be derived within the

04 November 2024 08:02:31

© Author(s) 2024



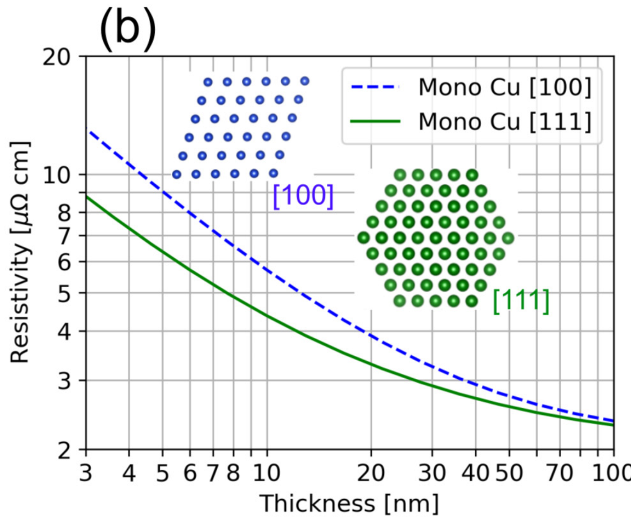


FIG. 7. (a) Decomposition of the electrical conductivity for Cu as a function of the mean free path along the [111] and [100] crystallographic directions. The distinct profiles observed along these two directions can be attributed to the Fermi surface anisotropy. (b) *Ab initio* calculations of the film thickness dependence of the resistivity for monocrystalline Cu with two different surface normal orientations considering surface scattering effects. Computational details are the same as those in Ref. 72.

constant relaxation time approximation by dividing the $\underline{\underline{\rho_0\tau}}$ transport tensor by the Fermi–Dirac weighted average velocity,

$$v \equiv \frac{\sum_n \langle |\mathbf{v}^{(n)}(\mathbf{k})| \rangle_{bz}}{\sum_n \langle 1 \rangle_{bz}}. \tag{11}$$

While the numerical values of the various transport tensors may exhibit discrepancies for a given metal due to the inherent approximations, screening methodologies based on these tensors generally yield consistent results. Consequently, both approaches can be used interchangeably for screening purposes.

One practical application of this approach involves the approximate determination of a single-valued mean free path λ (or relaxation time τ) of a metal when the bulk resistivity ρ_0 is known, for instance, from experimental data. It is noteworthy that for cubic systems, the $\underline{\underline{\rho_0\lambda}}$ and $\underline{\underline{\rho_0\tau}}$ tensors are diagonal and, thus, reduce to a single isotropic value.[69] Many semiclassical thin film transport models, such as the Mayadas–Shatzkes model in Eq. (7),[48] assume a simplified isotropic free-electron gas and consequently neglect band structure effects, including their influence on the mean free path. For real metals with complex band structures, it may be possible to replace the exact **k**-dependent mean free path by an effective mean free path. However, rigorous calculations of the electron–phonon coupling are required for accurate determination of this effective value. Therefore, the λ value extracted from the $\underline{\underline{\rho_0\lambda}}$ tensor (divided by the bulk resistivity ρ_0) has been utilized as an effective mean free path in thin-film transport models. Given the experimental challenges associated with directly measuring the mean free path,[111] the accuracy of this approximation remains uncertain. Nevertheless, employing $\underline{\underline{\rho_0\lambda}}$-derived values for the mean free path has generally led to satisfactory agreement between semiclassical transport models and experimental observations.[67,70,94–101]

Second, the $\underline{\underline{\rho_0\lambda}}$ tensor can serve as a figure of merit for a metal, indicating its potential for achieving low resistivity at nanoscale dimensions. Lower values of this tensor correspond to metals with greater scaling potential. Consequently, both the $\underline{\underline{\rho_0\lambda}}$ and $\underline{\underline{\rho_0\tau}}$ tensors have been extensively employed to identify promising alternative metals for nanoscale interconnect applications. A significant advantage of this approach lies in its substantially reduced computational cost compared to independently calculating the electron–phonon mean free path and bulk resistivity, enabling the screening of a wide range of materials. However, given the inherent approximations, the screening results should be interpreted with caution, as they may not accurately predict the thin film resistivity (see also Sec. II A 2). Nevertheless, this screening methodology has proven valuable, and the current state-of-the-art techniques utilizing this approach for alternative metal screening are discussed in Sec. IV.

04 November 2024 08:02:31

D. Resistivity scaling for thin films and nanowires in the presence of surface scattering

While the methodology introduced in Sec. II C has been successfully applied to screening both elemental and compound metals, its accuracy in predicting thin-film or nanowire resistivities is limited. In reality, the mean free path of charge carriers depends strongly on their wavevector **k**. As depicted in Fig. 7(a) for Cu, the mean free path varies significantly along different directions on the Fermi surface. Consequently, incorporating the complete anisotropic band structure into transport calculations and screening efforts is essential for achieving a more accurate understanding of resistivity at nanoscale dimensions.

© Author(s) 2024

Equation (4) captures the rescaling of the bulk relaxation time, accounting for all pertinent scattering mechanisms. It should be noted that grain boundary scattering can be implicitly accounted for through an effective mean free path. Under the assumption of a spherical Fermi surface, the analytical Mayadas–Shatzkes model, as expressed in Eq. (7), can be derived. Incorporating the full electronic band structure yields the following expression:

$$\frac{\tau_{n\mathbf{k}}}{\tau^0_{n\mathbf{k}}} = 1 + \frac{|\lambda_{n\mathbf{k}}.\hat{u}|}{h}\frac{1-p}{1-p\exp\left(\frac{-h}{|\lambda_{n\mathbf{k}}.\hat{u}|}\right)}\left[1-\exp\left\{\frac{-h}{|\lambda_{n\mathbf{k}}.\hat{u}|}\right\}\right]. \quad (12)$$

Here, $\tau^0_{n\mathbf{k}}$ represents the relaxation time, accounting for both phonon and grain boundary scattering.

When grain boundary scattering is neglected (i.e., considering only phonon and surface scattering), the thin film resistivity can be predicted *ab initio*. The calculated relationship between thin-film resistivity and film thickness for Cu is shown in Fig. 7(b). It is important to note that Eq. (12) indicates that the resistivity of thin films (or nanowires) depends not only on the transport direction but also on the orientation of the surface normal (growth orientation). This holds true even for metals with isotropic bulk resistivity, such as cubic metals, including Cu, and can be explained by the reduced symmetry arising from dimensional confinement.

For single-crystal films with negligible grain boundary scattering, the results are, in principle, exact, apart from the usual approximations inherent to density functional theory (DFT). While grain boundary scattering in textured films could theoretically be incorporated via a grain-size-dependent mean free path, its accurate treatment relies heavily on the knowledge of the detailed microstructure and remains challenging for current *ab initio* techniques.

Beyond transport calculations, the proposed model can also be extended to derive a figure of merit for thin films or nanowires, analogous to the $\underline{\underline{\rho_0\lambda}}$ tensor in Eq. (10). For a thin film with surface normal $\hat{\boldsymbol{u}}$, we find[72]

$$\left.\frac{1}{\rho\lambda(\hat{\mathbf{u}})}\right|_{\text{film}} = -\frac{n_s e^2}{N_{\mathbf{k}}\Omega}\sum_{|\hat{\mathbf{v}}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|>\theta}\frac{\partial f_{n,\mathbf{k}}}{\partial\varepsilon}\frac{|\mathbf{v}_{n,\mathbf{k}}\cdot\hat{\mathbf{n}}|^2}{2|\mathbf{v}_{n\mathbf{k}}||\hat{\mathbf{v}}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|}. \quad (13)$$

To prevent divergence, an angular cutoff θ was introduced. The unit vector $\hat{\mathbf{n}}$ represents the in-plane transport direction.

The expression for a nanowire is given by[72]

$$\left.\frac{1}{\rho\lambda(\hat{\mathbf{u}},\hat{\mathbf{s}})}\right|_{\text{wire}} = -\frac{n_s e^2}{N_{\mathbf{k}}\Omega}\sum_{|\hat{\mathbf{v}}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|>\theta,|\hat{\mathbf{v}}_{n\mathbf{k}}\cdot\hat{\mathbf{s}}|>\theta}\frac{\partial f_{n,\mathbf{k}}}{\partial\varepsilon}|\mathbf{v}_{n,\mathbf{k}}\cdot\hat{\mathbf{n}}|^2\tau^{nw}_{n\mathbf{k}}, \quad (14)$$

with $\tau^{nw}_{n\mathbf{k}}$ given by the expression[72]

$$\begin{cases} \tau^{nw}_{n\mathbf{k}} \approx \frac{h}{2|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|}\left(1-\frac{h}{w}\frac{|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|}{|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{s}}|}\right)+O(h^3) \text{ if } w|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|<h|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{s}}|, \\ \tau^{nw}_{n\mathbf{k}} \approx \frac{w}{2|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|}\left(1-\frac{w}{h}\frac{|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{s}}|}{|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|}\right)+O(h^3) \text{ if } w|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|>h|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{s}}|, \\ \tau^{nw}_{n\mathbf{k}} \approx \frac{h}{3|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|}+O(h^4) \text{ if } w|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{u}}|=h|\mathbf{v}_{n\mathbf{k}}\cdot\hat{\mathbf{s}}|. \end{cases} \quad (15)$$

Here, $\hat{\mathbf{s}}$ and $\hat{\mathbf{u}}$ denote the two confinement directions corresponding to the width w and thickness h, respectively. An alternative formulation to the thin-film and nanowire figures of merit has been proposed in Ref. 105 and leads to comparable results in terms of metal benchmarking.

This figure of merit accounts for anisotropic transport effects, such as the suppression of surface scattering discussed in Sec. II A 3, making it particularly suitable for single-crystal wires, in which transport occurs in well-defined crystallographic directions. For certain crystalline orientations, this can result in highly favorable figures of merit for specific materials, in particular, one-dimensional metals.[105] However, it is important to note that in random polycrystalline films and nanowires, surface scattering is averaged over all grain orientations. Additionally, in films or nanowires where resistivity is predominantly governed by grain boundary scattering (e.g., in small-grain polycrystalline films), the suppression of surface scattering is significantly reduced (see Sec. II A 3). Under these conditions, benchmarking metals using Eq. (10) remains the most appropriate approach.

III. INTERCONNECT RELIABILITY

A second critical aspect in selecting new metallization schemes for interconnects is the reliability of both the metal and the surrounding dielectric materials. Interconnect failure can originate from degradation in either the metal or the dielectric. Analogous to line resistance, interconnect reliability tends to deteriorate as wires and vias are miniaturized. Initially, the limited electromigration resistance of Al led to the adoption of Cu as the primary interconnect metallization more than two decades ago.[34] However, the reliability of Cu metallization is now facing increasing challenges. As elaborated in Secs. III A and III B, barrier and liner layers are essential for maintaining reliability but must be scaled alongside interconnect dimensions to leave sufficient room for the Cu conductor. Due to the limited scalability of these layers, they eventually occupy a substantial fraction of the interconnect volume while contributing minimally to the overall conductance. As demonstrated in Sec. V using calibrated line resistance models, barrier- and liner-less metallization is essential for realizing low-resistance interconnects, outperforming current Cu-based metallization schemes. In Secs. III A and III B, we will delve into the fundamentals of both metal and dielectric reliability. The current state of the art regarding the reliability of specific elemental and binary alternative metals will be explored in Sec. IV.

04 November 2024 08:02:31

A. Dielectric breakdown and the need for barrier layers

Time-dependent dielectric breakdown (TDDB) is a physical degradation process in which a dielectric material, subjected to a constant electric field below its intrinsic breakdown strength, progressively deteriorates and ultimately fails over time. This failure can be attributed to the formation of conductive paths (filaments) within the dielectric, which can short-circuit adjacent metallic electrodes.[112] Rapid failure may result either from gradual intrinsic damage to the dielectric material (e.g., vacancy formation) or from the drift of metal from nearby interconnect lines or vias. In the latter scenario, metal ions drift through the dielectric under the influence of the applied electric field, contaminating the dielectric,

© Author(s) 2024

increasing leakage currents, and ultimately causing dielectric breakdown and shorting between interconnect lines.[113,114]

The time-dependent dielectric breakdown behavior depends on the materials used, both metals and dielectrics. For metals, there exists a thermodynamic barrier that determines the detachment of ionized metal atoms and their subsequent drift or diffusion into the low-κ dielectric. This barrier generally scales with the metal's cohesive energy. Consequently, refractory metals, which exhibit significantly higher cohesive energies compared to Cu, present a higher barrier, thereby suppressing the drift and diffusion of metal ions into the dielectric and resulting in a substantially longer time-dependent dielectric breakdown lifetime. It is important to note that the drift and diffusion of metal ions *within* the dielectric are less influenced by the cohesive energy of the metal and are instead primarily dependent on the binding energy of metal impurities in the dielectric. Nevertheless, for metals relevant to interconnects, the dominant thermodynamic barrier arises from the detachment energy. Therefore, metals with high cohesive energy (i.e., refractory metals) are expected to exhibit significantly improved time-dependent dielectric breakdown lifetimes.

Moreover, the selection of dielectrics also influences the time-dependent dielectric breakdown performance of interconnects. Advanced interconnects utilize low-κ materials to minimize interconnect capacitance.[115–118] The low dielectric permittivity κ of these dielectrics is typically associated with a reduced dipole density, either intrinsically due to their composition or by decreasing physical density, such as through the introduction of porosity. This can have a pronounced impact on time-dependent dielectric breakdown behavior, as it is well-established that Cu readily detaches and diffuses in such dielectrics, leading to rapid dielectric breakdown. As a result, Cu interconnects require the use of refractory barrier layers between the dielectric and the Cu metallization to prevent Cu detachment and drift into the dielectric. In general, amorphous barrier materials are preferred over polycrystalline counterparts, as grain boundaries can act as diffusion pathways. Currently, TaN is employed as the primary barrier material, with the potential for being scaled down to thickness around 1–1.5 nm without compromising functionality.[119,120] Ongoing research has explored alternative barrier materials, such as Zn-doped Ru,[121] though their integration poses challenges and is not expected to yield significant improvements over TaN barriers.

Beyond intrinsic material properties, process limitations and dimensional scaling can further compromise time-dependent dielectric breakdown behavior. Factors, such as narrow gaps, line-edge roughness, plasma-induced damage, and misalignment (see Fig. 8), can all contribute to dielectric degradation. Therefore, selecting a suitable alternative metal for advanced interconnects should not only be based on its intrinsic properties (such as the metal detachment barrier) but also on its compatibility with integration processes, as the introduction of new materials can exacerbate dielectric breakdown. It is, thus, crucial to experimentally evaluate time-dependent dielectric breakdown performance using appropriate test structures, such as planar capacitors (PCAPS)[122] or sidewall capacitors (SWCAPS),[123] to facilitate the downselection of promising alternative metals.

The primary driving forces behind time-dependent dielectric breakdown are the applied electric field and the temperature of the interconnect. In practice, time-dependent dielectric breakdown constrains the maximum electric field that can be safely applied between adjacent lines, making it a critical consideration in circuit design and layout. For commercial circuits, lifetime requirements are typically set at 10 years for temperatures up to 135 °C. Direct measurement of such long lifetimes is impractical; therefore, the maximum electric field for reliable operation is determined through extrapolation from accelerated tests conducted at elevated temperatures and electric fields. There is an ongoing debate in the literature regarding the most appropriate model for time-dependent dielectric breakdown lifetime extrapolation, with several proposed models,[124]

$$E\text{−model}: \quad t_{50\%} \propto \exp(-\gamma E), \tag{16}$$

$$\sqrt{E}\text{−model}: \quad t_{50\%} \propto \exp\left(-\gamma\sqrt{E}\right), \tag{17}$$

$$\text{Power − law model}: \quad t_{50\%} \propto E^{-m}, \tag{18}$$

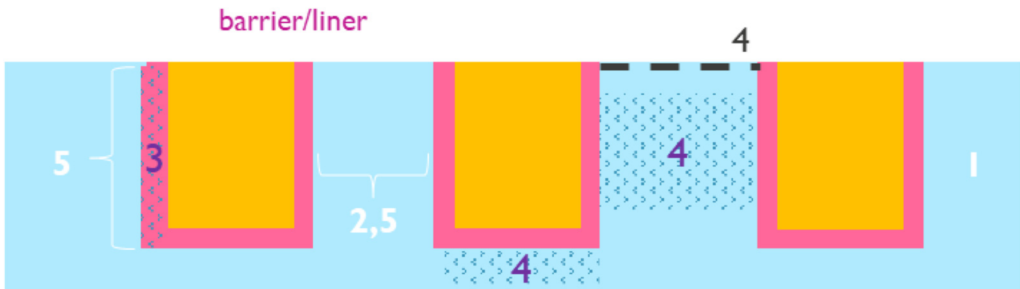


FIG. 8. Illustration of factors influencing time-dependent dielectric breakdown and interconnect lifetime: (1) intrinsic dielectric properties, breakdown location, and mechanism; (2) insulating dielectric thickness; (3) barrier properties and conductor metal detachment; (4) dielectric damage induced by integration processes, such as barrier deposition, chemical–mechanical polishing, etching, or moisture absorption; and (5) line variability, including line-edge roughness, trench height, or via misalignment.

04 November 2024 08:02:31

© Author(s) 2024

$$\text{Impact damage model:} \qquad t_{50\%} \propto \frac{\exp\left(-\gamma\sqrt{E}+\frac{\alpha}{E}\right)}{E}, \tag{19}$$

$$1/E\text{—model:} \qquad t_{50\%} \propto \exp\left(\frac{\gamma}{E}\right). \tag{20}$$

Here, $t_{50\%}$ represents the time elapsed before a line fails with a probability of 50%. The impact damage model, also known as the lucky electron model, is widely regarded to most accurately describe the underlying physical mechanisms of time-dependent dielectric breakdown.[125] However, some researchers prefer the power-law model for fitting time-dependent dielectric breakdown data, as it offers reliable predictions with a limited number of fitting parameters.[124,126,127] In contrast, studies on damascene structures[128,129] have found that both the E- and $\sqrt{E}$-models tend to be overly conservative in fitting low-field time-dependent dielectric breakdown data. The behavior of these models, along with their comparison to experimental data for Cu, is depicted in Fig. 9. It is important to note that additional area scaling and extrapolation to low failure percentiles are necessary to determine failure rates and define operating condition limits for industry-relevant interconnects.[130]

Accelerated time-dependent dielectric breakdown testing can also provide insights into the underlying failure mechanisms, such as whether breakdown occurs via dielectric failure or through the formation of metal filaments. Typical bias-temperature stress experiments employ PCAPs or SWCAPs at elevated temperatures, using methods, such as triangular voltage sweeps or the application of constant voltage (see Fig. 10). For capacitors with different electrodes—one consisting of the metal of interest and the other of a refractory metal—metal drift can be identified and distinguished from intrinsic breakdown by comparing results under positive and negative bias. For instance, under positive voltage stress applied to the weak top electrode in a PCAP [Fig. 10(a)], and in the absence of an effective diffusion barrier, metal ions will drift into the dielectric [Fig. 10(b)]. In contrast, no metal drift is observed under negative voltage stress [Fig. 10(c)]. This allows for the differentiation between the metal drift and intrinsic dielectric breakdown mechanisms, as the latter are not dependent on bias polarity [Figs. 10(d) and 10(e)].

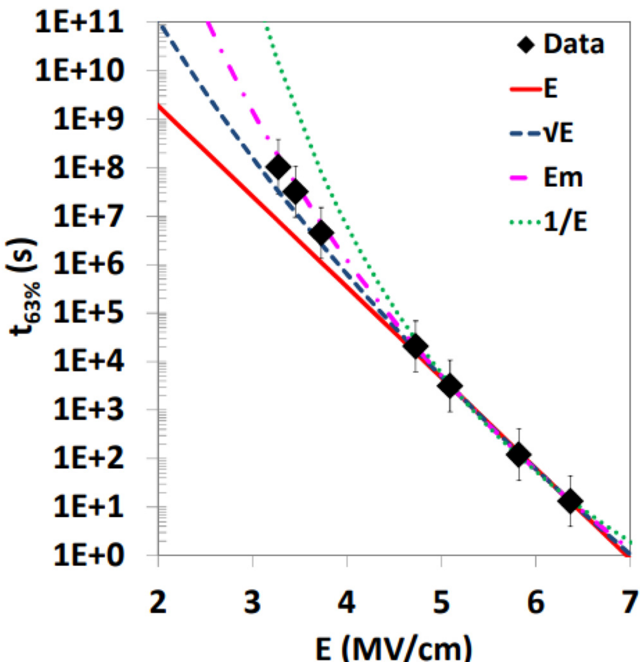


FIG. 9. Comparison of the available models for time-dependent dielectric breakdown lifetime extrapolation vs measured data for Cu.[124] Reproduced with permission from Croes *et al.*, in *2013 IEEE International Reliability Physics Symposium*, pp. 2F.4.1–2F.4.8 (2013). Copyright 2013 IEEE.

Alternatively, during triangular voltage sweeps, metal drift can be detected when the leakage current increases during the initial sweep but disappears in subsequent sweeps, indicating that metal ions have migrated through the dielectric [Figs. 10(f)–10(i)]. Time-dependent dielectric breakdown measurements conducted at various temperatures and voltages enable the study of conditions associated with intrinsic breakdown, metal filament growth, and filament formation.[131] Given that these mechanisms are influenced by the metal, the dielectric material, and their respective thicknesses, it is crucial to continuously refine testing methodologies for alternative metals and advanced interconnects.

From a dielectric breakdown perspective, the primary limitation in scaling Cu interconnects is the requirement for barrier layers to prevent metal detachment and drift into the surrounding dielectrics. As interconnect dimensions shrink, these barriers—having significantly higher resistance than Cu—occupy a substantial fraction of the interconnect volume, which ultimately impedes effective metal fill at ultrasmall dimensions. As discussed further in Sec. V, this results particularly in a sharp increase in line resistance for interconnects with widths below 10 nm, necessitating the adoption of barrierless alternative metallization strategies.

04 November 2024 08:02:31

B. Electromigration

Electromigration (EM) is a well-documented main failure mechanism in integrated circuits. When an electric current flows through a conductor, the metal atoms are subjected to two opposing forces: the direct force exerted by the electric field and the force arising from a momentum transfer (the "electron wind") from the moving electrons [see Fig. 11(a)].

Over time, the electron wind can induce metal atoms to migrate in the direction of electron flow, from the cathode to the anode. This migration results in metal atom depletion at the cathode, leading to the formation of voids [Figs. 11(b) and 11(c)] and ultimately causing open circuits. Conversely, metal atoms accumulate at the anode, promoting hillock formation [Fig. 11(b)] and potentially leading to short circuits.[132]

The driving force F_{EM}, also known as the electron wind force F_{wind}, governing the electromigration process[135] can be expressed as

$$F_{EM} = Z^{*} e\rho \times j_e, \tag{21}$$

where ρ represents the metal resistivity, j_e denotes the electron current density, Z^{*} is the effective ion valence, and e is the charge of an electron.

© Author(s) 2024

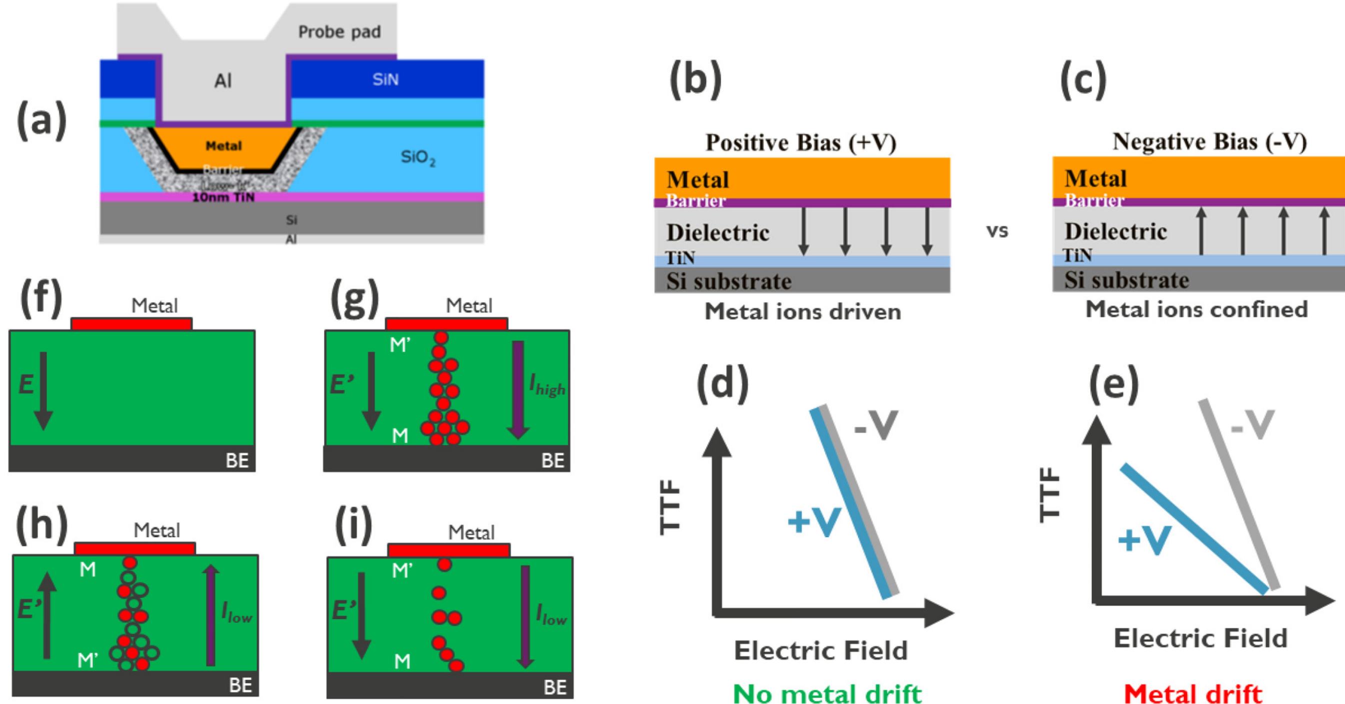


FIG. 10. (a) Device structure of a planar capacitor (PCAP) used for time-dependent dielectric breakdown lifetime measurements. (b) and (c) Schematics of metal drift processes under constant voltage stress. For weak metal top electrodes, metal ions can migrate during positive voltage, while metal drift does not occur under negative bias. (d) and (e) Time-to-failure (TTF) behavior as a function of applied bias voltage $\pm V$. (f)–(i) Illustration of metal filament formation and dissolution during triangular voltage sweeps with applied electric fields E as indicated.

04 November 2024 08:02:31

Einstein's equation relates the atomic mass flux J to the electron wind force,

$$J = \frac{DC}{k_B T} \times F_{EM}, \tag{22}$$

where C is the atom concentration, D is the diffusion constant given by $D = D_0 \exp\left(-\frac{E_A}{k_B T}\right)$, with D_0 representing the effective diffusivity along different paths, E_A the activation energy for the dominant diffusion pathway, k_B the Boltzmann constant, and T the temperature.

In a metal line, atoms can diffuse through various pathways: within the bulk of the line, along grain boundaries, and at the interface between the metal and the dielectric. The predominant diffusion path is material-dependent and is determined by its activation energy E_A, which, in turn, is governed by the bonding energy of the crystal metal lattice. In Cu interconnects, voids arising from electromigration typically nucleate at the top interface between Cu and the dielectric barrier (typically SiN or SiCN), and void growth subsequently proceeds through grain boundaries.[136–139]

One of the critical challenges of downscaling interconnect dimensions is the rapid increase in the relative volume of atoms diffusing along interfaces and grain boundaries, coupled with a decrease in the overall metal volume. This combination leads to a pronounced degradation in the electromigration lifetime of scaled Cu interconnects.[140,141] As a result, the maximum current densities that can be carried reliably (with a 10-year lifetime at 135 °C) steadily decrease in scaled interconnects, imposing increasingly stringent constraints on circuit design and layout.

The reduction in electromigration lifetimes for scaled interconnects has been mitigated (slowed) by the introduction of liner layers between TaN barriers and Cu conductors, particularly at the top interface of the line. Co has been the primary liner material in recent technology nodes, with Ru/Co bilayer liners emerging. However, similar to the TaN barrier, which prevents Cu drift into surrounding dielectrics, the thickness of liner layers poses significant challenges for scaling.[119,120,142] Prefill techniques offer a potential alternative to improve reliability, although they introduce additional process complexities.[143,144] Analogous to the TaN diffusion barriers, liners contribute minimally to the overall line conductance while occupying an increasing fraction of the line volume. This reduces the available space for the primary conductor (i.e., Cu), leading to a sharp rise in line resistance as interconnect dimensions are scaled down.

An alternative approach to liner scaling is the use of conductor metals with intrinsically high resistance to electromigration, offering significantly better electromigration performance than Cu. Since the activation energy E_A for electromigration generally scales

© Author(s) 2024

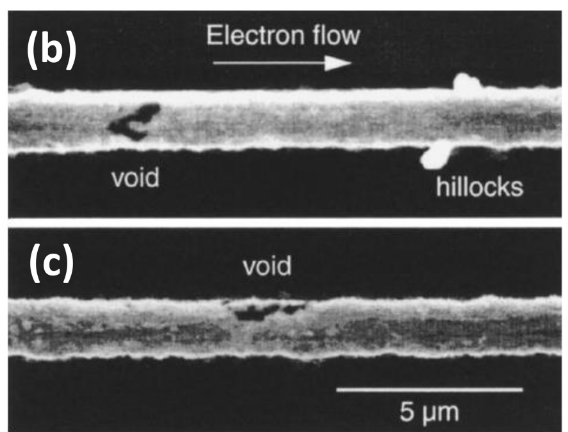


FIG. 11. (a) Schematic illustrating the electromigration driving force in a metal (F_{wind}).[133] (b) and (c) Scanning electron micrographs of hillocks and voids induced by electromigration in a Cu line.[134] Reproduced with permission from Ryu *et al.*, IEEE Trans. Electron Devices **46**, 1113 (1999). Copyright 1999 IEEE.

with the cohesive energy of the metal, refractory metals with high melting points present a promising solution. It is noteworthy that metals with high cohesive energies are also advantageous for barrierless dielectric reliability, suggesting that the material properties influencing the different reliability aspects are related. The critical importance of selecting alternative metals with high potential for barrier- and liner-free, reliable metallization schemes is further explored in Sec. V.

C. Self-heating and thermal properties

As previously discussed, the reliability of metal interconnects is heavily influenced by the absolute temperature at critical points within the interconnect structure, as well as the temperature gradients present throughout the metal stack. The temperature in the interconnect is determined by several factors: the thermal resistance of the interconnect structure, the thermal coupling between the interconnects and the heat-generating transistors, self-heating within the interconnect, and the thermal interactions between adjacent metal lines.

As interconnect dimensions continue to shrink and low-κ dielectrics are introduced, thermal management becomes increasingly critical. Due to the typically low thermal conductivity of low-κ interlayer dielectrics (as low as $0.3\,\mathrm{W\,m^{-1}\,K^{-1}}$ for OSG 3.0, an organosilicate glass with a dielectric constant of $\kappa = 3.0$),[145,146] heat dissipation within the interconnect stack predominantly occurs through metal lines and vias and is highly dependent on the thermal conductivity of the metals and their connectivity scheme.[147] The scaling of metal linewidth and thickness leads to a reduction in thermal conductivity, an increase in electrical resistivity (see Sec. II), aggravating self-heating, and an enhanced contribution of barrier thermal resistance.[147] As a result, the interconnect stack exhibits higher thermal resistance, with interconnect thermal resistance becoming the dominant factor in overall thermal resistance for advanced packages, leading to increased self-heating of the metal interconnects.[148]

Given that the thermal behavior of interconnect structures is primarily governed by the metallization, accurately predicting the thermal properties of alternative metals is crucial. Interconnect-level thermal models[149,150] can account for factors, such as the metal line density, the via density, and the connectivity between various metal layers. However, these models must also incorporate the size-dependent behavior of the materials to provide a comprehensive understanding of thermal performance.

To accurately capture ballistic thermal transport effects involving both electrons and phonons, *ab initio* simulations can be employed to predict the thermal conductivity of relevant materials. In bulk metals, the total thermal conductivity K_0 is the sum of contributions from all electron (K_{el}) and phonon (K_{ph}) modes, given by

$$\begin{aligned} K_0 &= K_{el} + K_{ph} \\ &= \sum_{\mathbf{k}} C_{el}(\mathbf{k}) v_{el}^2(\mathbf{k}) \tau_{el}(\mathbf{k}) + \sum_{\mathbf{q}} C_{ph}(\mathbf{q}) v_{ph}^2(\mathbf{q}) \tau_{ph}(\mathbf{q}). \end{aligned} \tag{23}$$

Here, C represents the heat capacity, v is the group velocity, and τ denotes the relaxation time. The subscripts "el" and "ph" refer to the contributions of electrons and phonons, respectively, while $\mathbf{k}$ and $\mathbf{q}$ represent the wavevectors of electrons and phonons, respectively.

In semiconductors or dielectrics, heat is transported primarily by phonons, whereas in metals, electrons are the dominant heat carriers. Consequently, in metals, the thermal conductivity K_0 and the electrical resistivity ρ_0 are related through the Wiedemann–Franz law,

$$K_0 = \frac{LT}{\rho_0}, \tag{24}$$

where L denotes the Lorenz number and T the temperature. For free electrons, $L = 2.4 \times 10^{-8}\,\mathrm{W\Omega\,K^{-2}}$. Many bulk metals exhibit Lorenz numbers close to this free-electron value (e.g., Cu[151]), although certain metals, such as those in the Pt group[152] or W,[151] show Lorenz numbers approximately 10%–15% higher. Such deviations from free-electron behavior typically stem from additional contributions of phonon transport to the thermal conductivity.

To account for the influence of reduced metal dimensions on thermal conductivity, a thin-film model based on the Mayadas–Shatzkes framework[48] (see Sec. II A 1) has been employed to estimate the size-dependent thermal conductivity for various metals (or metal stacks). Experimentally calibrated reflection coefficients and surface specularity parameters (see Sec. IV) were used. This

04 November 2024 08:02:31

© Author(s) 2024

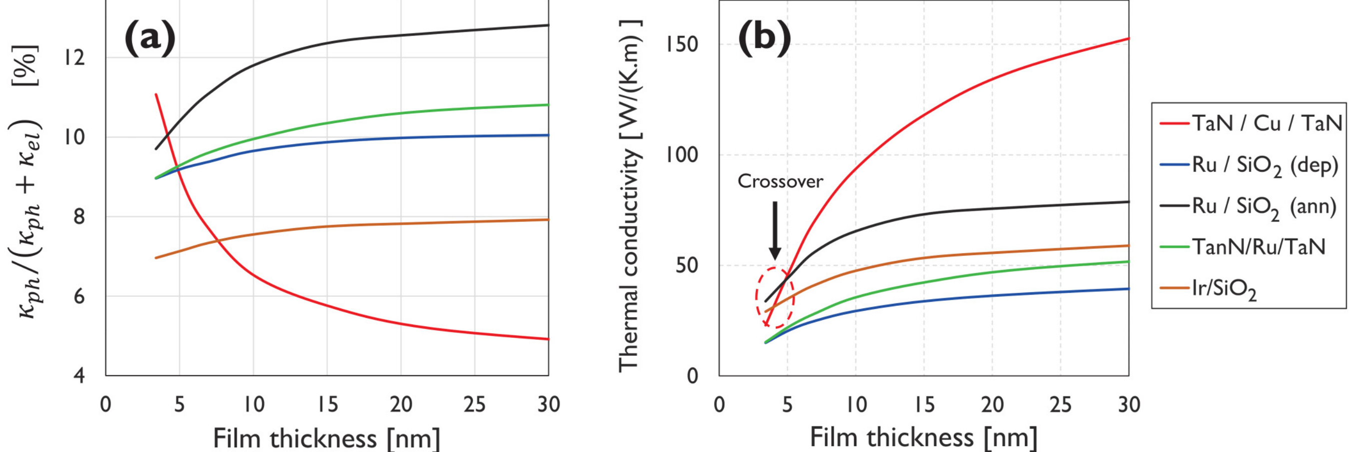


FIG. 12. Thickness-dependent thermal conductivity: (a) Phonon-dominated regime. (b) Total thermal conductivity, including contributions of both phonons and electrons.

model allows for the separation of phonon and electron contributions to total thermal conductivity.

As shown in Fig. 12(a), phonon contributions remain below 15% for relevant interconnect dimensions, indicating electron-dominated thermal transport and (approximate) applicability of the Wiedemann–Franz law. Figure 12(b) illustrates the thickness dependence of the thermal conductivity for several metals. Size-dependent thermal conductivity behavior is influenced by an electron mean free path, grain boundary scattering, and surface scattering characteristics.[153,154] The extent to which the Lorenz number is modified in nanoscale metal films and wires is an ongoing area of research. While theory and experiments suggest a possible reduction from bulk values, conclusive evidence is still lacking.[155–159]

IV. ALTERNATIVE METAL SCREENING AND DOWNSELECTION

Due to the complexity and high cost associated with fabricating nanoscale interconnect lines at target dimensions, direct experimental identification of the most auspicious metals among numerous candidates is impractical. Therefore, a simplified procedure needs to be devised to identify and select the most promising candidates based on easily measurable parameters for a wide range of materials. While the specific set of criteria may vary, recent approaches have focused on both nanoscale metal resistivity and reliability.[24,160,161] Further insights into candidate metal properties can be gained through thin-film experiments, which can serve as initial approximations of expected line performance, following the workflow in Fig. 3. Sections IV A–IV D discuss the current state of understanding for elemental, binary, and ternary metals based on this workflow.

A. Elemental metals

Considering the discussions in Secs. II and III, the following three material properties have been identified as representative indicators of the overall performance of metals in scaled interconnects.

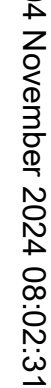
(i) the bulk resistivity, ρ_0;
(ii) the mean free path of the charge carriers λ or, alternatively, the product of the bulk resistivity and the mean free path of the charge carriers, $\rho_0 \times \lambda$; and
(iii) the cohesive energy or, alternatively, the melting temperature.

The first two indicators represent the potential for low resistivity at small dimensions, as discussed in Sec. II. The third parameter can be considered an indicator for electromigration resistance and barrierless reliability, as more refractory metals generally exhibit better performance (see Sec. III).

Values for the first indicator (i) can be found in the literature. While *ab initio* calculations of ρ_0 are feasible, they are computationally intensive and unsuitable for screening a large number of metals. Similarly, calculating the mean free path λ is resource-intensive. However, the product $\rho_0 \times \lambda$ (or the related transport tensor components) can be obtained relatively easily from *ab initio* calculations, as explained in Sec. II C. The third proxy can be either obtained from the literature (melting point) or calculated (cohesive energy). A strong correlation between melting points and cohesive energies has been observed [Fig. 13(a)], justifying their interchangeable use.[160,161]

In practice, the product of bulk resistivity and mean free path, $\rho_0 \times \lambda$, has been preferred as a figure of merit for metals. However, it is essential to consider parameter (i), the bulk resistivity ρ_0, in conjunction with $\rho_0 \times \lambda$. While this is straightforward for elemental metals, it can be challenging for binary and ternary metals due to limited knowledge of their fundamental properties.

The primary limitation of using the $\rho_0 \times \lambda$ figure of merit alone is the inherent correlation between ρ_0 and λ: short mean free paths (short relaxation times) lead to high resistivities, as evident from Eq. (3). Figure 13(b) demonstrates this relationship by plotting the mean free path deduced from the $\rho_0 \times \lambda$ product against bulk resistivity ρ_0 for various elemental metals. As shown in


04 November 2024 08:02:31

© Author(s) 2024

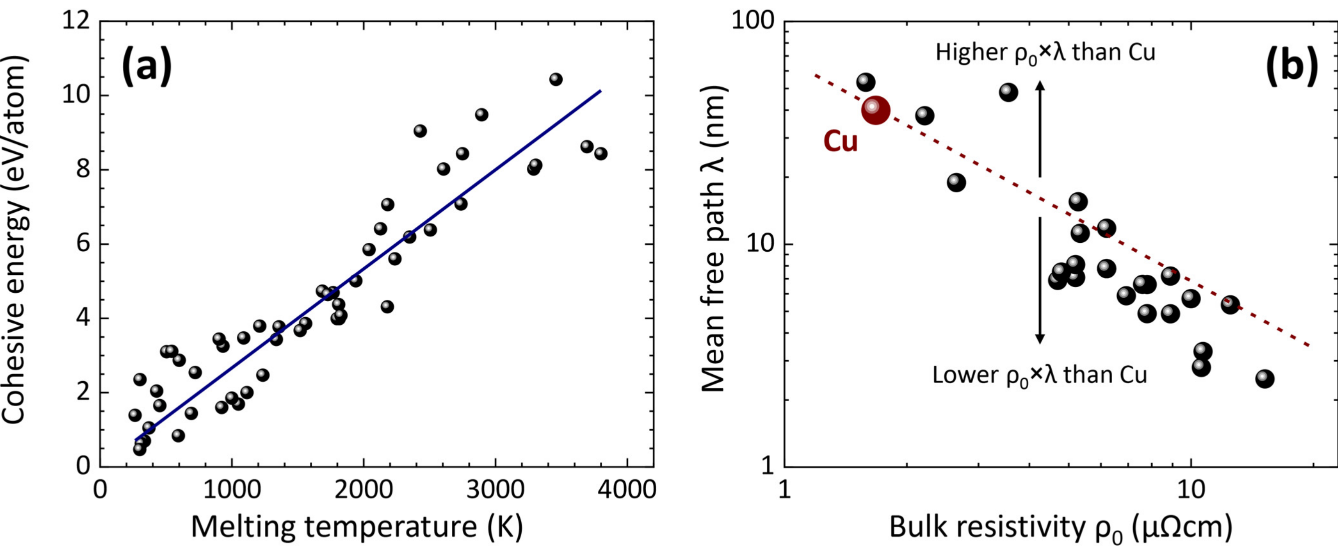


FIG. 13. (a) Relationship between calculated cohesive energy and melting temperature for various elements. (b) Comparison of calculated mean free path λ from the $\rho_0 \times \lambda$ product and experimental resistivities ρ_0 for elemental metals with resistivities below $20\,\mu\Omega$ cm. Cu is highlighted for reference, with the dotted line representing its expected trend for the Cu $\rho_0 \times \lambda = 6.8 \times 10^{-16}\,\Omega$ m.

Fig. 14, a short λ can result in a less pronounced thickness-dependent resistivity compared to Cu, leading to a resistivity crossover at a finite dimension. However, even with a constant $\rho_0 \times \lambda$, a lower bulk resistivity ρ_0 in an alternative metal is still advantageous, as it typically results in a crossover with Cu resistivity at larger dimensions compared to metals with higher ρ_0 (see Fig. 14). While metals with the smallest λ may eventually exhibit the lowest resistivity, the crossover with Cu resistivity might occur at dimensions that are not practical for interconnect applications.

The proposed indicators can be applied to all metallic elements in the periodic table. Using the $\rho_0 \times \lambda$ product of Cu

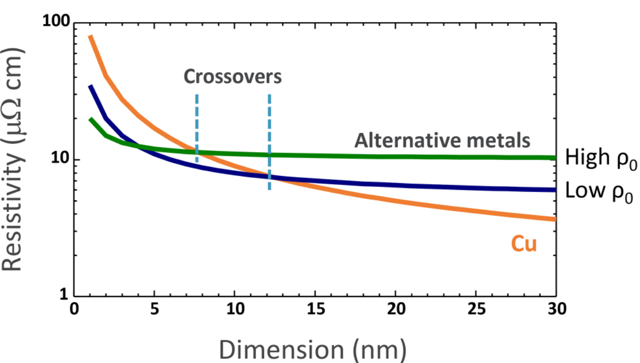


FIG. 14. Resistivity scaling trends: metals with small mean free paths λ may have comparable or lower resistivity than Cu at reduced dimensions. The crossover dimension depends, however, on the bulk resistivity ρ_0 for a constant $\rho_0 \times \lambda$ product.

($\rho_0 \times \lambda = 6.8 \times 10^{-16}\,\Omega$ m), a bulk resistivity of $10\,\mu\Omega$ cm, and the melting point of Cu (1358 K) as cutoff values, the most promising elemental metals can be identified, as shown in Table II. For reference, the properties of Cu are also included. The list includes several transition metals, among them Pt-group metals, such as Ru, Rh, and Ir.

The limited number of promising elements allows for experimental thin-film studies on all candidates, following the workflow outlined in Fig. 3. Figure 15 illustrates the thickness-dependent resistivity of various elemental metal thin films. As expected due to its long mean free path, Cu exhibits a rapid increase in resistivity with decreasing thickness, particularly below 10 nm. In contrast, many alternative elemental metals demonstrate a much less pronounced increase, resulting in comparable or even lower thin-film resistivities at thicknesses below 5–10 nm, depending on the metal. Notably, several Pt-group metals, including Rh, Ir, and Ru, exhibit low resistivities, making them promising candidates for future interconnect applications. Resistivity modeling[70] has confirmed that the weaker film thickness dependence and ultimately lower thin-film resistance compared to Cu can indeed be attributed to shorter mean free paths.

Another promising metal candidate is Mo,[24,31,69,101,165] which, despite exhibiting slightly higher thin-film resistivity, offers several advantages for interconnect integration and is significantly more cost-effective than the expensive Pt-group metals. Consequently, Mo has emerged as a potential candidate for both logic and memory interconnects.[101,166–168]

A metal-spacer-defined metal-etch short-loop vehicle, developed at imec, has provided additional insights into the resistivity of ultrasmall nanowires and expected line resistance scaling. This vehicle enables the fabrication of nanowires with cross-sectional

04 November 2024 08:02:31

© Author(s) 2024

TABLE II. Properties of prospective alternative metals (and Cu for reference): crystal structure, bulk resistivity ρ_0, calculated $\rho_0 \times \lambda$ figure of merit (see Sec. II C), mean free path λ, melting temperature, and cohesive energy.[69,70,162,163]

	Crystal structure	Bulk resistivity ρ_0 ($\mu\Omega$ cm)	$\rho_0 \times \lambda$ 10^{-16} Ω m	Mean free path λ (nm)	Melting temp. (K)	Cohesive energy (eV)
Cu	fcc	1.68	6.8	40.7	1358	3.8
Co	hcp	zz, ∥ 5.1	4.8	9.4	1768	4.7
		($xx = yy$, ⊥) 9.1	7.5	8.2		
Ni	fcc	6.93	4.1	5.9	1728	4.6
Mo	bcc	5.3	5.8	10.9	2895	9.5
Ru	hcp	zz, ∥ 5.7	3.8	6.7	2606	8.0
		($xx = yy$, ⊥) 7.4	5.1	6.9		
Rh	fcc	4.7	3.2	6.8	2236	5.6
Ir	fcc	5.0	3.8	7.5	2719	7.1

areas below 100 nm^2.[169–172] The results in Fig. 16 demonstrate that Ir interconnects exhibit superior resistivity scaling compared to state-of-the-art Cu damascene interconnects, while Ru and Co (to a lesser extent) show similar resistivities for sufficiently narrow lines. These results confirm the potential of these materials as alternatives to Cu for interconnect metallization. It is noteworthy that, despite comparable resistivities, Ru can offer significantly better line resistance than Cu when integrated without barriers and liners due to its larger conducting volume. This aspect will be discussed further in Sec. V.

Beyond thin-film and short-loop nanowire resistivity evaluations, selected alternative metals have been integrated into scaled interconnect lines to assess their line resistance scalability as well as their reliability, particularly with regard to the need for barrier layers. Specific results are now available for Co, Ru, and Mo.

Co metallization has been the subject of extensive recent research and has been integrated into commercial high-volume circuit manufacturing.[174–176] However, Co migrates into surrounding low-κ dielectrics, requiring a barrier layer (typically TiN) analogous to Cu.[176] In advanced technology nodes with ultrathin low-κ films, maintaining hydrophobic interfaces and continuous thick barriers are, however, crucial to prevent metal drift, posing significant challenges to the integration and scalability of Co metallization in advanced interconnects.[177,178]

In contrast to Co, Mo has emerged as a promising candidate for barrierless integration, eliminating the need for an adhesion layer or diffusion barrier on SiO_2, low-κ organosilicate glasses, or SiCO dielectric films. This finding has been corroborated by multiple studies.[179,180]

Ru is another potential barrierless alternative to Cu. Its high cohesive energy and excellent oxidation resistance allow for

04 November 2024 08:02:31

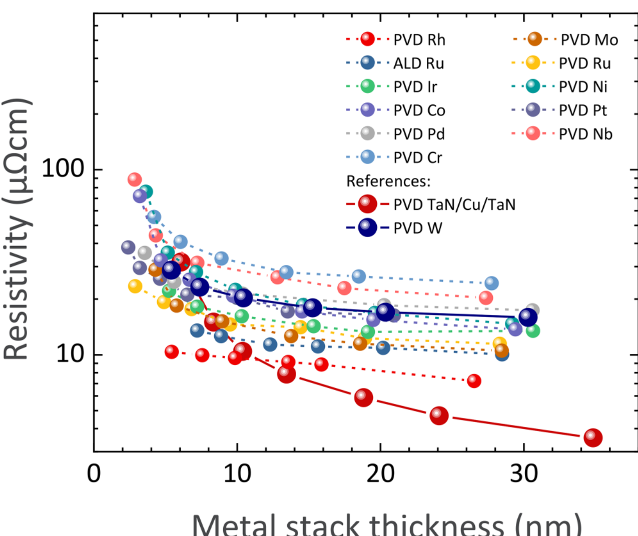


FIG. 15. Experimental resistivity scaling trends for thin-film metals: thin-film resistivities vs metal film (stack) thickness for various potential alternative metals. Pt-group data from Refs. 70 and 164.

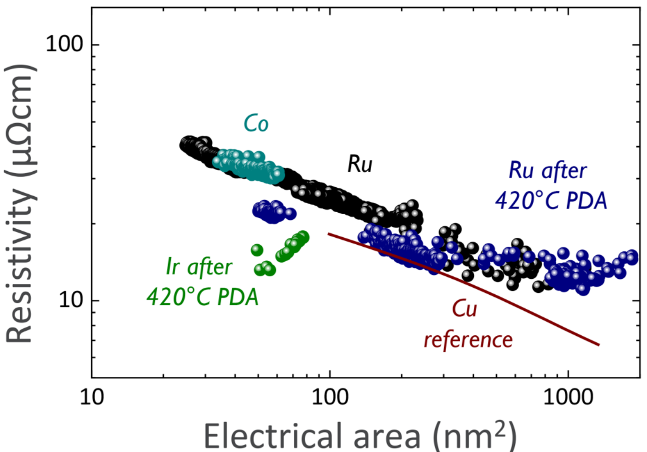


FIG. 16. Resistivity scaling of narrow interconnect lines: comparison of Co, Ru, and Ir data obtained from metallic spacer etched test structures.[28,169–172] Co and Ru shown data are for as-deposited metals, while Ir and additional Ru data were obtained after post-deposition annealing at 420 °C. A reference line is shown for Cu dual-damascene metallization.[173]

© Author(s) 2024

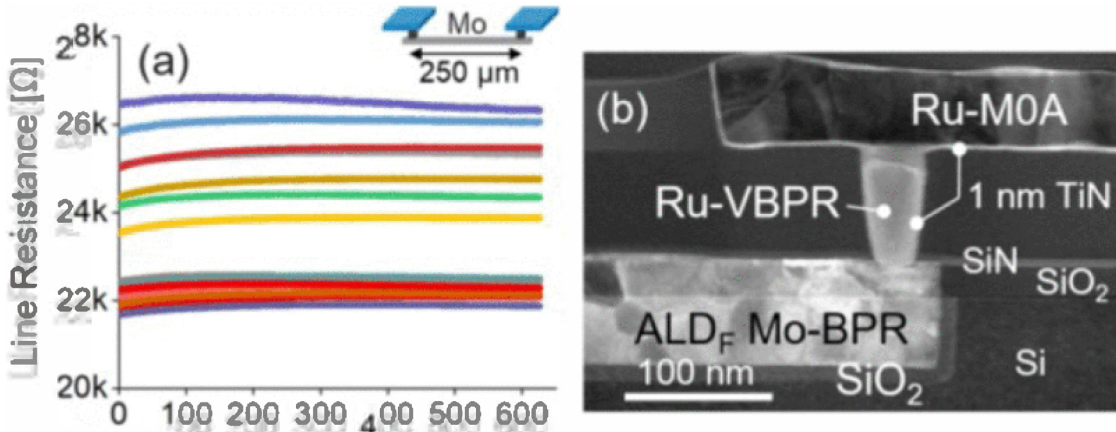


FIG. 17. Electromigration stability of Mo–Ru hybrid interconnects: (a) No failures were observed after more than 600 h testing at 330 °C and 5 MA/cm^2. (b) Cross-sectional transmission-electron micrograph of the tested structure. Reproduced with permission from Gupta *et al.*, in *2022 IEEE International Interconnect Technology Conference*, pp. 58–60 (2022). Copyright 2022 IEEE.

barrierless integration, although a thin adhesion-promoting layer might be necessary. However, this adhesion layer (typically TiN) can be scaled down to a few Å, well below the minimum thickness required for functional diffusion barriers.[181] Further research has confirmed that the reliability of Ru is not compromised when integrated with a 0.3 nm TiN adhesion layer, with no evidence of metal drift. Additionally, Ru combined with dense low-κ dielectrics ($\kappa = 3.0$) has demonstrated a 10-year lifetime based on damascene time-dependent dielectric breakdown results.[167,182]

Both Mo and Ru interconnects exhibit exceptional electromigration performance. As a matter of fact, observing electromigration failures in Mo and Ru interconnects has been challenging due to the extreme temperatures and current densities required.[166,183] Figure 17 illustrates an example of electromigration testing for Mo interconnects, where no failures were observed even after more than 600 h of stressing at 330 °C.[166]

Furthermore, Hu *et al.*[38] demonstrated excellent reliability in 36 nm wide Ru interconnect lines. Additionally, Varela Pedreira *et al.*[183] reported unsuccessful attempts to induce electromigration failures in barrierless 21 nm metal pitch Ru interconnects, even at high current densities exceeding 30 MA/cm^2. In the same study, the authors subjected barrierless Ru lines to even more extreme conditions, driving current densities of 150–200 MA/cm^2, which resulted in significant self-heating (~260 °C). Only under these extreme conditions, void formation was observed at the grain boundaries and the dielectric interface (Fig. 18).[184] Moreover, Beyne *et al.*[185] investigated scaled Ru wires with rough surfaces and no barrier using low-frequency noise measurements. Their findings suggest that the metal/dielectric interface serves as the primary diffusion path.

The results of the combined modeling and experimental screening process for elemental metals, following the workflow outlined in Fig. 3, are summarized in Table II. Six elemental metals have emerged as promising candidates for advanced interconnect metallization: the platinum-group metals Rh, Ru, and Ir, along with the transition metals Ni, Co, and Mo. Among these, Co has already been integrated into local interconnects of commercial CMOS technologies.[174–176] Mo and Ru have garnered the most attention for use in highly scaled lines and vias, due to their demonstrated reliability, even in barrierless configurations. Currently, barrierless Ru metallization combined with airgap structures is considered the leading candidate for logic interconnects with sub-20 nm pitches,[16,18,25,26,186,187] while Mo is also being actively investigated as a viable alternative, particularly for memory applications.[16,18,166–168]

04 November 2024 08:02:31

B. Graphene and hybrid graphene-metal metallization

In addition to conventional metals, graphene has also been proposed as a potential conductor for advanced interconnects.[188–191] Graphene exhibits high carrier mobility and can support large current densities while demonstrating excellent resistance to electromigration.[192,193] However, pristine graphene is a semimetal with a low charge carrier density, resulting in high sheet resistance, which limits its direct applicability in interconnects.[194] To overcome this, multilayer graphene structures and doping are required to reduce resistivity to practical levels.

One effective doping method is intercalation [see Fig. 19(a)], which has demonstrated considerable lowering of thin-film resistivities.[195,196] Notably, $FeCl_3$-intercalated graphene has recently achieved resistivity values comparable to, or even lower than, those of Cu.[197–200] The intercalation process preserves the integrity of the graphene Dirac cone while modulating the Fermi level, thereby increasing the charge carrier concentration. Nevertheless, despite the much improved resistivity in doped intercalated graphene, the high contact resistance when co-integrated with metallic vias remains a significant challenge. Future advancements may arise from exploring alternative n-type intercalation species,[199] but further research is necessary to demonstrate the successful

© Author(s) 2024

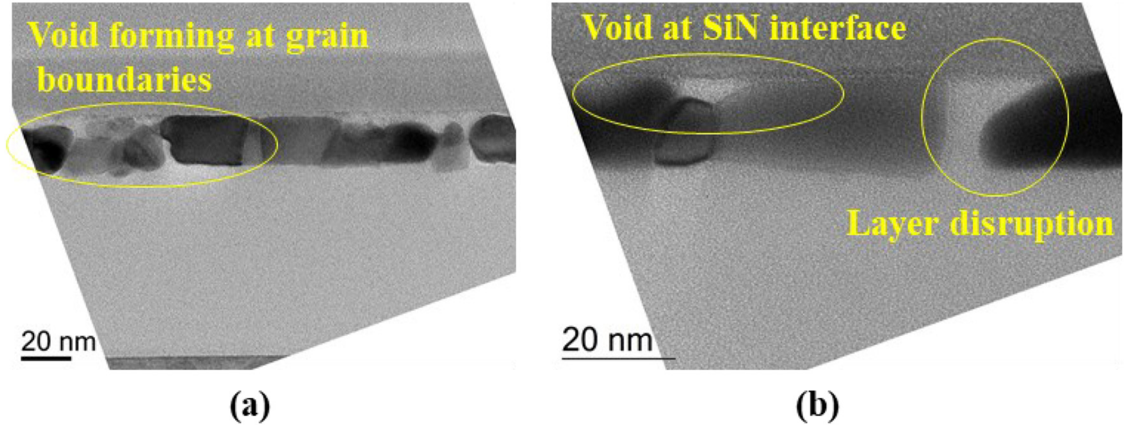


FIG. 18. Transmission-electron micrographs illustrating electromigration-induced void formation in Ru interconnects: voids located (a) at grain boundaries and (b) at the dielectric interface.[184] Reproduced with permission from Varela Pedreira *et al.*, in *2020 IEEE International Reliability Physics Symposium*, pp. 1–7 (2020). Copyright 2020 IEEE.

integration of intercalated multilayer graphene into scaled interconnect architectures.

In addition to intercalated graphene, graphene–metal hybrid composite metallization is another promising approach for interconnects. For instance, studies of Ru thin films capped with multilayer graphene have demonstrated a reduction in both sheet resistance and effective resistivity by approximately 10%–20% compared to uncapped Ru films [see Fig. 19(b)].[201] This improvement has been attributed to a 0.5 eV reduction in the Fermi level, indicative of *p*-type doping in the graphene layer, likely driven by charge transfer from Ru.[202] Similar reductions in sheet and line resistance have been observed in Cu–graphene hybrid metallization schemes as well.[203,204] While many studies have focused on hybrids incorporating single-layer graphene, the use of bilayer or multilayer graphene may yield even greater resistance reductions, although the potential benefits could be limited by charge screening effects and interlayer resistance.

Beyond thin-film studies, the integration of graphene–metal hybrid composite materials presents several challenges. The deposition temperatures required to produce high-quality graphene typically exceed the thermal budget for interconnect processing, which is constrained to around 400 °C. Therefore, the development of low-temperature processes for defect-free graphene deposition is essential.[205] Moreover, when integrated, e.g., in a metal patterning scheme, graphene should ideally be deposited selectively on the sidewalls of patterned interconnect lines to avoid shorts between adjacent lines. Alternatively, graphene integration within damascene interconnect architectures has also been explored,[206] resulting in substantial improvements in electromigration resistance.[207] However, further research is needed to validate the performance benefits of such hybrid systems in realistic scaled interconnect structures.

C. Binary intermetallics

The preceding analysis of elemental metals can be considered exhaustive, encompassing all metals of potential interest. To expand the range of materials of potential interest, recent research has focused increasingly on compound metals. Among binary or ternary metal systems, disordered compounds (alloys) typically exhibit high resistivities due to strong alloy scattering (see Sec. II B). In contrast, numerous ordered intermetallic systems have demonstrated experimentally low resistivities, typically within a specific narrow composition range.[108]

Figure 6 illustrates a well-known example of the Au–Cu system,[107] which includes the intermetallics $AuCu_3$ and AuCu. The figure shows that the resistivities of these intermetallics can be significantly lower than those of random alloys within the same material system and may even approach the resistivities of the constituent elemental metals.

To benchmark and downselect binary intermetallics, the criteria discussed for elemental metals in Sec. IV A can be applied equally. However, a comprehensive benchmarking and downselection process, similar to that conducted for elemental metals, remains beyond reach due to the vast number of potential intermetallic compounds and the limited available data for many of them. Nevertheless, the $\rho_0 \times \lambda$ figure of merit can be calculated for selected intermetallics using *ab initio* methods, as described in Sec. II C. It is important to note that many intermetallics possess non-cubic crystal structures, often requiring tensor formulations. Melting points can generally be found in the literature, such as, e.g., binary phase diagrams, or replaced by calculated cohesive energies when not readily available.

Thus far, *ab initio* screening studies have identified numerous binary intermetallics with low $\rho_0 \times \lambda$ values and cohesive energies exceeding those of Cu (Fig. 20); however, only few surpass Ru. A significant obstacle in evaluating intermetallics is the frequent absence of accurate reported bulk resistivities ρ_0. As a result, a downselection process as comprehensive as that for elemental metals is not readily achievable.

Experimental investigations have primarily focused on several aluminide intermetallics due to their low bulk resistivities (below

04 November 2024 08:02:31

© Author(s) 2024

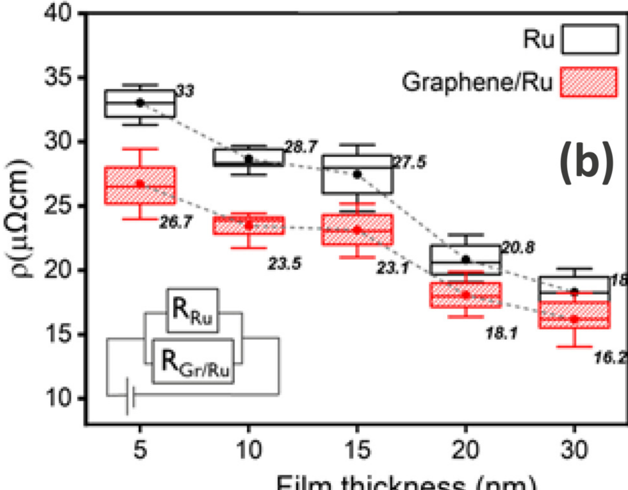


FIG. 19. (a) Cross-sectional transmission-electron micrograph and energy-dispersive x-ray spectroscopy chemical mapping of $FeCl_3$-intercalated graphene.[199] Reproduced with permission from Li *et al.*, in *2023 IEEE International Electron Devices Meeting*, pp. 1–4 (2023). Copyright 2020 IEEE. (b) Resistivity measurements of bare and graphene-capped Ru interconnects for varying Ru thicknesses.[201] Reproduced with permission from Achra *et al.*, Carbon **183**, 999 (2021). Copyright 2021 Elsevier.

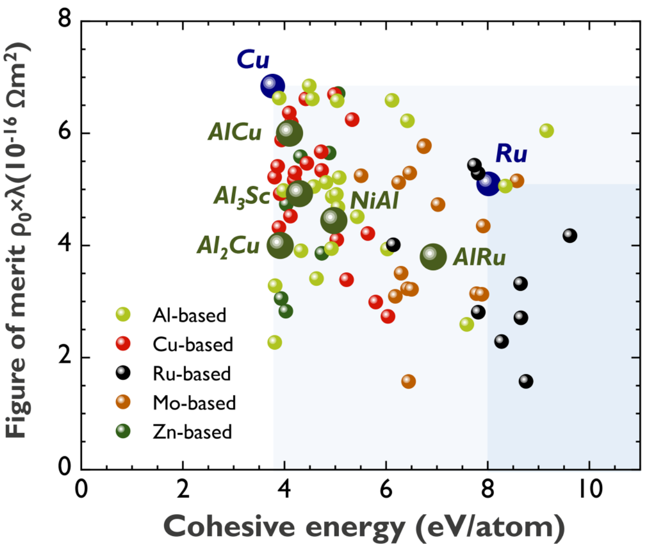


FIG. 20. *Ab initio* screening of binary intermetallics: Calculated $\rho_0 \times \lambda$ product vs cohesive energy. Several Al-based intermetallics, highlighted by larger dots, show promising properties based on the screening criteria described in the text. Cu and Ru are added as reference.

$10\,\mu\Omega$ cm), higher melting points compared to Cu, and notable oxidation resistance.[208] Among the most promising candidates are NiAl, AlCu, Al_2Cu, AlRu, and Al_3Sc. The properties of these aluminide intermetallics are summarized in Table III and can be directly compared to those of the promising elemental metals listed in Table II. For these aluminides, experimental studies have demonstrated low resistivities,[209,210] although this has predominantly been observed for relatively thick films with thicknesses $\gg$10 nm.

Among the most promising aluminide intermetallics, NiAl has emerged as the most extensively studied compound.[209,211–214] In physical vapor-deposited films on 300 mm Si substrates, a

04 November 2024 08:02:31

TABLE III. Properties of prospective intermetallics as alternative metals, including Cu as a reference: crystal structure, bulk resistivity, calculated $\rho_0 \times \lambda$ figure of merit (see Sec. II C), deduced mean free path λ, melting temperature, and calculated cohesive energy of various intermetallics. Note that AlCu and Al_2Cu exhibit transitions to different high-temperature phases between 850 and 900 K, rather than to the liquidus.[223]

	Crystal structure	Bulk resistivity ρ_0 ($\mu\Omega$ cm)	$\rho_0 \times \lambda$ 10^{-16} Ω m	Mean free path λ (nm)	Melting temp. (K)	Cohesive energy (eV)
Cu	fcc	1.68	6.8	40.7	1358	3.8
AlNi[211]	$Pm\bar{3}m$ (B2)	5.5	4.4	8	1910	5.0
AlRu[221]	$Pm\bar{3}m$ (B2)	~10	3.8	~4	2250	6.9
AlCu[217]	C2/m	8	6.0	7.5	N/A	4.1
Al_2Cu[210]	$Fm\bar{3}m$	6.5	4.0	5.5	N/A	3.9
Al_3Sc[220]	$Pm\bar{3}m$ ($L1_2$)	7	4.9	7	1280	4.3
Cu_2Mg[110]	$Fd\bar{3}m$	5.7	9.6	22	1073	2.9
CuTi[224]	P4/nmm	19.5	3.4	12.5	1260	4.3

© Author(s) 2024

resistivity of 13.9 $\mu\Omega$ cm was achieved at a film thickness of 56 nm after post-deposition annealing at 600 °C.[209] This resistivity can be further reduced by depositing NiAl at an elevated temperature of 420 °C, followed by an *in situ* Si capping layer to prevent surface oxidation. Under these conditions, a resistivity of 18 $\mu\Omega$ cm was obtained for a 22 nm thick film.[213] To achieve even lower resistivities at reduced thicknesses, epitaxial NiAl films on Ge (100) have been explored, resulting in a resistivity as low as 11.5 $\mu\Omega$ cm for a 7.7 nm thick film.[215] However, integrating such epitaxial layers into scalable and manufacturable interconnects remains a substantial challenge.

AlCu and Al_2Cu films[210,212,216–218] with thicknesses around 10 nm have demonstrated resistivities below 20 $\mu\Omega$ cm, and below 10 $\mu\Omega$ cm for films around 30 nm in thickness, after post-deposition annealing at 500 °C. The resistivity of Al_2Cu is lower than that of Ru for film thicknesses of 10 nm and above, while both AlCu and Al_2Cu outperform Mo across the entire studied thickness range from 5 to 30 nm. Additionally, these compounds exhibit resistivities comparable to TaN/Cu/TaN for thicknesses below 8 nm. Al_2Cu also displays excellent gap-filling capabilities and promising reliability metrics in time-dependent dielectric breakdown, electromigration, and bias temperature stress tests.[219] However, further investigation is required to fully validate the potential of AlCu and Al_2Cu for advanced interconnects with high reliability.

A resistivity of 12.6 $\mu\Omega$ cm has been reported for a 24 nm Al_3Sc thin film following post-deposition annealing at 500 °C.[220] The resistivity was limited by a combination of grain boundary scattering and point defect (alloy) scattering, which presents significant challenges for further improvements. AlRu has also been identified as a potential candidate to replace Cu; however, experimental resistivities for AlRu have remained comparatively high thus far compared to those of the other aluminides discussed here, primarily due to challenges in producing highly ordered films with large grains.[221]

For Cu_2Mg, a resistivity of 25.5 $\mu\Omega$ cm has been reported for a 5 nm thick film, along with excellent gap-filling performance achieved via sputtering reflow. However, a thick MgO layer is formed within the underlying SiO_2 due to interfacial reactions between Cu_2Mg and SiO_2. This interfacial reaction raises significant concerns regarding the feasibility of integrating Cu_2Mg into scaled interconnects, where (near-)zero interface formation is essential to achieve low-resistance lines, casting doubt on its suitability for such applications.[222]

In contrast to elemental metals, binary intermetallics present several additional challenges, including crystalline order and the minimization of point defect densities, precise control of composition and its uniformity, the formation of secondary phases, agglomeration, (interface) reactivity, and nonstoichiometric surface oxidation, as exemplified in Fig. 21. A primary challenge lies in controlling the composition of binary intermetallics, as reported for the $Al_{1-x}Ni_x$ and Al_xSc_{1-x} systems.[211,220] As shown in Fig. 22(a), the resistivity of Al_xNi_{1-x} exhibits a pronounced minimum at the stoichiometric composition of $Al_{0.50}Ni_{0.50}$. A similar observation for Al_xSc_{1-x} is depicted in Fig. 22(b).

As discussed in Sec. II B, the increase in resistivity can be attributed to the generation of nonstoichiometric substitutional or vacancy point defects, which introduce strong disorder scattering. The experimental findings indicate that compositional control at a level of better than 1 at. % over the entire wafer is essential to achieve low and uniform resistivities, a demanding requirement for high-volume manufacturing. Furthermore, in both cases shown in Fig. 22, low resistivities were only observed after high-temperature post-deposition annealing, likely due to thermally activated ordering (point defect reduction) and grain growth. Consequently, the compatibility of these annealing steps with the thermal budget of the device fabrication process must be carefully evaluated.

As a further illustration of the challenges associated with binary intermetallics, Fig. 23 presents a cross-sectional transmission-electron micrograph and the corresponding energy-dispersive x-ray spectroscopy chemical analysis of an NiAl film after air exposure. The chemical analysis reveals the presence of a native surface oxide, which deviates from the bulk NiAl stoichiometry, exhibiting a composition close to pure Al_2O_3.[209] This phenomenon can be attributed to element-specific surface processes, specifically metal outdiffusion governing the formation of the native oxide. This can significantly complicate compositional control, particularly for ultrathin films.[225]

The tendency of forming nonstoichiometric native surface oxides has been observed in various aluminide intermetallics, although the specific oxide compositions may vary depending on the material system.[33,218,220] Therefore, *in situ* surface passivation techniques may be essential for the successful integration of (aluminide) intermetallics into scaled interconnects, both after deposition and potentially after patterning also.

D. Ternary compounds

Beyond binary intermetallics, several ternary compounds have been explored for advanced interconnect metallization. Given the vast combinatorial space of ternary intermetallics and the limited knowledge of their properties, a comprehensive screening approach, akin to that employed for elemental or binary systems, is computationally prohibitive. Consequently, research has, thus far, focused on specific material classes, with particular attention given to MAX phases.[28,226] MAX phases are layered hexagonal carbide or nitride metallic ceramics, described by the generic formula $M_{n+1}AX_n$ [Fig. 24(a)], where $1 \leq n \leq 3$; M is an early transition metal, A is an A-group element, and X is either C or N.[227–232]

MAX phases typically exhibit significant thermal and electrical conductivities, along with high melting points. Certain MAX compounds, such as Cr_2AlC and V_2AlC, demonstrate bulk in-plane resistivities on the order of 10 $\mu\Omega$ cm at room temperature [Fig. 24(b)].[233] An *ab initio* screening study has identified low $\rho_0 \times \lambda$ products (see Sec. II C) for several MAX phases, confirming their potential for scaled interconnect metallization.[234]

Another material system of potential interest are metallic delafossite oxides, particularly $PdCoO_2$ and $PtCoO_2$.[235] These layered hexagonal compounds [see Fig. 24(c)] exhibit ultralow bulk resistivities comparable to that of Al,[235–238] along with exceptionally long mean free paths.[239] Recent experimental studies have reported thin films with thicknesses within the target range for interconnect applications.[240–243] However, further experimental investigation is required to thoroughly assess the scalability and suitability of these delafossite oxides for interconnect line integration.

04 November 2024 08:02:31

© Author(s) 2024

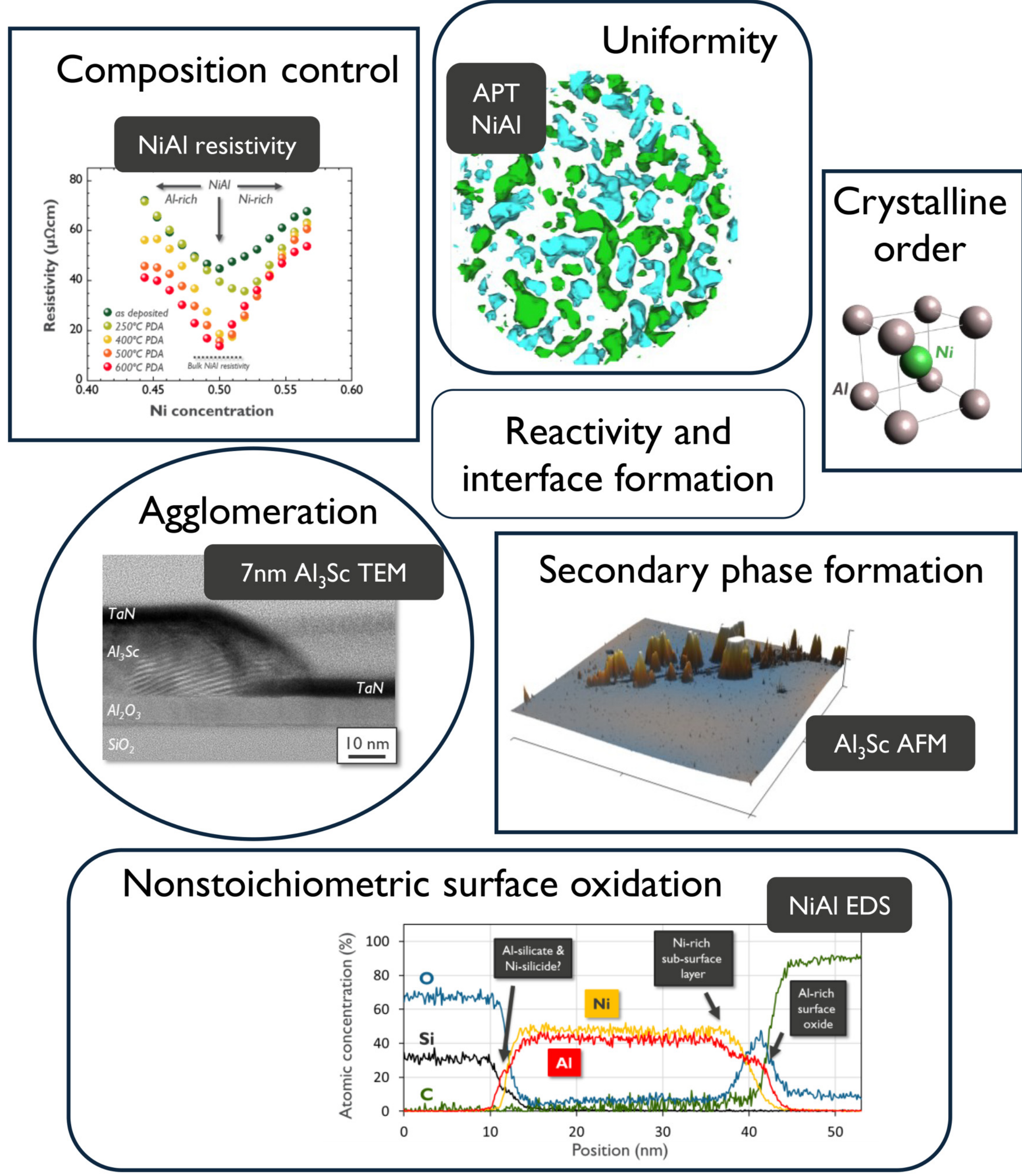
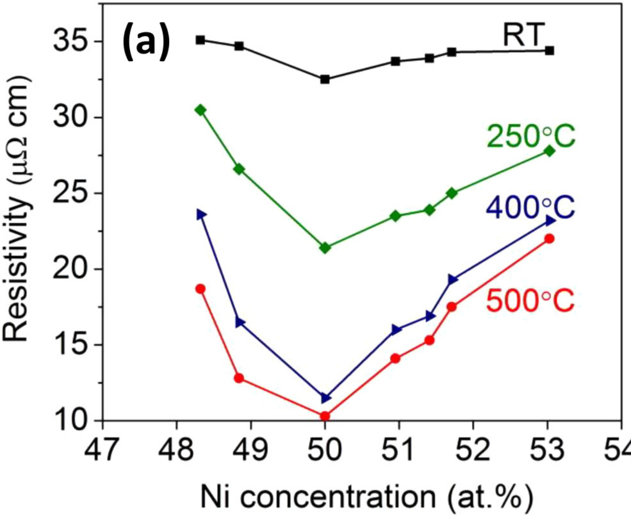


FIG. 21. Common challenges for obtaining low resistivities in intermetallic compounds: composition dependence of resistivity, nanoscale composition uniformity, secondary phase formation, crystalline order, reactivity and interface formation, agglomeration, as well as nonstoichiometric surface oxidation.

Ternary compounds, like their binary counterparts, are likely to encounter additional challenges in terms of composition control and processing. Furthermore, both MAX phases and delafossite compounds are highly anisotropic conductors, exhibiting low resistivity in the in-plane directions. While this anisotropy could be advantageous by suppressing surface scattering at top surfaces or interfaces (see Sec. II A 3),[104,105] achieving the desired crystallographic orientation becomes critical. Specifically, fully (001)-textured films without misoriented grains must be realized to harness these properties. Therefore, extensive experimental

04 November 2024 08:02:31

© Author(s) 2024



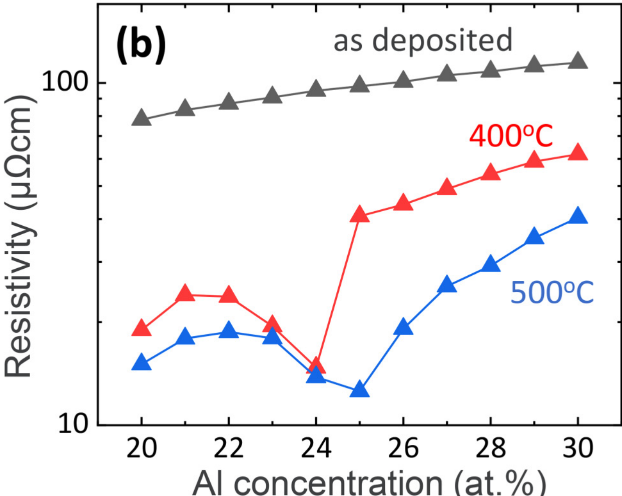


FIG. 22. (a) Resistivity of Ni_xAl_{1-x} vs. Ni concentration around stoichiometric NiAl.[211] Reproduced with permission from Chen *et al.*, Appl. Phys. Lett. **113**, 183503 (2018). Copyright 2018 AIP Publishing LLC. (b) Resistivity of Al_xSc_{1-x} vs Al concentration around stoichiometric Al_3Sc.[212,220] In both cases, a pronounced resistivity minimum is observed at the stoichiometric composition.

validation is still required to confirm the viability of these ternary metals for interconnect applications.

E. Beyond binary and ternary intermetallics: One-dimensional metals and topological Weyl semimetals

As discussed in Sec. II A 3, anisotropic resistivity and reduced dimensionality can mitigate surface scattering. One-dimensional conductors, in particular, have been proposed as ideal interconnect materials due to their ability to suppress surface scattering at the top, bottom, and sidewalls of interconnect lines.[105] Unlike two-dimensional layered metals (MAX, delafossite oxides), which exhibit low resistivity in two directions but higher resistivity in the perpendicular direction, one-dimensional metals possess a single direction of low resistivity with significantly increased resistivity in the two orthogonal directions.

The suppression of surface scattering in one-dimensional metals can be incorporated into both resistivity simulations[72] and material benchmarking (see Sec. II D).[105] Similar to the $\rho_0 \times \lambda$ tensor introduced in Sec. II C, a figure of merit for nanowires has been defined in Eq. (14) that accounts for the reduction in surface scattering.[72,105] Potential one-dimensional metal candidates include binary hexagonal intermetallics (e.g., CoSn, OsRu), orthorhombic intermetallics (e.g., VPt_2, $MoNi_2$), and ternary borides (e.g., YCo_3B_2).[105]

However, it should be noted that no thin-film results have yet unambiguously demonstrated the suppression of surface scattering in such materials. Furthermore, integrating such materials into interconnects will necessitate single crystals with the low resistivity axis aligned with the interconnect wires. Currently, no viable manufacturing pathways exist for producing such interconnects, indicating that significant research and development are still needed to realize the potential of these materials.

Additionally, topological semimetals, which encompass both Weyl and multifold-fermion semimetals, have recently emerged as promising candidates for future interconnect technologies. Weyl semimetals are distinguished by their unique electronic structure, characterized by linear band dispersion, degenerate Weyl nodes, and topologically protected surface states.[244] These surface states exhibit high conductivity and are robust against disorder. Examples of Weyl semimetals include TaAs,[245] TaP, NbAs,[246] MoP,[247] and NbP, while CoSi,[248,249] RhSi, and AlPt represent multifold-fermion semimetals.

In the case of CoSi, calculations have shown that the effective resistivity (resistance normalized by the cross-sectional area) decreases as wire dimensions are reduced, even in the presence of grain boundaries, due to the dominance of surface-driven transport channels.[250] Experimental evidence for the topological semimetal NbAs suggests that indeed the effective resistivity can decrease as the cross-sectional area decreases,[246] although further investigations are required to confirm these findings in interconnect-relevant structures. Similar to one-dimensional metals, topological semimetals will require the fabrication of single-crystal (epitaxial) wires. Furthermore, the reliability of interconnects based on topological semimetals remains uncertain, necessitating further fundamental research to evaluate their viability for scalable interconnect applications.

04 November 2024 08:02:31

V. RESISTANCE MODELING FOR NANOSCALE INTERCONNECT LINES

The resistivity trends presented in Fig. 16 can be leveraged to develop calibrated models for interconnect line resistance, enabling benchmarking against (projected) Cu line resistance values at scaled dimensions. A simplified geometrical model for Ru and Ir interconnects, defined by a width w, height $h = w \times AR$, and aspect ratio (AR), has recently been introduced based on the data from Fig. 16.[28] To project barrierless line resistance as a function of

© Author(s) 2024

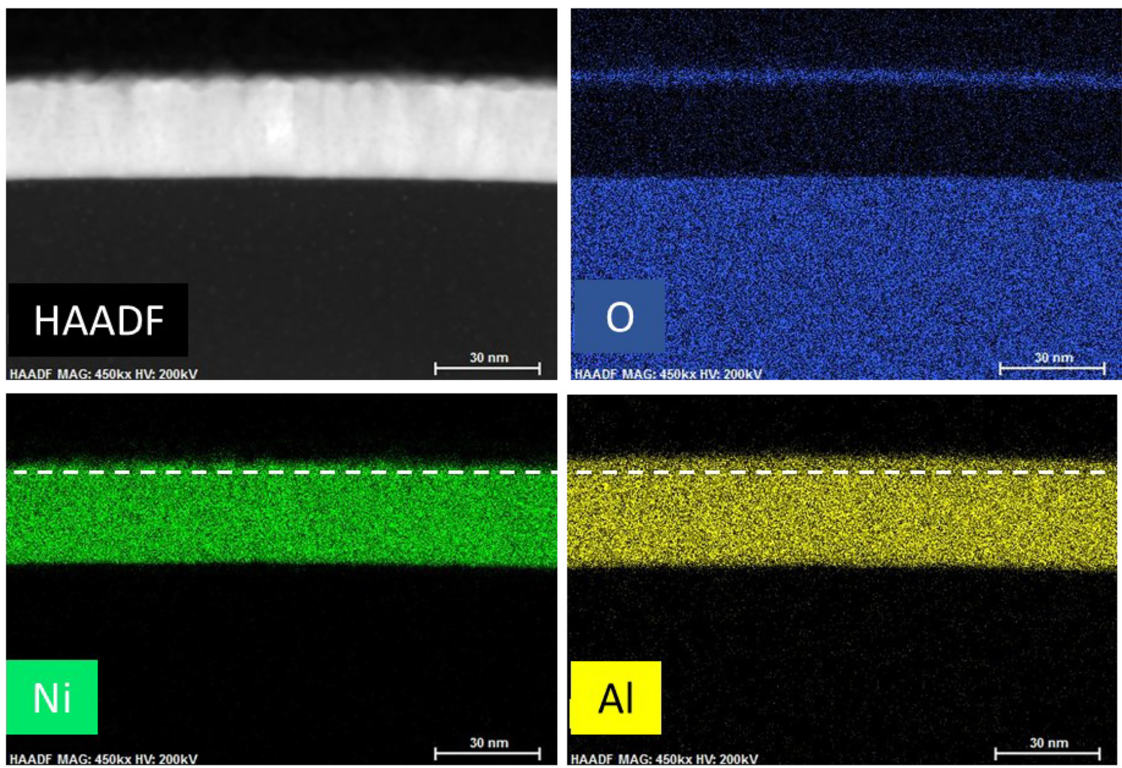


FIG. 23. High-angle annular dark field transmission-electron micrograph as well as O, Al, and Ni energy-dispersive x-ray spectroscopy chemical maps of a 30 nm thick NiAl film (on SiO_2/Si) after air exposure. The chemical image analysis indicates the presence of an AlO_x surface oxide.

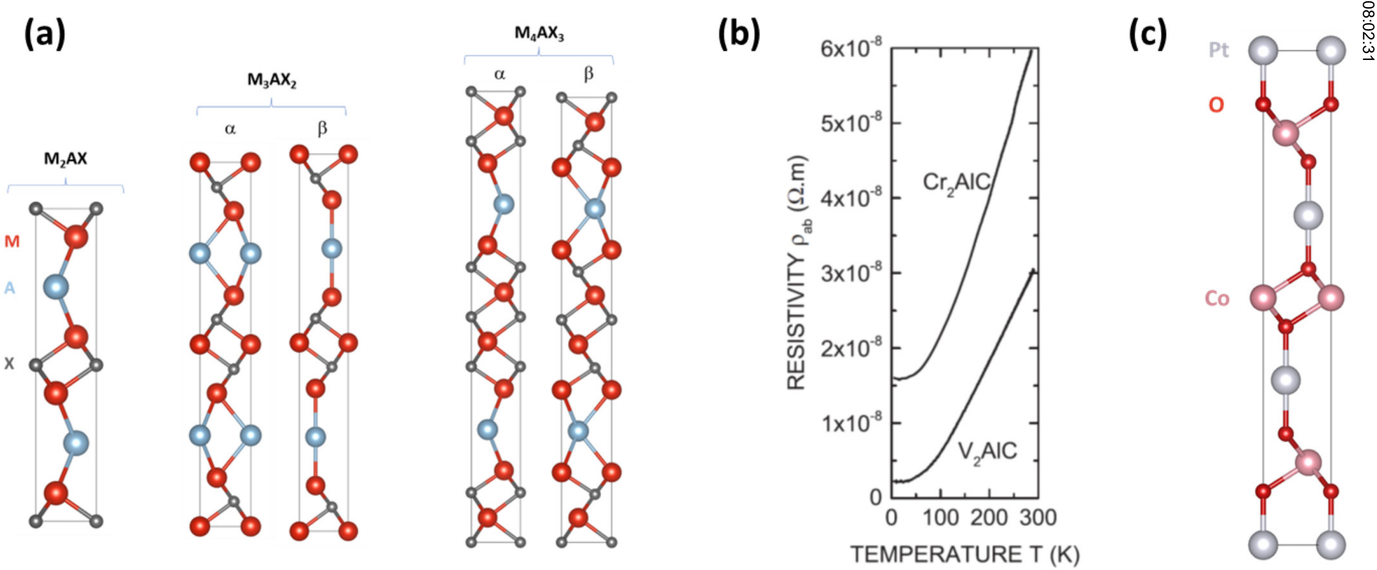


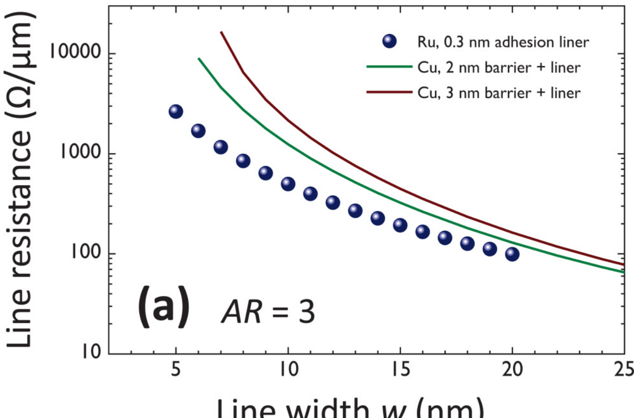
FIG. 24. (a) Crystal structure of MAX phases, $M_{n+1}AX_n$, where M is an early transition metal, A is an A-group element, X is C or N, and n is an integer between 1 and 3. (b) Temperature-dependent in-plane resistivity of Cr_2AlC and V_2AlC single crystals.[233] Reproduced with permission from Ouisse *et al.*, Phys. Rev. B **92**, 045133 (2015). Copyright 2015 American Physical Society. (c) Crystal structure of the delafossite oxide $PtCoO_2$.

04 November 2024 08:02:31

© Author(s) 2024

line width w, resistivity trends as a function of cross-sectional area were derived from the data for Ru (after post-deposition annealing at 420 °C). The Ru metallization scheme also incorporated a 0.3 nm thick adhesion liner.[181] For comparison, Cu resistivities were taken from an established line resistance model at an aspect ratio of 2, characteristic for dual damascene interconnects.[173]

The projected line resistances for Ru and Cu metallization, considering different combined diffusion barrier and liner thicknesses, are shown in Fig. 25 for aspect ratios of 3 [Fig. 25(a)] and 5 [Fig. 25(b)]. The data demonstrate a significant potential for lower line resistances with Ru interconnects compared to Cu, even with scaled barrier and liner layers, particularly at higher aspect ratios. For instance, the model suggests that Ru interconnect lines could achieve a threefold reduction in line resistance over Cu when the total barrier and liner thickness is 2 nm, with a linewidth of $w = 8$ nm and an aspect ratio of 3.



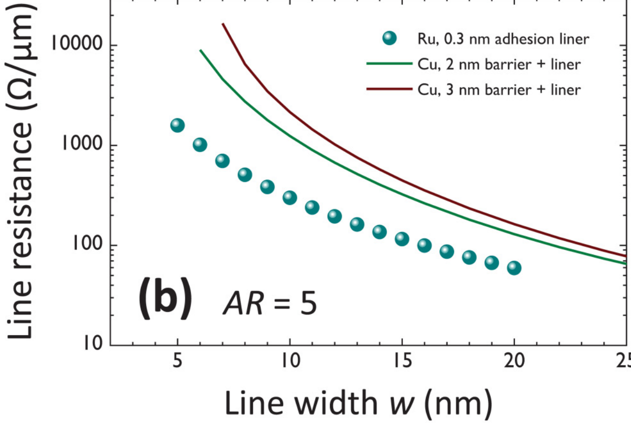


FIG. 25. Projected line resistance for Ru and Cu interconnects with aspect ratios of (a) 3 and (b) 5, respectively. The Ru model includes a 0.3 nm adhesion liner, while the Cu trend lines incorporate barrier and liner layers with aggregate thicknesses of 2 and 3 nm. The data are based on calibrated models for Ru[28] and Cu.[173]

Moreover, these resistance models can provide insights into the mechanisms driving the crossover in line resistance between Cu- and Ru-based interconnects. A quantitative comparison of Ru and Cu resistivities (see Fig. 16) indicates that the scaling advantage of Ru does not arise from a lower resistivity but from the increased conductor volume when the barrier and liner layers required for Cu are replaced by a much thinner adhesion layer. Nevertheless, resistivity scaling remains a crucial factor as high resistivities at low dimensions due to poor resistivity scaling can negate the potential benefits of increased conductor volume. Therefore, barrierless metallization and favorable resistivity scaling must complement each other to realize low line resistances in scaled interconnects.

A second factor contributing to reduced line resistance is an increased aspect ratio.[16] While the aspect ratio is not an intrinsic material property, it is strongly influenced by the integration process. Conventional dual-damascene Cu interconnects (Fig. 2) are limited to aspect ratios of 2 to 3 due to the challenges of Cu filling. However, alternative process schemes, such as semidamascene integration (Fig. 26), can enable higher aspect ratios by combining damascene via filling with direct metal etching. While Cu etching of scaled high-aspect-ratio lines remains difficult, Ru and Mo are much better suited for reactive-ion etching (see Sec. IV C and Table IV). Specifically, Ru lines with aspect ratios up to 6 and metal pitches as small as 18 nm have been demonstrated.[252] As shown in Fig. 25(b), increasing the aspect ratio to 5 can result in a fivefold reduction in line resistance for Ru compared to Cu (at an aspect ratio of 2) with a 2 nm barrier/liner thickness and a linewidth of 8 nm. Therefore, the combination of alternative metals with novel integration schemes offers significant potential for reducing line resistance in scaled interconnects.

VI. MATERIAL CONSIDERATIONS FOR INTERCONNECT PROCESSING

Integrating alternative metals into scaled interconnects often requires the development of novel unit processes and metallization modules within the final stages of the alternative metal workflow depicted in Fig. 3. While a comprehensive review of available process technologies, their maturity, and their limitations is beyond the scope of this Tutorial, we will introduce several topics that become increasingly critical in the development of scaled

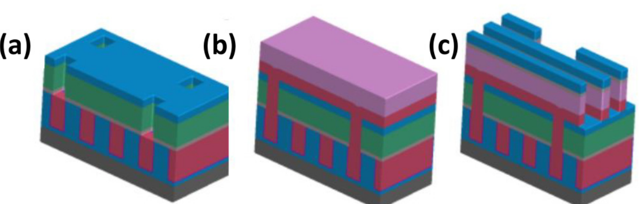


FIG. 26. Schematic representation of the semidamascene interconnect integration process: (a) via patterning in low-κ dielectric (green) using a hardmask (blue), (b) metal filling of the etched vias (red-brown) followed by metal overfill (light purple), and (c) line patterning in the overfilled metal layer (light purple) using a second hardmask (blue).[251]

04 November 2024 08:02:31

© Author(s) 2024

TABLE IV. Summary of process readiness for high-volume manufacturing of selected alternative metals at the time of publication: compatibility of metal process temperatures with logic back-end-of-line (BEOL) thermal budget, maturity of chemical–mechanical polishing, reactive-ion etching, and wet cleaning unit processes, as well as relative extendability of alternative metallization to future technology nodes. +, mature process; o, risk process; and –, research process.

Metal	Logic BEOL thermal budget	Trench filling	Chemical–mechanical polishing	Reactive-ion etching	Wet cleaning	Extendability
Cu	+	+	+	–	+	–
W	+	+	+	+	+	–
Mo	o	o	o	o	o	+
Ru	+	o	o	+	o	+
Ir	+	–	–	–	–	o
Rh	+	–	–	–	–	o
NiAl	+	–	–	–	–	o
$CuAl_x$	+	–	–	–	–	o
Al_3Sc	+	–	–	–	–	o
$PtCoO_2$ (delafossite)	–	–	–	–	–	o
Cr_2AlC (MAX)	–	–	–	–	–	o

interconnect line manufacturing. This section will conclude with a brief evaluation of the current maturity of key unit processes for selected alternative metals.

A. Adhesion and stress

A fundamental property of interconnect metallization is its adhesion to surrounding low-κ dielectrics. Metal–dielectric interfaces often exhibit weaker adhesion compared to metal–metal or dielectric–dielectric interfaces, potentially leading to metal film delamination and catastrophic failure. While deposition conditions impact adhesion, it can be considered a material-dependent property. Noble metals generally exhibit weaker adhesion to dielectrics than base metals due to weaker interfacial bonding. High-quality graphene also suffers from poor adhesion due to weak van der Waals interactions with surrounding dielectrics or metals.

Adhesion can be enhanced by incorporating adhesion liners between the main metal (e.g., a noble metal) and the surrounding dielectrics. However, like diffusion barriers, adhesion liners occupy interconnect volume and typically contribute minimally to conductance. Therefore, minimizing their thickness is crucial. Experimental studies have demonstrated that base metals, such as Mo, exhibit strong adhesion to common dielectrics.[101] This allows for Mo metallization without the need for additional barriers or liners.

In contrast, the more noble metal Ru requires an adhesion liner (e.g., TiN or TaN) due to its weaker adhesion to dielectrics. Nevertheless, studies have shown that the liner thickness can be reduced to as little as 0.3 nm without compromising its effectiveness.[181] This suggests that even non-continuous films can function as adhesion liners and may be more scalable than diffusion barriers. Even more noble metals, such as Ir and Rh, however, require further investigation to ensure adequate adhesion and prevent delamination.

Delamination can be exacerbated by high built-in stress within the metallization stack, further weakening the interface between metals and dielectrics. Additionally, the combination of high compressive stress and capillary forces during filling can lead to nanostructure deformation, such as line wiggling.[253] Stress is not an intrinsic material property but is mainly determined by the deposition method. Physical vapor deposited films often exhibit high (tensile) stress after deposition, which is typically generated during island coalescence at the initial stages of nucleation and growth. However, the overall stress behavior can be complex, in particular during thermal cycling.[83,84,254–257]

For instance, as-deposited PVD Mo films have been observed to have built-in tensile stress as high as 1500 MPa depending on the film thickness.[101] Post-deposition annealing and associated grain growth can significantly modify stress, even leading to compressive stress after cooling within certain temperature ranges.[101,258] While stress management is primarily a topic for deposition process development, it is particularly critical for metals with inherently weak adhesion.

B. Oxidation resistance

During interconnect patterning, certain metal surfaces may be exposed to air or other reactive environments, making chemical inertness, particularly oxidation resistance, a critical consideration. Even self-limiting surface oxidation processes result in the formation of native oxide layers, typically around 2 nm thick, consuming approximately 1 nm of metal.[101] For scaled metal lines with dimensions on the order of 10 nm, surface oxidation must, therefore, be avoided. Noble metals are inherently more chemically inert than base metals and, thus, offer greater resistance to oxidation. While this also leads to weaker adhesion, it renders noble metals more compatible with interconnect process flows.

For compound metals, the situation is even more complex. As discussed in Sec. IV C for NiAl (see Fig. 23), surface oxides of binary metals can be nonstoichiometric, leading to compositional

04 November 2024 08:02:31

© Author(s) 2024

changes in the region immediately beneath the surface oxide.[209,220] In such material systems, controlling the composition of scaled interconnect lines is extremely challenging, and surface oxidation must, thus, be strictly avoided. While *in situ* patterning and passivation or capping can potentially address these issues, they introduce significant process complexity and should be carefully considered during metal selection.

C. Process technology readiness

As mentioned above, a comprehensive review of the state-of-the-art process technology for Cu and alternative metal integration is beyond the scope of this Tutorial. However, from a general perspective, both dual-damascene (Fig. 2) and semidamascene integration routes (Fig. 26) require critical unit processes for manufacturing scaled interconnects. These include metal trench and via filling, typically accomplished through electroplating or chemical vapor deposition. Line definition requires chemical–mechanical polishing (CMP) for dual-damascene and reactive-ion etching (RIE) for semidamascene integration. While Cu is well-suited for dual-damascene integration due to the availability of mature chemical–mechanical polishing processes, its suitability for semidamascene integration is limited by the challenges associated with Cu reactive-ion etching.

For alternative metals, the availability of chemical–mechanical polishing and/or reactive-ion etching processes, in addition to deposition techniques, is, thus, crucial. Ru has demonstrated excellent results with reactive-ion etching, enabling scaled lines with high aspect ratios and precise sidewall control.[187,251,252] However, for many other alternative metals, both chemical–mechanical polishing and reactive-ion etching remain underdeveloped. Rh, for example, offers low resistivity, a high melting point, and potential for high electromigration resistance.[260] Adhesion engineering remains, however, a challenge, particularly when minimizing the thickness of adhesion liners to avoid reducing conductor volumes. Rh can be electroplated,[261] and the filling of sub-40 nm wide lines and vias with high aspect ratios has been demonstrated (Fig. 27).[259] Yet, dual-damascene integration requires chemical–mechanical polishing, which is not well-established for Rh and requires aggressive abrasives and oxidizers.[259] Moreover, the lack of manufacturable reactive-ion etching processes for Rh hinders semidamascene integration, making it a significant obstacle to realizing the potential of Rh metallization in high-volume manufacturing CMOS circuits.

Table IV provides a summary of the process readiness for selected elemental metals, as well as binary and ternary compounds. The table provides the authors' assessment of the process maturity for each material as of the time of publication: a "+" indicates a mature process suitable for high-volume manufacturing, an "o" signifies the availability of a risk process, and a "−" denotes a process that is currently at the research stage. The table highlights the intricate and lengthy journey required for the successful integration of alternative metals into manufacturable interconnects. Mo and Ru processes appear to be the most mature ones, making them leading candidates for high-volume manufacturing, as already outlined in Sec. IV. In contrast, many critical process steps are still lacking for other metals.

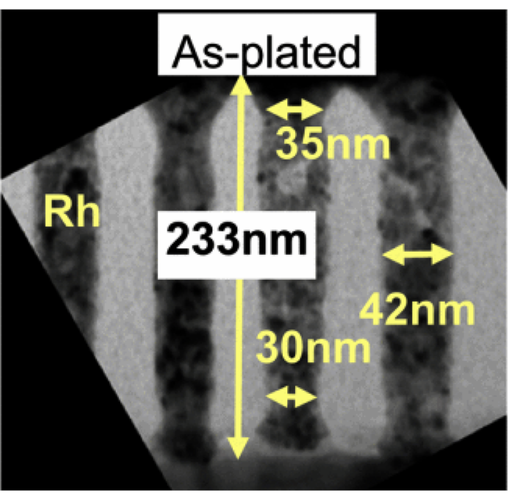


FIG. 27. Cross-sectional transmission-electron micrograph of an Rh-filled interconnect line with a width of <40 nm.[259] Reproduced with permission from Shao *et al.*, 2007 IEEE International Interconnect Technology Conference, pp. 102–104 (2007). Copyright 2007 IEEE.

VII. SUSTAINABILITY OF ALTERNATIVE METALS

Traditionally, the selection of alternative interconnect metals has mainly considered technological, physical, and economic factors. However, recognizing the increasing importance of sustainability, this section introduces a streamlined framework for assessing the sustainability of alternative interconnect metals. This framework incorporates seven sustainability aspects (SAs) and evaluates examples of selected current and emerging interconnect metals (Cu, Al, Ni, Ru, Co, Mo, Ir, Rh). To avoid shifting environmental burdens, a life cycle approach is essential, requiring consideration of the integration method for alternative interconnect metals. Understanding material and energy flows during integration is crucial for assessing overall sustainability. While processes with fewer steps may reduce environmental impact, energy requirements during integration must also be carefully considered. This section discusses these integration considerations and provides a condensed overview of the sustainability assessment framework detailed in Ref. 262.

The proposed sustainability assessment framework for alternative interconnect metals is categorized into seven sustainability aspects (SAs), each with at least one indicator to quantify its impact. SA1 focuses on supply risk, using the Herfindahl–Hirschman index (HHI) to assess market concentration.[263,264] The Herfindahl–Hirschman index values in Table V were extracted from Refs. 265 and 266. SA2 addresses criticality and conflict, considering metals listed as critical raw materials (CRMs) in the US[267] and EU,[268] as well as those on the EU conflict mineral list.[269] SA3 evaluates metal circularity within integrated circuit manufacturing processes and acknowledges the challenges of calculating the site material circularity index (CI).[270] SA4 assesses climate change impact through global warming potential (GWP) values,[271] while

04 November 2024 08:02:31

© Author(s) 2024

TABLE V. Summary table of sustainability aspect (SA) indicators for current and alternative interconnect metals. The volumetric impact values for SA4–SA7 have been quantified based on the cradle-to-gate production of 1 cm^3 of an interconnect metal. The values for such an indicator have been classified as green, amber, or red as defined in Ref. 262.

	Density[274] (kg/m^3)	SA1: HHI[265,266] (0–10000)	SA2 (Refs. 267–269)	SA4 Embedded GWP[271] ($kg\ CO_2/cm^3$)	SA5: WS[262] (m^3/cm^3)	SA6: ADP[273] ($kg\ Sb\ Eq/cm^3$)	SA7 Human Toxicity[271] ($CTUh/cm^3$)	SA7 Particulates[262] (disease incidences/cm^3)
Cu	9.0	1097	Yes/No/No	0.0251	0.02	2.42×10^{-04}	2.42×10^{-06}	5.11×10^{-09}
Ni	8.9	2110	No/Yes/No	0.0579	0.03	1.07×10^{-05}	2.05×10^{-07}	8.27×10^{-08}
Mo	10.0	2266	No/No/No	0.0583	0.02	2.25×10^{-03}	9.20×10^{-06}	2.00×10^{-09}
Al	2.7	3372	Yes/Yes/No	0.0222	0.01	1.13×10^{-10}	1.46×10^{-08}	6.84×10^{-09}
Co	9.0	4876	Yes/Yes/No	0.0739	0.34	4.18×10^{-06}	3.38×10^{-08}	3.12×10^{-08}
Ru	12.4	8718	Yes/Yes/No	26	164	3.34	1.98×10^{4}	…
Rh	12.4	7352	Yes/Yes/No	436	152	2.61×10^{-05}	3.35×10^{-03}	4.75×10^{-05}
Ir	22.4	7986	Yes/Yes/No	198	200	3.14	1.12×10^{-03}	…

SA5 focuses on water scarcity using the EF 3.1 methodology[272] for upstream water use. SA6 examines the impact on natural resources through abiotic resource depletion potential (ADP) values,[273] and SA7 assesses human health impacts using EF 3.1 methodologies, such as "human toxicity cancer and non-cancer" and "particulate matter." These indicators collectively provide a comprehensive evaluation of the sustainability of alternative interconnect metals. For more detailed information on each SA and its associated indicator(s), please refer to Ref. 262.

Table V provides a summary of the sustainability performance of the examined interconnect metals, presenting a nuanced perspective on the seven proposed indicators. The sustainability impacts (SA4–SA7 in Table V) are calculated based on the cradle-to-gate impact to produce 1 cm^3 of metal. This calculation assumes that the volume of the final deposited layer of an interconnect metal is independent of the metal. However, the volume ratio required to achieve the desired final volume deposited should be considered.

Evaluating metal deposition efficiency η_{dep} is essential to determine the actual used volume V_u. Typical deposition processes exhibit a range of η_{dep} values spanning from 1% to 20% for chemical-vapor-based deposition processes[275] but can be much higher for physical vapor processes. Additionally, subtractive integration schemes lead to further material loss determined by the material use efficiency of the integration process η_{int} and influenced by the choice of an interconnect metal. By contrast, damascene integration schemes require the depositions of large overburden before chemical–mechanical polishing, leading also to $\eta_{int} \ll 1$. V_u can be defined as

$$V_u = \frac{V_{IC}}{\eta_{dep}\eta_{int}}, \tag{25}$$

where V_{IC} is the volume of the manufactured interconnect (layer), determined by interconnect dimensions as well as circuit-specific via and line densities.

A more accurate assessment of the environmental impact of the interconnect metal for specific sustainability aspect, IX_{met}, can be obtained by

$$IX_{met} = V_u \times SAX_{vol}, \tag{26}$$

with the volumetric impacts for SA4–SA7 in Table V.

The preceding introduction outlines a streamlined sustainability assessment methodology for alternative interconnect metals.[262] The proposed seven sustainability indicators offer a holistic, life cycle perspective, enabling a comprehensive evaluation of sustainability. A qualitative analysis of the volumetric impact values in Table V can aid process engineers in identifying trade-offs and making informed decisions for developing advanced interconnect applications. Notably, Al, Ni, Co, and Mo exhibit relatively favorable performance in at least three of the seven indicators, while the platinum-group metals (Ru, Ir, and Rh) demonstrate comparatively poor results in at least six of the seven indicators.

Further analysis involves multiplying the volumetric impact in Table V by the total volume of the metal consumed to achieve a fixed function, i.e., a set volume of a deposited metal. This incorporates the material use efficiency inherent in the deposition and integration methods. Moreover, the application of normalization or weighting factors is recommended to prioritize sustainability indicators based on the situational circumstances, such as company specific sustainability goals, willingness to take financial risks, or location specific regulations/accessibility to materials. Combined with the technological assessment, this streamlined sustainability methodology offers decision makers a foundation for expanding criteria in the selection of alternative metals for advanced interconnect applications.

VIII. SUMMARY AND CONCLUSIONS

The scaling of the interconnect metal pitch is today a crucial challenge in the development of advanced microelectronic technology. As the transistor pitch approaches its physical limits, reducing metal wire pitch has become a primary strategy for further

04 November 2024 08:02:31

© Author(s) 2024

shrinking the circuit area. While transistor stacking can still increase the density, it also necessitates tighter metal pitches to prevent interconnect congestion, potentially offsetting the benefits of stacking. Furthermore, the interconnect *RC* delay poses a significant constraint on the throughput of CMOS circuits, even at current technology nodes. To keep *RC* under control, both the resistance (*R*) and the capacitance (*C*) of the interconnect must be optimized. Optimizing *R* involves maximizing the metal fill factor within lines and vias while using a metal with the lowest possible resistivity. Optimizing *C* requires the use of low-κ dielectrics or incorporating air gaps between lines, which is beyond the scope of this Tutorial.

The current Cu-based dual-damascene metallization scheme, introduced in 1999, is facing increasing challenges. To ensure reliability, Cu metallization requires barrier layers to prevent Cu diffusion into the surrounding dielectrics, which can cause dielectric breakdown. Today, TaN has emerged as the standard barrier material. Electromigration criteria further necessitate the inclusion of Co liner layers between Cu and TaN, as well as on the top of the Cu line (Co all-around liners). Both TaN and Co layers occupy a substantial portion of the volume of scaled interconnects while contributing minimally to line conductance. However, reducing the thickness of these layers without compromising their functionality is increasingly difficult. Despite ongoing efforts, achieving a combined thickness of 1 nm remains challenging. Even at a linewidth of 10 nm, a combined barrier and liner thickness of 1 to 1.5 nm would occupy 20% to 30% of the line volume, significantly impacting line resistance. Moreover, the increasing difficulty of void-free filling of narrow lines using the damascene process suggests that Cu dual-damascene metallization may become unsustainable for metal pitches below 20 nm.

In the last decade, the limitations of Cu-based dual-damascene metallization have spurred the search for alternative metals. Given the relatively simple structure of interconnects, advancements in this field are mainly driven by material choices, making alternative interconnect metallization an exciting area of materials science. As demonstrated in this Tutorial, the pursuit of novel interconnect metals requires a multifaceted approach that considers various criteria. While line resistance is paramount, reliability and thermal aspects must not be overlooked. As illustrated by the calibrated narrow line models in Sec. V, achieving low line resistance necessitates a conductor metal with low resistivity and barrierless metallization to maximize conductor volume. Therefore, promising alternative metals must meet dielectric breakdown and electromigration criteria without the need for barriers. Other important material properties include adhesion to surrounding dielectrics, built-in stress, and oxidation resistance. Furthermore, process readiness and sustainability considerations should not be neglected.

The combination of resistance and reliability criteria has led to a focus on refractory metals—which promise high barrierless reliability—with a short mean free path for charge carriers, low bulk resistivity, and, thus, with low resistivity at nanoscale dimensions. While research initially centered on elemental metals, it has more recently expanded to include binary and ternary intermetallics. Among the materials studied, Ru and Mo have thus far emerged as the most promising candidates. Currently, the semiconductor industry is investing significant resources in developing the necessary process technology to integrate these metals into sub-10 nm interconnect lines without barriers. Their favorable etch characteristics also enable alternative integration routes, such as semidamascene integration, which can potentially facilitate higher aspect ratio lines, further reducing line resistance. Consequently, Ru and Mo are expected to be integrated into logic and memory devices in future technology nodes within the next decade.

Additional promising conductor materials include intercalated graphene and, in the longer term, topological materials, such as Weyl semimetals. While these materials, including binary and ternary intermetallics, are currently being studied as thin films, their behavior in scaled wires remains to be explored. As discussed in Secs. IV C–IV E, integrating these materials into interconnects presents significantly greater challenges compared to elemental metals. The development of manufacturable process technology for these materials is still in its early stages. Yet, the growing interest in such a diverse range of materials, with the potential for further discoveries, suggests that this field will remain a dynamic and exciting area of materials science for years to come.

ACKNOWLEDGMENTS

The authors would like to thank Shibesh Dutta (ASM Netherlands), Anshul Gupta (imec), Kristof Moors (FZ Jülich, imec), Valeria Founta (KU Leuven, imec), Xinyue Zhang (KU Leuven, imec), Ingrid De Wolf (imec, KU Leuven), Nancy Heylen (imec), Johan Meersschaut (imec), Jeroen Scheerder (imec), Olivier Richard (imec), Paola Favia (imec), Kris Vanstreels (imec), Marleen van der Veen (imec), Chen Wu (imec), Gayle Murdoch (imec), Nicolas Jourdan (imec), Antony Peter (imec), Bart Sorée (imec, KU Leuven), Bensu Tunca Altıntaş (imec), Nick Goossens (KU Leuven), Jef Vleugels (KU Leuven), Sean McMitchell (imec), Alfonso Sepulveda Marquez (imec), Sven Van Elshocht (imec), Christopher J. Wilson (imec), and Jürgen Bömmels (imec) for many fruitful discussions. Dawit Abdi (imec) and Odysseas Zografos (imec) are acknowledged for providing Fig. 1(b). The authors would also like to acknowledge the support provided by imec's pline and MCA department for the numerous experiments conducted on this topic over the past decade. This work has been supported by imec's industrial affiliate program on nano-interconnects.

04 November 2024 08:02:31

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jean-Philippe Soulié: Conceptualization (equal); Supervision (equal); Writing – original draft (lead); Writing – review & editing (lead). **Kiroubanand Sankaran:** Conceptualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Benoit Van Troeye:** Conceptualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Alicja Leśniewska:** Conceptualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Olalla Varela Pedreira:** Conceptualization (equal); Writing – original draft (equal); Writing – review & editing

© Author(s) 2024

(equal). **Herman Oprins:** Conceptualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Gilles Delie:** Conceptualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Claudia Fleischmann:** Conceptualization (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Lizzie Boakes:** Conceptualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Cédric Rolin:** Conceptualization (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Lars-Åke Ragnarsson:** Conceptualization (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Kristof Croes:** Conceptualization (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Seongho Park:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Johan Swerts:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Geoffrey Pourtois:** Conceptualization (equal); Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Zsolt Tőkei:** Conceptualization (equal); Funding acquisition (lead); Project administration (equal); Supervision (equal); Writing – review & editing (equal). **Christoph Adelmann:** Conceptualization (lead); Funding acquisition (equal); Project administration (equal); Supervision (equal); Writing – original draft (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

REFERENCES

[1] G. E. Moore, Electronics **38**, 114 (1965).
[2] D. Burg and J. H. Ausubel, PLoS One **16**, e0256245 (2021).
[3] G. E. Moore, "No exponential is forever: But "forever" can be delayed!," in *2003 IEEE International Solid-State Circuits Conference* (IEEE, 2003).
[4] B. Sell *et al.*, "Intel 4 CMOS technology featuring advanced FinFET transistors optimized for high density and high-performance computing," in *2022 IEEE Symposium on VLSI Technology and Circuits: Digest of Technical Papers* (IEEE, 2022), pp. 282–283.
[5] S. Salahuddin *et al.*, "Buried power SRAM DTCO and system-level benchmarking in N3," in *2020 IEEE Symposium on VLSI Technology: Digest of Technical Papers* (IEEE, 2020), pp. 1–2.
[6] M. K. Gupta *et al.*, IEEE Trans. Electron Dev. **68**, 3819 (2021).
[7] M. Bohr, "Interconnect scaling—The real limiter to high performance ULSI," in *1995 IEEE International Electron Devices Meeting* (IEEE, 1995), pp. 241–244.
[8] J. D. Meindl, Comput. Sci. Eng. **5**, 20 (2003).
[9] N. Ekekwe, IEEE Potentials **29**, 26 (2010).
[10] *Advanced Interconnects for ULSI Technology*, edited by M. R. Baklanov, P. S. Ho, and E. Zschech (John Wiley & Sons, Ltd., Chichester, UK, 2012).
[11] J. Clarke *et al.*, "Process technology scaling in an increasingly interconnect dominated world," in *2014 IEEE Symposium on VLSI Technology: Digest of Technical Papers* (IEEE, 2014), pp. 1–2.
[12] M. Hauschildt *et al.*, Jpn. J. Appl. Phys. **53**, 05GA11 (2014).
[13] R. Brain, "Interconnect scaling: Challenges and opportunities," in *2016 IEEE International Electron Devices Meeting* (IEEE, 2016), pp. 9.3.1–9.3.4.
[14] A. A. Vyas, C. Zhou, and C. Y. Yang, IEEE Trans. Nanotechnol. **17**, 4 (2018).
[15] G. Bonilla, N. Lanzillo, C.-K. Hu, C. Penny, and A. Kumar, "Interconnect scaling challenges, and opportunities to enable system-level performance beyond 30 nm pitch," in *2020 IEEE International Electron Devices Meeting* (IEEE, 2020), pp. 20.4.1–20.4.4.
[16] Z. Tökei *et al.*, "Inflection points in interconnect research and trends for 2 nm and beyond in order to solve the RC bottleneck," in *2020 IEEE International Electron Devices Meeting* (IEEE, 2020), pp. 32.2.1–32.2.4.
[17] S. Li, M.-S. Lin, W.-C. Chen, and C.-C. Tsai, "Interconnect in the era of 3DIC," in *2022 IEEE Custom Integrated Circuits Conference* (IEEE, 2022), pp. 1–5.
[18] T. Nogami, JSAP Rev. **2023**, 230210.
[19] C. Auth *et al.*, "A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *2012 IEEE Symposium on VLSI Technology: Digest of Technical Papers* (IEEE, 2012), pp. 131–132.
[20] N. Loubet *et al.*, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in *2017 IEEE Symposium on VLSI Technology: Digest of Technical Papers* (IEEE, 2017).
[21] H. Jagannathan *et al.*, "Vertical-transport nanosheet technology for CMOS scaling beyond lateral-transport devices," in *2021 IEEE International Electron Devices Meeting* (IEEE, 2021), pp. 26.1.1–26.1.4.
[22] L. Gosset *et al.*, Microelectron. Eng. **82**, 321 (2005).
[23] H. Chang *et al.*, "Airgap integration on patterned metal lines for advanced interconnect performance scaling," in *2023 IEEE International Interconnect Technology Conference* (IEEE, 2023), pp. 1–4.
[24] C. Adelmann *et al.*, "Alternative metals for advanced interconnects," in *2014 IEEE International Interconnect Technology Conference* (IEEE, 2014), pp. 173–176.
[25] X. Zhang *et al.*, "Ruthenium interconnect resistivity and reliability at 48 nm pitch," in *2016 IEEE International Interconnect Technology Conference* (IEEE, 2016), pp. 31–33.
[26] L. G. Wen *et al.*, "Ruthenium metallization for advanced interconnects," in *2016 IEEE International Interconnect Technology Conference* (IEEE, 2016), pp. 34–36.
[27] D. C. Edelstein, "20 years of Cu BEOL in manufacturing, and its future prospects," in *2017 IEEE International Electron Devices Meeting* (IEEE, 2017), pp. 14.1.1–14.1.4.
[28] C. Adelmann *et al.*, "Alternative metals: From *ab initio* screening to calibrated narrow line models," in *2018 IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 154–156.
[29] K. Lin, M. Chandhok, and M. Reshotko, "The future of interconnects: Challenges and enabling technologies," in *2018 IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 2–3.
[30] D. Gall, "The resistivity bottleneck: The search for new interconnect metals," in *2020 IEEE International Symposium on VLSI Technology, Systems and Applications* (IEEE, 2020), pp. 112–113.
[31] D. Gall, J. Appl. Phys. **127**, 050901 (2020).
[32] D. Gall *et al.*, MRS Bull. **46**, 959 (2021).
[33] C. Adelmann *et al.*, "Intermetallic compounds as alternatives to copper for advanced interconnect metallization," in *2023 IEEE International Interconnect Technology Conference* (IEEE, 2023), pp. 1–3.
[34] D. Edelstein *et al.*, "Full copper wiring in a sub-0.25 μm CMOS ULSI technology," in *1997 IEEE Intern Electron Devices Meeting* (IEEE, 1997), pp. 773–776.
[35] J. Kriz *et al.*, Microelectron. Eng. **85**, 2128 (2008).
[36] T. Gupta, *Copper Interconnect Technology* (Springer, New York, 2009).
[37] A. S. Oates, ECS J. Solid State Sci. Technol. **4**, N3168 (2014).
[38] C.-K. Hu *et al.*, "Future on-chip interconnect metallization and electromigration," in *2018 IEEE International Reliability Physics Symposium* (IEEE, 2018), pp. 4F.1-1–4F.1-6.
[39] As of 2024, the ITRS website is offline. a mirror of the original website (as of 2015) can be found at https://web.archive.org/web/20151228041321/http://www.itrs.net/; accessed 20 October 2024.
[40] "International Roadmap for Devices and Systems—IRDS"; see https://irds.ieee.org/; accessed 20 October 2024.

04 November 2024 08:02:31

© Author(s) 2024

[41]T. Yamamoto, "Process technology toward 1 nm and beyond," in *Short Course SC-1 at 2023 IEEE International Electron Devices Meeting* (IEEE, 2023).
[42]C.-H. Chang *et al.*, "Critical process features enabling aggressive contacted gate pitch scaling for 3 nm CMOS technology and beyond," in *2022 IEEE International Electron Devices Meeting* (IEEE, 2022), pp. 27.1.1–27.1.4.
[43]S.-Y. Wu *et al.*, "A 3 nm CMOS FinFlex^{TM} platform technology with enhanced power efficiency and performance for mobile SoC and high performance computing applications," in *2022 IEEE International Electron Devices Meeting* (IEEE, 2022), pp. 27.5.1–27.5.4.
[44]K. Fuchs, Math. Proc. Cambridge Philos. Soc. **34**, 100 (1938).
[45]E. H. Sondheimer, Adv. Phys. **1**, 1 (1952).
[46]S. B. Soffer, J. Appl. Phys. **38**, 1710 (1967).
[47]A. F. Mayadas, M. Shatzkes, and J. F. Janak, Appl. Phys. Lett. **14**, 345 (1969).
[48]A. F. Mayadas and M. Shatzkes, Phys. Rev. B **1**, 1382 (1970).
[49]J. R. Sambles and K. C. Elson, J. Phys. F: Met. Phys. **10**, 1487 (1980).
[50]Y. Namba, Jpn. J. Appl. Phys. **9**, 1326 (1970).
[51]H. Marom and M. Eizenberg, J. Appl. Phys. **99**, 123705 (2006).
[52]V. Timoshevskii, Y. Ke, H. Guo, and D. Gall, J. Appl. Phys. **103**, 113705 (2008).
[53]B. Feldman, R. Deng, and S. T. Dunham, J. Appl. Phys. **103**, 113715 (2008).
[54]Y. Ke *et al.*, Phys. Rev. B **79**, 155406 (2009).
[55]J. M. Rickman and K. Barmak, J. Appl. Phys. **112**, 013704 (2012).
[56]K. Moors, B. Sorée, Z. Tőkei, and W. Magnus, J. Appl. Phys. **116**, 063714 (2014).
[57]K. Moors, B. Sorée, and W. Magnus, J. Appl. Phys. **118**, 124307 (2015).
[58]T. Zhou and D. Gall, Phys. Rev. B **97**, 165406 (2018).
[59]T. Zhou, P. Zheng, S. C. Pandey, R. Sundararaman, and D. Gall, J. Appl. Phys. **123**, 155107 (2018).
[60]K. Hinode, Y. Hanaoka, K.-I. Takeda, and S. Kondo, Jpn. J. Appl. Phys. **40**, L1097 (2001).
[61]W. Steinhögl, G. Schindler, G. Steinlesberger, and M. Engelhardt, Phys. Rev. B **66**, 075414 (2002).
[62]S. Maîtrejean, R. Gers, T. Mourier, A. Toffoli, and G. Passemard, Microelectron. Eng. **83**, 2396 (2006).
[63]H. Marom, J. Mullin, and M. Eizenberg, Phys. Rev. B **74**, 045411 (2006).
[64]K. Khoo *et al.*, Jpn. J. Appl. Phys. **46**, 4070 (2007).
[65]R. L. Graham *et al.*, Appl. Phys. Lett. **96**, 042116 (2010).
[66]T.-H. Kim *et al.*, Jpn. J. Appl. Phys. **50**, 08LB09 (2011).
[67]J. S. Chawla, F. Gstrein, K. P. O'Brien, J. S. Clarke, and D. Gall, Phys. Rev. B **84**, 235423 (2011).
[68]R. S. Smith *et al.*, AIP Adv. **9**, 025015 (2019).
[69]D. Gall, J. Appl. Phys. **119**, 085101 (2016).
[70]S. Dutta *et al.*, J. Appl. Phys. **122**, 025107 (2017).
[71]K. Moors, K. Sankaran, G. Pourtois, and C. Adelmann, Phys. Rev. Mater. **6**, 123804 (2022).
[72]B. Van Troeye, K. Sankaran, Z. Tőkei, C. Adelmann, and G. Pourtois, Phys. Rev. B **108**, 125117 (2023).
[73]E. H. Sondheimer, Adv. Phys. **50**, 499 (2001).
[74]H. Abrams, Metallography **4**, 59 (1971).
[75]A. Thorvaldsen, Acta Mater. **45**, 595 (1997).
[76]J. H. Mooij, Phys. Stat. Sol. A **17**, 521 (1973).
[77]M. Gurvitch, Phys. Rev. B **24**, 7404 (1981).
[78]C. C. Tsuei, Phys. Rev. Lett. **57**, 1943 (1986).
[79]Y. Imry, Phys. Rev. Lett. **44**, 469 (1980).
[80]P. A. Lee and T. V. Ramakrishnan, Rev. Mod. Phys. **57**, 287 (1985).
[81]R. D. Doherty *et al.*, Mater. Sci. Eng. A **238**, 219 (1997).
[82]F. J. Humphreys and M. Hatherly, *Recrystallization and Related Annealing Phenomena*, 2nd ed. (Elsevier, Oxford, 2004).
[83]C. V. Thompson, Annu. Rev. Mater. Sci. **30**, 159 (2000).
[84]I. Petrov, P. B. Barna, L. Hultman, and J. E. Greene, J. Vac. Sci. Technol. A **21**, S117 (2003).
[85]T. Zhou, A. Jog, and D. Gall, Appl. Phys. Lett. **120**, 241603 (2022).
[86]B. Feldman, S. Park, M. Haverty, S. Shankar, and S. T. Dunham, Phys. Stat. Sol. B **247**, 1791 (2010).
[87]B. Zhou, Y. Xu, S. Wang, G. Zhou, and K. Xia, Solid State Commun. **150**, 1422 (2010).
[88]M. César, D. Liu, D. Gall, and H. Guo, Phys. Rev. Appl. **2**, 044007 (2014).
[89]T.-H. Kim *et al.*, Nano Lett. **10**, 3096 (2010).
[90]Y. F. Zhu, X. Y. Lang, W. T. Zheng, and Q. Jiang, ACS Nano **4**, 3781 (2010).
[91]S. M. Rossnagel and T. S. Kuan, J. Vac. Sci. Technol. B **22**, 240 (2004).
[92]M. Tay, K. Li, and Y. Wu, J. Vac. Sci. Technol. B **23**, 1412 (2005).
[93]B. Feldman and S. T. Dunham, Appl. Phys. Lett. **95**, 222101 (2009).
[94]A. J. Learn and D. W. Foster, J. Appl. Phys. **58**, 2001 (1985).
[95]Q. G. Zhang, B. Y. Cao, X. Zhang, M. Fujii, and K. Takahashi, Phys. Rev. B **74**, 134109 (2006).
[96]Q. G. Zhang *et al.*, Appl. Phys. Lett. **89**, 114102 (2006).
[97]J. M. Camacho and A. Oliva, Thin Solid Films **515**, 1881 (2006).
[98]T. Sun *et al.*, Phys. Rev. B **79**, 041402(R) (2009).
[99]T. Sun *et al.*, Phys. Rev. B **81**, 155454 (2010).
[100]K. Barmak *et al.*, J. Vac. Sci. Technol. A **32**, 061503 (2014).
[101]V. Founta *et al.*, Materialia **24**, 101511 (2022).
[102]N. V. Volkenshtejn *et al.*, Phys. Met. Metallogr. **45**, 54 (1978).
[103]E. M. Savitskii, V. P. Polyakova, and N. B. Gorina, Platin. Met. Rev. **23**, 57 (1979).
[104]M. De Clercq *et al.*, Phys. Rev. Mater. **2**, 033801 (2018).
[105]S. Kumar, C. Multunas, B. Defay, D. Gall, and R. Sundararaman, Phys. Rev. Mater. **6**, 085002 (2022).
[106]N. W. Ashcroft and N. D. Mermin, *Solid State Physics* (Holt, Rinehart, and Winston, New York, 1976).
[107]C. H. Johansson and J. O. Linde, Ann. Phys. **417**, 1 (1936).
[108]Y. Terada, K. Ohkubo, T. Mohri, and T. Suzuki, Mater. Trans. **43**, 3167 (2002).
[109]S. Poncé, W. Li, S. Reichardt, and F. Giustino, Rep. Prog. Phys. **83**, 036501 (2020).
[110]L. Chen *et al.*, J. Appl. Phys. **129**, 035301 (2021).
[111]K. L. Krewer *et al.*, Appl. Phys. Lett. **116**, 102406 (2020).
[112]J. W. McPherson, Microelectron. Reliab. **52**, 1753 (2012).
[113]C. Wu, Y. Li, M. R. Baklanov, and K. Croes, ECS J. Solid State Sci. Technol. **4**, N3065 (2014).
[114]K. Croes *et al.*, "Interconnect metals beyond copper: Reliability challenges and opportunities," in *2018 IEEE International Electron Devices Meeting* (IEEE, 2018), pp. 5.3.1–5.3.4.
[115]*Low Dielectric Constant Materials for IC Applications*, edited by P. S. Ho, J. J. Leu, and W. W. Lee (Springer, Berlin, 2003).
[116]D. Shamiryan, T. Abell, F. Iacopi, and K. Maex, Mater. Today **7**, 34 (2004).
[117]W. Volksen, R. D. Miller, and G. Dubois, Chem. Rev. **110**, 56 (2010).
[118]A. Grill, S. M. Gates, T. E. Ryan, S. V. Nguyen, and D. Priyadarshini, Appl. Phys. Rev. **1**, 011306 (2014).
[119]C. Witt *et al.*, "Testing the limits of TaN barrier scaling," in *2018 IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 54–56.
[120]O. Varela Pedreira *et al.*, "Scaled TaN barriers for Cu interconnects: Reliability performance," in *2019 IEEE International Interconnect Technology Conference* (IEEE, 2019).
[121]A. Joi *et al.*, J. Appl. Phys. **132**, 175704 (2022).
[122]L. Zhao *et al.*, "A novel test structure to study intrinsic reliability of barrier/low-k," in *2009 IEEE International Reliability Physics Symposium* (IEEE, 2009), pp. 848–850.
[123]K. L. Lin *et al.*, "Demonstration of a sidewall capacitor to evaluate dielectrics and metal barrier thin films," in *2014 IEEE International Interconnect Technology Conference* (IEEE, 2014), pp. 177–180.
[124]K. Croes *et al.*, "Low field TDDB of BEOL interconnects using >40 months of data," in *2013 IEEE International Reliability Physics Symposium* (IEEE, 2013), pp. 2F.4.1–2F.4.8.
[125]J. R. Lloyd, E. Liniger, and T. M. Shaw, J. Appl. Phys. **98**, 084109 (2005).
[126]T.-Y. Jeong *et al.*, "Low voltage IMD-TDDB lifetime model for advanced future logic technology nodes," in *2015 IEEE International Interconnect Technology Conference* (IEEE, 2015), pp. 299–302.

04 November 2024 08:02:31

© Author(s) 2024

[127]E. Chery, X. Federspiel, D. Roy, F. Volpi, and J. M. Chaix, Microelectron. Eng. **109**, 90 (2013).
[128]K. Croes and Z. Tökei, "E- and $\sqrt{E}$-model too conservative to describe low field time dependent dielectric breakdown," in *2010 IEEE International Reliability Physics Symposium* (IEEE, 2010), pp. 543–548.
[129]E. G. Liniger, S. A. Cohen, and G. Bonilla, "Low-field TDDB reliability data to enable accurate lifetime predictions," in *2014 IEEE International Reliability Physics Symposium* (IEEE, 2014), pp. BD.4.1–BD.4.4.
[130]P. J. Roussel *et al.*, "New methodology for modelling MOL TDDB coping with variability," in *2018 IEEE International Reliability Physics Symposium* (IEEE, 2018), pp. 3A.5–1–3A.5–6.
[131]C. Wu *et al.*, "Insights into metal drift induced failure in MOL and BEOL," in *2018 IEEE International Reliability Physics Symposium* (IEEE, 2018), pp. 3A.1.1–3A.1.7.
[132]J. Black, IEEE Trans. Electron Dev. **16**, 338 (1969).
[133]J. Lienig and G. Jerke, in *18th International Conference on VLSI Design Held Jointly with 4th International Conference on Embedded Systems Design* (IEEE, 2005), p. 77.
[134]C. Ryu *et al.*, IEEE Trans. Electron Devices **46**, 1113 (1999).
[135]A. Lodder and J. P. Dekker, AIP Conf. Proc. **418**, 315 (1998).
[136]C.-K. Hu, R. Rosenberg, H. Rathore, D. Nguyen, and B. Agarwala, "Scaling effect on electromigration in on-chip Cu wiring," in *1999 IEEE International Interconnect Technology Conference* (IEEE, 1999), pp. 267–269.
[137]C. S. Hau-Riege and C. V. Thompson, Appl. Phys. Lett. **78**, 3451 (2001).
[138]E. Ogawa, K.-D. Lee, V. Blaschke, and P. Ho, IEEE Trans. Reliab. **51**, 403 (2002).
[139]M. Hauschildt *et al.*, "Electromigration early failure void nucleation and growth phenomena in Cu and Cu(Mn) interconnects," in *2013 IEEE International Reliability Physics Symposium* (IEEE, 2013), pp. 2C.1.1–2C.1.6.
[140]H. Zahedmanesh, O. Varela Pedreira, C. Wilson, Z. Tőkei, and K. Croes, "Copper electromigration; prediction of scaling limits," in *2019 IEEE International Interconnect Technology Conference* (IEEE, 2019), pp. 3–5.
[141]S. Choi *et al.*, "Effect of metal line width on electromigration of BEOL Cu interconnects," in *2018 IEEE International Reliability Physics Symposium* (IEEE, 2018), pp. 4F.4-1–4F.4-6.
[142]N. Jourdan *et al.*, "CVD-Mn/CVD-Ru-based barrier/liner so4lution for advanced BEOL Cu/low-k interconnects," in *2016 IEEE International Interconnect Technology Conference* (IEEE, 2016), pp. 37–39.
[143]O. Varela Pedreira *et al.*, "Electromigration and thermal storage study of barrierless Co vias," in *2018 IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 48–50.
[144]O. Varela Pedreira *et al.*, "Reliability benchmark of various via prefill metals," in *2022 IEEE International Interconnect Technology Conference* (IEEE, 2022), pp. 31–33.
[145]B. Guralnik *et al.*, Rev. Sci. Instrum. **92**, 094711 (2021).
[146]H. Oprins *et al.*, "Experimental thermal characterization of thin film low-k dielectric materials," in *2024 IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems* (IEEE, 2024), pp. 1–8.
[147]X. Chang *et al.*, "Thermal analysis of advanced back-end-of-line structures and the impact of design parameters," in *2022 IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems* (IEEE, 2022), pp. 1–8.
[148]M. Lofrano *et al.*, "Joule heating investigation for advanced interconnect schemes with airgaps," in *2021 IEEE International Interconnect Technology Conference* (IEEE, 2021), pp. 1–3.
[149]X. Chang *et al.*, "Calibrated fast thermal calculation and experimental characterization of advanced BEOL stacks," in *2023 IEEE International Interconnect Technology Conference* (IEEE, 2023), pp. 1–3.
[150]M. Lofrano *et al.*, "Towards accurate temperature prediction in BEOL for reliability assessment," in *2023 IEEE International Reliability Physics Symposium* (IEEE, 2023), pp. 1–7.
[151]J. G. Hust and L. L. Sparks, "Lorenz ratios of technically important metals and alloys," NBS Technical Report No. 634, U.S. Department of Commerce (1973).
[152]R. W. Powell, R. P. Tye, and M. J. Woodman, Platin. Met. Rev. **6**, 138 (1962).
[153]D. G. Cahill *et al.*, J. Appl. Phys. **93**, 793 (2002).
[154]D. G. Cahill *et al.*, Appl. Phys. Rev. **1**, 011305 (2014).
[155]D. Li *et al.*, Appl. Phys. Lett. **83**, 2934 (2003).
[156]N. Stojanovic, D. H. S. Maithripala, J. M. Berg, and M. Holtz, Phys. Rev. B **82**, 075418 (2010).
[157]H. Wang, J. Liu, X. Zhang, and K. Takahashi, Int. J. Heat Mass Transf. **66**, 585 (2013).
[158]C. Huang, Y. Feng, X. Zhang, J. Li, and G. Wang, Phys. E **58**, 111 (2014).
[159]S. D. Sawtelle and M. A. Reed, Phys. Rev. B **99**, 054304 (2019).
[160]K. Sankaran, S. Clima, M. Mees, and G. Pourtois, ECS J. Solid State Sci. Technol. **4**, N3127 (2014).
[161]K. Sankaran *et al.*, "Exploring alternative metals to Cu and W for interconnects: An ab initio insight," in *2014 IEEE International Interconnect Technology Conference* (IEEE, 2014), pp. 193–196.
[162]J. Bass, "Pure metal resistivities at T= 273.2 K," in *Electrical Resistivity, Kondo and Spin Fluctuation Systems, Spin Glasses and Thermopower*, Landolt-Börnstein: Numerical Data and Functional Relationships in Science and Technology Vol. 15a, edited by K.-H. Hellwege and J. L. Olsen (Springer, Berlin, 1983), Chap. 1.2.1, pp. 5–99.
[163]*CRC Handbook of Chemistry and Physics*, 95th ed., edited by W. Haynes, D. Lide, and T. Bruno (CRC Press, Boca Raton, FL, 2014).
[164]M. Popovici *et al.*, Chem. Mater. **29**, 4654 (2017).
[165]D. Gall, "Metals for low-resistivity interconnects," in *2018 IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 157–159.
[166]A. Gupta *et al.*, "Barrierless ALD molybdenum for buried power rail and via-to-buried power rail metallization," in *2022 IEEE International Interconnect Technology Conference* (IEEE, 2022), pp. 58–60.
[167]M. Hosseini *et al.*, "ALD Mo for advanced MOL local interconnects," in *2022 IEEE International Interconnect Technology Conference* (IEEE, 2022), pp. 145–147.
[168]A. Gupta *et al.*, "Buried power rail metal exploration towards the 1 nm node," in *2021 IEEE International Electron Devices Meeting* (IEEE, 2021), pp. 22.5.1–22.5.4.
[169]S. Dutta *et al.*, IEEE Electron Device Lett. **38**, 949 (2017).
[170]S. Dutta *et al.*, "Ruthenium interconnects with 58 nm^2 cross-section area using a metal-spacer process," in *2017 IEEE International Interconnect Technology Conference* (IEEE, 2017), pp. 1–3.
[171]S. Dutta, K. Moors, M. Vandemaele, and C. Adelmann, IEEE Electron Device Lett. **39**, 268 (2018).
[172]S. Dutta *et al.*, IEEE Electron Device Lett. **39**, 731 (2018).
[173]I. Ciofi *et al.*, IEEE Trans. Electron Devices **63**, 2488 (2016).
[174]C. Auth *et al.*, "A 10 nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects," in *2017 IEEE International Electron Devices Meeting* (IEEE, 2017), pp. 29.1.1–29.1.4.
[175]A. Yeoh *et al.*, "Interconnect stack using self-aligned quad and double patterning for 10 nm high volume manufacturing," in *2018 IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 144–147.
[176]F. Griggio *et al.*, "Reliability of dual-damascene local interconnects featuring cobalt on 10 nm logic technology," in *2018 IEEE International Reliability Physics Symposium* (IEEE, 2018), pp. 6E.3-1–6E.3-5.
[177]D. Tierno *et al.*, Microelectron. Reliab. **100-101**, 113407 (2019).
[178]D. Tierno *et al.*, "Impact of surface condition on cobalt drift into LK3.0 films," in *2020 IEEE International Interconnect Technology Conference* (IEEE, 2020), pp. 142–144.
[179]A. Leśniewska *et al.*, "Dielectric reliability study of 21 nm pitch interconnects with barrierless Ru fill," in *2020 IEEE International Reliability Physics Symposium* (IEEE, 2020), pp. 1–6.
[180]A. Leśniewska *et al.*, "Reliability of a DME Ru semidamascene scheme with 16 nm wide airgaps," in *2021 IEEE International Reliability Physics Symposium* (IEEE, 2021), pp. 1–6.
[181]L. G. Wen *et al.*, ACS Appl. Mater. Interfaces **8**, 26119 (2016).

04 November 2024 08:02:31

© Author(s) 2024

[182]D. Tierno *et al.*, "Reliability of barrierless PVD Mo," in *2021 IEEE International Interconnect Technology Conference* (IEEE, 2021), pp. 1–3.
[183]O. Varela Pedreira *et al.*, "Reliability study on cobalt and ruthenium as alternative metals for advanced interconnects," in *2017 IEEE International Reliability Physics Symposium* (IEEE, 2017), pp. 6B-2.1–6B-2.8.
[184]O. Varela Pedreira *et al.*, "Metal reliability mechanisms in ruthenium interconnects," in *2020 IEEE International Reliability Physics Symposium* (IEEE, 2020), pp. 1–7.
[185]S. Beyne *et al.*, IEEE Trans. Electron Devices **66**, 5278 (2019).
[186]Z. Tőkei *et al.*, "On-chip interconnect trends, challenges and solutions: How to keep RC and reliability under control," in *2016 IEEE Symposium on VLSI Technology: Digest of Technical Papers* (IEEE, 2016), pp. 1–2.
[187]D. Wan *et al.*, "Subtractive etch of ruthenium for sub-5 nm interconnect," in *2018 IEEE International Interconnect Technology Conference* (IEEE, 2018), pp. 10–12.
[188]R. Murali, K. Brenner, Y. Yang, T. Beck, and J. D. Meindl, IEEE Electron Device Lett. **30**, 611 (2009).
[189]S. Rakheja, V. Kumar, and A. Naeemi, Proc. IEEE **101**, 1740 (2013).
[190]J. Jiang, J. H. Chu, and K. Banerjee, "CMOS-compatible doped-multilayer-graphene interconnects for next-generation VLSI," in *2018 IEEE International Electron Devices Meeting* (IEEE, 2018), pp. 34.5.1–34.5.4.
[191]J. Jiang, K. Parto, W. Cao, and K. Banerjee, IEEE J. Electron Devices Soc. **7**, 878 (2019).
[192]J. Jiang, J. Kang, and K. Banerjee, "Characterization of self-heating and current-carrying capacity of intercalation doped graphene-nanoribbon interconnects," in *2017 IEEE International Reliability Physics Symposium* (IEEE, 2017), pp. 6B–1.1–6B–1.6.
[193]K. Agashiwala *et al.*, "Reliability and performance of CMOS-compatible multi-level graphene interconnects incorporating vias," in *2020 IEEE International Electron Devices Meeting* (IEEE, 2020), pp. 31.1.1–31.1.4.
[194]C. Xu, H. Li, and K. Banerjee, "Graphene nano-ribbon (GNR) interconnects: A genuine contender or a delusive dream?," in *2008 IEEE International Electron Devices Meeting* (IEEE, 2008), pp. 1–4.
[195]C. Xu, H. Li, and K. Banerjee, IEEE Trans. Electron Devices **56**, 1567 (2009).
[196]K. Agashiwala *et al.*, IEEE Trans. Electron Devices **68**, 2083 (2021).
[197]I. Khrapach *et al.*, Adv. Mater. **24**, 2844 (2012).
[198]J. Jiang *et al.*, Nano Lett. **17**, 1482 (2017).
[199]S. W. Li *et al.*, "Intercalated graphene as next generation back-end-of-line conductors," in *2023 IEEE International Electron Devices Meeting* (IEEE, 2023), pp. 1–4.
[200]J.-Z. Huang *et al.*, ACS Appl. Nano Mater. **6**, 10680 (2023).
[201]S. Achra *et al.*, Carbon **183**, 999 (2021).
[202]S. Achra *et al.*, "Characterization of interface interactions between graphene and ruthenium," in *2020 IEEE International Interconnect Technology Conference* (IEEE, 2020), pp. 133–135.
[203]R. Mehta, S. Chugh, and Z. Chen, Nano Lett. **15**, 2024 (2015).
[204]M. Son *et al.*, npj 2D Mater. Appl. **5**, 41 (2021).
[205]Z. Li *et al.*, ACS Nano **5**, 3385 (2011).
[206]X. Kang *et al.*, "Evaluation of Cu/graphene integration schemes for its application on CMOS BEOL interconnect," in *2020 IEEE 15th International Conference on Solid-State & Integrated Circuit Technology* (IEEE, 2020), pp. 1–3.
[207]T. Nogami *et al.*, "Electromigration and line R of graphene capped Cu dual damascene interconnect," in *2021 IEEE International Electron Devices Meeting* (IEEE, 2021), pp. 22.2.1–22.2.4.
[208]J. A. Howell, S. E. Mohney, and C. L. Muhlstein, J. Vac. Sci. Technol. B **29**, 042002 (2011).
[209]J.-P. Soulié, Z. Tőkei, J. Swerts, and C. Adelmann, "Thickness scaling of NiAl thin films for alternative interconnect metallization," in *2020 IEEE International Interconnect Technology Conference* (IEEE, 2020), pp. 151–153.
[210]L. Chen, D. Ando, Y. Sutou, and J. Koike, J. Vac. Sci. Technol. B **37**, 031215 (2019).
[211]L. Chen, D. Ando, Y. Sutou, D. Gall, and J. Koike, Appl. Phys. Lett. **113**, 183503 (2018).
[212]J.-P. Soulié, Z. Tőkei, J. Swerts, and C. Adelmann, "Aluminide intermetallics for advanced interconnect metallization: Thin film studies," in *2021 IEEE International Interconnect Technology Conference* (IEEE, 2021), pp. 1–3.
[213]J.-P. Soulié, Z. Tőkei, J. Swerts, and C. Adelmann, "Improved resistivity of NiAl thin films at low temperature for advanced interconnect metallization," in *2022 IEEE International Interconnect Technology Conference* (IEEE, 2022), pp. 73–75.
[214]L. Chen, D. Ando, Y. Sutou, S. Yokogawa, and J. Koike, Appl. Surf. Sci. **497**, 143810 (2019).
[215]J.-P. Soulié, Z. Tőkei, N. Heylen, and C. Adelmann, "Reduced resistivity of NiAl by backthinning for advanced interconnect metallization," in *2023 IEEE International Interconnect Technology Conference* (IEEE, 2023), pp. 1–3.
[216]T. Kuge, M. Yahagi, and J. Koike, J. Alloys Compd. **918**, 165615 (2022).
[217]T. Kuge, M. Yahagi, and J. Koike, "Cual intermetallic compound for Cu alternative," in *2023 IEEE International Interconnect Technology Conference and IEEE Materials for Advanced Metallization Conference* (IEEE, 2023), pp. 1–3.
[218]J.-P. Soulié *et al.*, J. Vac. Sci. Technol. B **42**, 043203 (2024).
[219]J. Koike, T. Kuge, L. Chen, and M. Yahagi, "Intermetallic compounds for interconnect metal beyond 3 nm node," in *2021 IEEE International Interconnect Technology Conference* (IEEE, 2021), pp. 1–3.
[220]J.-P. Soulié *et al.*, Microelectron. Eng. **286**, 112141 (2024).
[221]Y.-Y. Fang *et al.*, Appl. Phys. Lett. **124**, 142108 (2024).
[222]L. Chen, D. Ando, Y. Sutou, M. Yahagi, and J. Koike, "Possibility of Cu_2Mg for liner-barrier free interconnects," in *2020 IEEE International Interconnect Technology Conference* (IEEE, 2020), pp. 85–87.
[223]O. Zobac, A. Kroupa, A. Zemanova, and K. W. Richter, Metall. Mater. Trans. A **50**, 3805 (2019).
[224]M. Zhang, S. Kumar, R. Sundararaman, and D. Gall, J. Appl. Phys. **133**, 045102 (2023).
[225]N. Cai, H. Qin, X. Tong, and G. Zhou, Surf. Sci. **618**, 20 (2013).
[226]J. H. Moon *et al.*, Adv. Sci. **10**, 2207321 (2023).
[227]M. W. Barsoum, Prog. Solid State Chem. **28**, 201 (2000).
[228]P. Eklund, M. Beckers, U. Jansson, H. Högberg, and L. Hultman, Thin Solid Films **518**, 1851 (2010).
[229]M. W. Barsoum, *MAX Phases: Properties of Machinable Ternary Carbides and Nitrides* (Wiley, Weinheim, 2013).
[230]M. Radovic and M. W. Barsoum, Am. Ceram. Soc. Bull. **92**, 20 (2013).
[231]J. Gonzalez-Julian, J. Am. Ceram. Soc. **104**, 659 (2021).
[232]M. Dahlqvist, M. W. Barsoum, and J. Rosen, Mater. Today **72**, 1 (2024).
[233]T. Ouisse *et al.*, Phys. Rev. B **92**, 045133 (2015).
[234]K. Sankaran, K. Moors, Z. Tőkei, C. Adelmann, and G. Pourtois, Phys. Rev. Mater. **5**, 056002 (2021).
[235]T. Harada, Mater. Today Adv. **11**, 100146 (2021).
[236]A. P. Mackenzie, Rep. Prog. Phys. **80**, 032501 (2017).
[237]T. Harada and Y. Okada, APL Mater. **10**, 070902 (2022).
[238]Y. Zhang *et al.*, Nat. Commun. **15**, 1399 (2024).
[239]M. D. Bachmann *et al.*, Nat. Phys. **18**, 819 (2022).
[240]M. Brahlek *et al.*, Phys. Rev. Mater. **3**, 093401 (2019).
[241]J. M. Ok *et al.*, APL Mater. **8**, 051104 (2020).
[242]D. J. Hagen *et al.*, Adv. Mater. Interfaces **9**, 2200013 (2022).
[243]T. Harada, T. Nagai, M. Oishi, and Y. Masahiro, J. Appl. Phys. **133**, 085302 (2023).
[244]S.-Y. Xu *et al.*, Science **349**, 613 (2015).
[245]B. Q. Lv *et al.*, Nat. Phys. **11**, 724 (2015).
[246]C. Zhang *et al.*, Nat. Mater. **18**, 482 (2019).
[247]H. J. Han *et al.*, Adv. Mater. **35**, 2208965 (2023).
[248]C.-T. Chen *et al.*, "Topological semimetals for scaled back-end-of-line interconnect beyond Cu," in *2020 IEEE International Electron Devices Meeting* (IEEE, 2020), pp. 32.4.1–32.4.4.
[249]S.-W. Lien *et al.*, npj Quantum Mater. **8**, 3 (2023).
[250]N. A. Lanzillo, U. Bajpai, I. Garate, and C.-T. Chen, Phys. Rev. Appl. **18**, 034053 (2022).

04 November 2024 08:02:31

© Author(s) 2024

[251]G. Murdoch *et al.*, "Semidamascene interconnects for 2 nm node and beyond," in *2020 IEEE International Interconnect Technology Conference* (IEEE, 2020), pp. 4–6.
[252]S. Decoster *et al.*, J. Vac. Sci. Technol. B **40**, 032802 (2022).
[253]K. Motoyama *et al.*, "Metal-induced line width variability challenge and mitigation strategy in advanced post-Cu interconnects," in *2022 IEEE International Interconnect Technology Conference* (IEEE, 2022), pp. 55–57.
[254]R. Messier, A. P. Giri, and R. A. Roy, J. Vac. Sci. Technol. A **2**, 500 (1984).
[255]H. Windischmann, Crit. Rev. Solid State Mater. Sci. **17**, 547 (1992).
[256]A. Bhandari, B. W. Sheldon, and S. J. Hearne, J. Appl. Phys. **101**, 033528 (2007).
[257]G. Abadias *et al.*, J. Vac. Sci. Technol. A **36**, 020801 (2018).
[258]V. Founta *et al.*, "Stress and thermal stress evolution in Mo and Ru thin films," in *2022 IEEE International Interconnect Technology Conference* (IEEE, 2022), pp. 70–72.
[259]I. Shao *et al.*, "An alternative low resistance MOL technology with electroplated rhodium as contact plugs for 32 nm CMOS and beyond," in *2007 IEEE International Interconnect Technology Conference* (IEEE, 2007), pp. 102–104.
[260]N. A. Lanzillo and D. C. Edelstein, J. Vac. Sci. Technol. B **40**, 052801 (2022).
[261]S.-H. Son, H.-K. Lee, and S.-C. Park, Surf. Interface Anal. **42**, 1244 (2010).
[262]L. Boakes, L.-Å. Ragnarsson, C. Rolin, and C. Adelmann, "Selection of alternative local interconnect metals: Beyond traditional criteria towards sustainable and secure supply chains," arXiv:2401.02864 (2024).
[263]M. Bromberg, "Herfindahl-Hirschman Index (HHI): Definition, formula, and example"; see https://www.investopedia.com/terms/h/hhi.asp.
[264]"Antitrust division, Herfindahl-Hirschman Index"; see https://www.justice.gov/atr/herfindahl-hirschman-index.
[265]World Mining Congress, "World mining data 2023"; see https://wmc.agh.edu.pl/wp-content/uploads/2023/05/WMD2023.pdf.
[266]European Commission's Joint Research Centre, "Raw materials profiles. RMIS—Raw materials information system"; see https://rmis.jrc.ec.europa.eu/rmp/.
[267]S. M. Fortier *et al.*, Min. Eng. **74**, 34 (2022).
[268]European Commission and Entrepreneurship for Internal Market Industry and SMEs, M. Grohol, and C. Veeh, "Study on the critical raw materials for the EU 2023," Final report, 2023.
[269]European Commission, "Conflict minerals regulation: The regulation explained," (2023); see https://policy.trade.ec.europa.eu/development-and-sustainability/conflict-minerals-regulation/regulation-explained_en.
[270]ANSI/UL Standard for Safety, "Ul 3600—Measuring and reporting circular economy aspects of products, sites and organizations," (2023).
[271]P. Nuss and M. J. Eckelman, PLoS One **9**, e101298 (2014).
[272]European Platform on Life Cycle Assessment, Developer Environmental Footprint (EF); see https://eplca.jrc.ec.europa.eu/LCDN/developerEF.xhtml.
[273]L. van Oers, J. B. Guinée, and R. Heijungs, Int. J. Life Cycle Assess. **25**, 294 (2020).
[274]Semicore, Inc., "Density reference table"; see https://www.semicore.com/reference/density-reference.
[275]M. Weber *et al.*, ACS Mater. Au **3**, 274 (2023).

04 November 2024 08:02:31

© Author(s) 2024