IEEE Open Journal of the
Solid-State Circuits Society

Received 1 November 2024; revised 12 December 2024; accepted 14 December 2024. Date of publication 19 December 2024;
date of current version 9 January 2025.

Digital Object Identifier 10.1109/OJSSCS.2024.3520525

A 70-MHz Bandwidth Time-Interleaved Noise-Shaping SAR-Assisted Delta–Sigma ADC With Digital Cross-Coupling in 28-nm CMOS

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ABSTRACT This work presents a 2× time-interleaved (TI) delta–sigma modulator (DSM) analog-to-digital converter (ADC) leveraging a 6-b noise-coupled (NC) noise-shaping (NS) SAR quantizer. A novel technique to implement the noise coupling mid-quantization is presented to relax the timing bottleneck by parallelizing the operations needed for coupling. The loop filter is implemented using power-efficient, no hold-phase ring amplifiers, with an input capacitor reset presampling to reduce kickback noise in the input network. The complete ADC clocks at a sampling rate of 1.4 GS/s, which is one of the highest among all discrete-time (DT) DSM ADCs and TI NS ADCs to date, and achieves 67/72-dB SNDR/SNR over a 70-MHz bandwidth while consuming 32 mW.

INDEX TERMS Cascade-of-integrators with feedforward (CIFF), delta–sigma modulation, discrete-time (DT) analog-to-digital converter (ADC), oversampling ADC, ring amplification.

I. INTRODUCTION

TIME-INTERLEAVING is a natural choice to increase the bandwidth in data converters, as is commonly done in Nyquist converters that dominate the state of the art in high-speed and high-performance analog-to-digital converters (ADCs). While oversampling converters could benefit from an increased output rate for increased bandwidth, simply implementing time-interleaving in noise-shaping (NS) ADCs will degrade the performance due to the noise transfer function (NTF) aliasing.

While previous works, such as [1], have demonstrated delta–sigma modulator (DSM) interleaving without NTF aliasing, this relies on delay-less paths that limit the maximum achievable clock speed. Alternative and less constraining techniques exist to deal with the interleaving problem under NS, such as extrapolation and noise coupling. Extrapolation is a technique that acts as a hardware reduction of the digital block filtering, allowing alias-free time-interleaving. Practical implementations of this technique, such as [2] and [3], suffer from interleaving artifacts that lead to small achievable bandwidths. On the other hand, noise coupling presents itself as a solution by shaping the quantization noise in the aggregated frequency domain ($N_{\text{channel}} \times f_{\text{channel}}$), thus reducing the amount of aliased noise inside the band of interest. In [4], a 2×TI structure with first-order noise coupling was developed, achieving high SNDR but still at a small bandwidth, and [5] presents a mathematical description of different orders of coupling and their performances. Since noise coupling only acts in the circuit's quantizer interface, it can potentially achieve high clock speed and bandwidth.

This work is a 2× time-interleaved (TI) DSM ADC leveraging a 2×TI 6-b noise-coupled (NC) NS SAR quantizer [6]. A novel technique to implement the noise coupling mid-quantization relaxes the timing bottleneck on a 2×TI NC NS SAR by enabling the parallelization of operations and achieving higher clock speeds. The loop filter uses power-efficient no-hold phase ringamps with an input capacitor

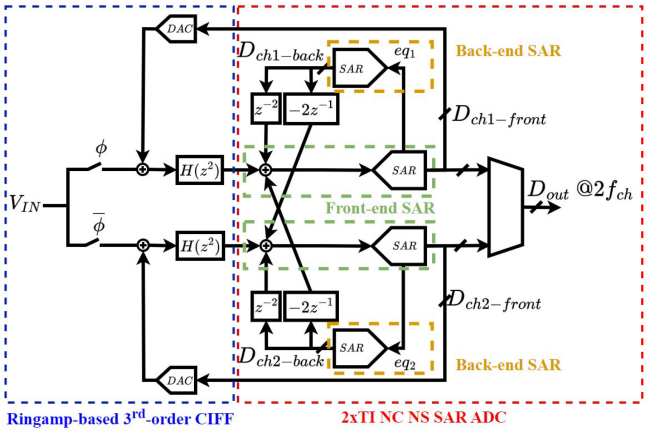

FIGURE 1. System-level description of the proposed 2×TI DSM ADC.

reset presampling to reduce kickback noise in the input network. The complete ADC is measured at a sampling rate of 1.4 GS/s, which is the highest among all discrete-time (DT) DSM ADCs and TI NS ADCs to date with linearity higher than 60 dB, and achieves 67/72-dB SNDR/SNR over a 70-MHz bandwidth while consuming 32 mW. Section II will inspect the system-level overview of the quantizer and its time-interleaving aspects. Section III describes the circuit implementation of the quantizer and the loop filter. Section IV presents the measurements, and Section V concludes this article.

II. SYSTEM-LEVEL OVERVIEW

A. TOP-LEVEL REPRESENTATION

Fig. 1 shows a top-level depiction of the full 2×TI DSM ADC. The 2×TI NC NS SAR has a front-end SAR that quantizes the output of each loop filter channel and a back-end SAR that quantizes the quantization residue (eq_1 and eq_2) of the respective front-end SAR. This information from the back-end SAR is then digitally coupled to both its channel and the other channel via the front-end SAR DAC, thus creating a second-order NS in the aggregated frequency domain ($z = e^{s/2f_{ch}}$), where $2f_{ch}$ is the TI output rate. The loop filter is a ringamp-based third-order cascade-of-integrators with feedforward (CIFF) [7].

B. TIME-INTERLEAVING IN DSM ADCS

Fig. 2 presents a more tangible argument for why there is a need for noise coupling in a time-interleaving NS structure. Take, for instance, a channel made of the third-order CIFF with input signal bypass in this work. Time-interleaving by 2 used in this work will effectively expand the first Nyquist band by 2, thus increasing the reach of the signal transfer functions (STFs), but the effect on the NTF is equivalent to a z to z^2 transform. This transformation will geometrically move the single channel poles and zeros by pushing them to the right side of the dashed black line while creating image poles and zeros on the left side. The Nyquist band expands in the frequency domain, but the NTF does not scale. In practice, the NTF is now aliased, and we cannot

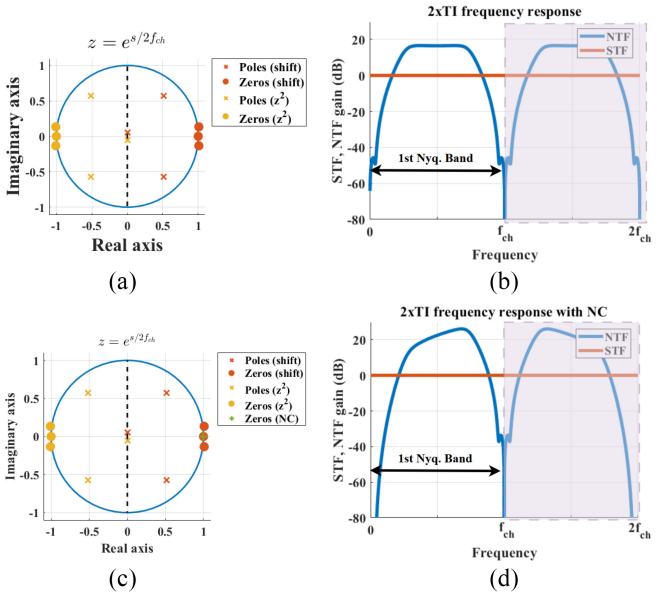

FIGURE 2. Geometric changes in poles–zeros location and frequency response changes due to time-interleaving. (a) Pole–zero location 2×TI. (b) Frequency response 2×TI. (c) Pole–zero location 2×TI with NC. (d) Frequency response 2×TI with NC.

increase the bandwidth without injecting quantization noise into it. A second-order noise coupling comes into play as it further shapes the NTF spectrum in the aggregated frequency domain ($z = e^{s/2f_{ch}}$) by adding two zeros at dc [see Fig. 2(c)] without any images at Nyquist (-1 on the unity circle). That is visible in the frequency domain as an extra shaping on the new first Nyquist band in Fig. 2(d), enabling further bandwidth increase due to the time-interleaving.

Even though noise coupling is a valid and simplified solution to increase the bandwidth, it comes with its own set of implementation challenges that can degrade the overall achieved SQNR. The speed bottleneck in this architecture is the cross-coupling path ($-2z^{-1}$) between the channels. When proper timing is allocated to all operations, the feedback path has to happen in the short nonoverlapping period between the clock phases, which could potentially degrade the system's maximum achievable clock frequency and, thus, the final bandwidth. This work solves those drawbacks with two techniques explained in the following sections: 1) mid-quantization cross-coupling and 2) digital coupling via a DAC. The first one relaxes the timing requirements for noise coupling by delaying the feedback, and the second one makes the noise coupling gain and feedback straightforward via a part of the DAC in the front-end SAR.

C. RESIDUE EXTRACTION VIA BACK-END SAR AND MID-QUANTIZATION NOISE COUPLING

Since its conception in [8], the NS SAR has gained a lot of traction as an oversampling converter that combines the power efficiency of a SAR converter with the SQNR gain of an NS structure. The fact that the SAR search naturally generated quantization residues that can be used for further signal processing was the key element that favored this combination. Many different techniques were developed

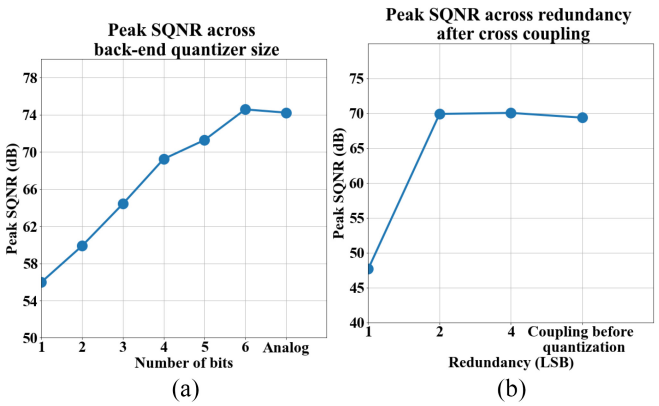

FIGURE 3. (a) Achieved peak SQNR across the number of bits of the back-end quantizer. (b) Achieved peak SQNR across the amount of redundancy after the cross-coupling moment.

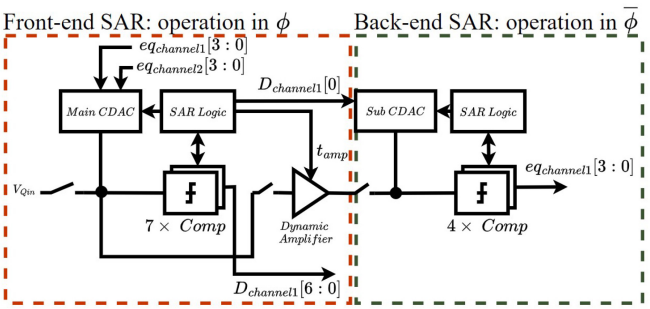

FIGURE 4. Block diagram of the proposed 2×TI NC NS SAR channel.

to enhance the architecture, mainly in two operations of the processing: 1) residue extraction (capacitor charge sharing [9] and quantization residue digitalization [10], [11]) and 2) residue feedback (passive integration [12] and multi-input comparator [13]).

To comply with the primary objective of this work, which is the extension of achievable bandwidth in DT DSM ADC, the implemented quantizer has to fit within very stringent timing requirements such that they do not become the bottleneck for clock scaling in a 2× TI structure. Aiming at hundreds of MHz of channel speed, the time allocated for quantization is minimal, which can heavily limit the amount of SAR searches that can be realized. We try to maximize the use of this time by making a series of intertwined design choices: 1) the use of a loop-unrolled SAR that minimizes the DAC logic and removes the comparator reset from the critical timing path, allowing a 6-b SAR search within the allocated time; 2) the implementation of a digital noise coupling via a back-end quantizer since the number of comparators makes the multi-input comparator unfeasible and passive integration may degrade the NTF to prohibitive values; and 3) mid-quantization noise coupling since it relaxes the timing requirements of the critical path when enough care is taken in designing the redundancy that recovers the SAR search to reachable values.

Using a back-end quantizer to digitize the quantization residue information for noise coupling will add robustness and flexibility to the NTF design. Still, it will inherently degrade the maximum achievable SQNR because of the new noise floor set by the back-end quantization. The degradation amount will heavily depend on the number of bits used in the back-end quantizer. Fig. 3(a) shows a system-level simulation of the 2×TI NC NS SAR with different sizes for the back-end quantizer and using the analog noise coupling as a benchmark (maximum achievable SQNR). In this work, the back-end quantizer was sized at 4 bits to balance a good compromise between NTF performance and time allocated to the back-end quantization.

After the back-end quantization, the cross-coupling path is ready to realize its feedback during the SAR quantization process. We use the knowledge that eq_1 and eq_2 are constrained between $\pm$LSB/2 due to the nature of the quantization noise, and given a uniform distribution of this noise, the cross-coupling signal is constrained between $\pm$LSB. That disturbance in the middle of the quantization is recovered by redundancy with weight 2 in the SAR search. Fig. 3(b) shows a top-level simulation that confirms this assumption, using a 4-bit back-end quantizer. The benchmark has the coupling happening before the quantization starts, thus not needing redundancy. The other points have the cross-coupling happening between two conversions of the same weight ($2^B \times$LSB), one being the standard from the SAR and the other being the redundant conversion. The redundancy size is 2^B in LSBs.

III. CIRCUIT IMPLEMENTATION

A. 2× TI NOISE-COUPLED NOISE-SHAPING SAR QUANTIZER

Fig. 4 shows the top-level representation of the 2×TI NC NS SAR channel. The front-end SAR is a 6-b loop-unrolled SAR with a redundant conversion with weight 2, and the back-end SAR is a 4-b loop-unrolled SAR. An open-loop dynamic amplifier (see Fig. 5) provides a linear gain of 4 between stages to prevent the quantization residue from being buried under comparator noise. This dynamic amplifier comprises two-stage *gmC* amplifiers with a pMOS input pair that benefits from the low input common mode from the front-end SAR residue. The amplification pulse's duration controls the amplifier's gain, and the capacitance difference added to the first-stage positive and negative outputs controls the offset, both points designed to cover a 3σ range of process variation. A local common-mode feedback path is added to the first stage via the resistors to decrease the gain variation concerning input common-mode variations.

Fig. 6 presents the timing for all operations. Amplification happens in parallel with the last comparison of the front-end quantizer, thus adding little to no timing degradation. That is possible because the DAC feedback from the previous comparison is moved to the back-end quantizer, performed in the nonoverlapping phase of the clock, thus not degrading the speed of the back-end quantizer either.

The DACs are implemented as in Fig. 7 in a monotonic step-down fashion [14]. It uses a bridge structure to

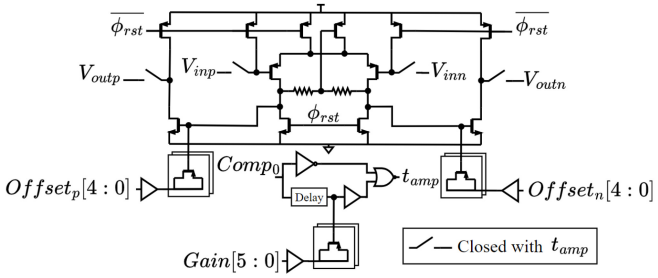

FIGURE 5. Proposed dynamic amplifier with gain and offset calibration.

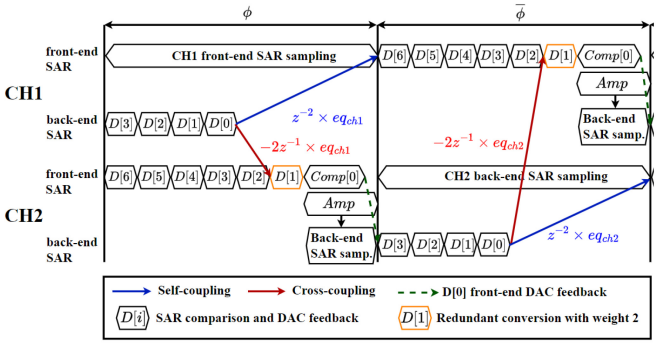

FIGURE 6. Timing diagram of the 2×TI NC NS SAR.

implement the noise-coupling capacitors. A capacitor bank is added to the noise coupling part of the bridge, adding tuning capabilities to the noise coupling gain while not degrading the SAR full scale due to the series capacitance of the bridge. This calibration helps recover from gain mismatches that may arise from the back-end SAR operation, ensuring stability and optimizing the two zero locations. A DAC averaging scheme on the first-stage CDAC is present to increase linearity. That is done by swapping the control bits at every clock phase (blue and red in Fig. 7), such that the effective capacitor value is the average of two capacitors. A bridge configuration is also proposed in the second-stage DAC. In that case, it aims to decrease the total capacitance seen by the dynamic amplifier, which relaxes its power consumption. A common-mode shift before the back-end SAR conversion helps to improve its speed even further.

With the complete picture of the implemented system, it is now possible to evaluate the noise coupling coefficient G in the quantizer NTF (1), leading to (2), where $\mathrm{LSB}_{\mathrm{back-end}}$ is the LSB step at the back-end DAC, $\mathrm{LBS}_{\mathrm{NC}}$ is the LSB step at the NC DAC, G_{dynamp} is the linear gain of the dynamic amplifier, and ΣC_X^Y corresponds to the related sum of capacitances at a specific capacitance bank X and stage Y. The bridge factors for the front-end and back-end can be calculated as in [15]. While the gain calibration of the dynamic amplifier provides the coarse matching for G, ultimately, the capacitor bank in the noise coupling DAC will optimize the zeros and lead the architecture to reach its optimum NTF. A system-level simulation on the complete 2×TI DSM ADC shows the optimized NTF's impact in the in-band noise rejection in Fig. 8(a), leading to as much as 9-dB extra noise rejection achieved from the optimal G to the unity matched G

$$\mathrm{NTF}_{\mathrm{NS-SAR}} = 1 - G \times 2z^{-1} + G \times z^{-2} \tag{1}$$

$$G = \frac{\mathrm{LSB}_{\mathrm{NC}}}{\left(\frac{\Sigma C_{\mathrm{NC}}+1}{C_{\mathrm{Bridge}}^{\mathrm{front-end}}}\right)} \times \frac{G_{\mathrm{dynamp}} \times \left(\frac{\Sigma C_{\mathrm{CDAC}}^{\mathrm{back-end}}+1}{C_{\mathrm{Bridge}}^{\mathrm{back-end}}}\right)}{\mathrm{LSB}_{\mathrm{back-end}}}. \tag{2}$$

B. RINGAMP-BASED LOOP FILTER

Fig. 9 shows the structure of the loop filter. The employed ringamps have no hold phase, meaning that they integrate their inputs to a capacitor during the amplification phase and are powered down in the subsequent phase to save power, losing their sampling phase as in traditional OTA-based switched capacitor circuits. To comply with that behavior, some modifications had to be made to the standard CIFF architecture. In particular, the distribution of delays is not performed evenly across the structure; instead, it is chosen to add an extra delay (at the input of the third integrator) and delay-less paths (from integrators 1 and 3 to the summing amplifier) to account for the no-hold characteristic. Fig. 10 shows a detailed diagram of the timing dependencies between stages. With these modifications, this structure can implement the same NTF as a traditional OTA-based design but with a potential power consumption decrease of around 50% due to power cycling.

The input capacitor uses 22 fF units, resulting in a 1.3-pF sampling DAC sized for thermal noise. Bottom-plate sampling reduces phase mismatches across the sampling paths for the binary scaled capacitors, thus increasing linearity. The signal-dependent charge in the top plate of the DAC results in disturbances for the input network when the DAC is connected at the beginning of the sampling phase, and this effect generates kickback noise. To alleviate that issue without needing a dedicated buffer, a reset phase is added before sampling to connect the top plates of the positive and negative sides, swiftly distributing the differential charge and approximately resetting all the capacitors to the common-mode reference.

The ringamps in this design are similar to the ones used in [16] (see Fig. 11). A heuristic strategy is followed based on the output capacitive load to size the amplifiers for each integrator. We start the design by sizing the output stage based on a slew time and load. From the experience with this technology [7], it is feasible to have a pure slewing phase of 150 ps for the ring amplification to balance speed and stability. Given that the output of the integrator is reset to V_{CM}, which is designed to be $V_{DD}/2$ after every integration, that eases the burden on the output stage slewing current, which leads to (3) where α is an architecture-dependent factor and is taken as a scaling factor to account for the propagation delay within the ringamp during slewing, which

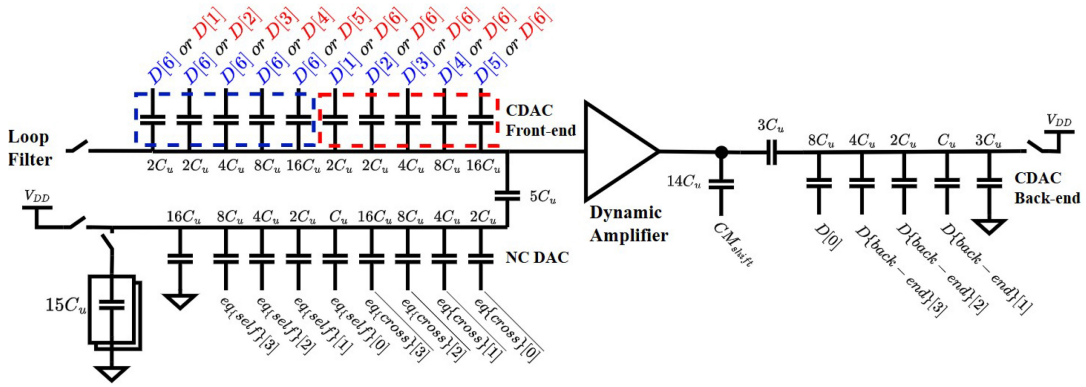

FIGURE 7. Bridge capacitor configuration of the first-stage CDAC and bridge capacitor configuration of the second-stage CDAC. $5C_u$ and $3C_u$ in series with the CDACs are the bridge capacitors for the front-end and back-end, respectively.

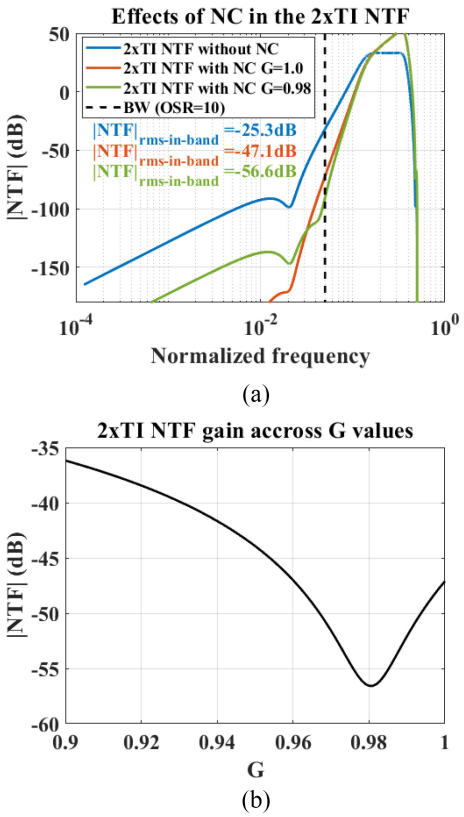

FIGURE 8. (a) Effects of the noise-coupling in a 2×TI DSM loop filter spectrum. (b) Effects on G variations in the quantization noise suppression.

in this work is empirically calculated as 1/3

$$I_{\text{slew,stg3,diff}}[A] = \frac{C_{\text{LOAD}}[F]}{\alpha \times 150p[s]} \times \frac{V_{DD}[V]}{2}. \tag{3}$$

In the same stage, the ratio between pMOS and nMOS widths is designed to give similar sinking and sourcing currents at the output, and that ratio is carried out to the other stages. After that, we size the remaining stages; the preceding second and first stages are sized to drive this output, optimizing the compromise between driving strength and parasitics such that the internal nondominant pole is pushed to higher frequencies. A good ratio that simplifies this optimum search is 2:1:1 from stages 1 to 3. That reason can be explained first by the biasing condition of each stage and slew limits. At the settling phase, the first stage is biased closer to weak inversion due to the designed common mode being at $V_{DD}/2$; thus, it requires more strength to drive the internal nodes. Due to the CMOS resistors on the first stage boosting the bias of the second stage to a stronger inversion, the sizing there can be slightly relaxed, reducing parasitic capacitances. The CMOS resistors that generate the deadzone for the third stage have the opposite effect; they weaken the inversion level of the last stage to stabilize the system when settling. Having the last stage be equal in size to the preceding stage was empirically found to be an excellent compromise to prevent the internal nodes from slewing before the output stage. Finally, a PSS/PNOISE simulation with the integrator testbench is run to validate the noise levels of the amplifiers.

Following this approach, the first integrator ratio had to be changed to achieve the target noise floor. This significantly increases its size and adds parasitic capacitance to the virtual ground node (around 100 fF). The integrator topology implemented in this design is parasitic insensitive from a transfer function perspective. Thus, the main design effort is mainly in the driving capability of the amplifier that should accommodate this extra load. The optimized ringamp sizing is present in Table 1. Note that while we aggressively scale stages 2 and 3 without significantly impacting the overall noise performance, the summing stage hits a scaling limit due to the quantizer capacitance it has to drive and the multiple capacitances from the different stages that increase its loading.

C. COMPARATOR AND DYNAMIC AMPLIFIER CALIBRATION

Some foreground calibrations had to be implemented to prevent degradation of SQNR, mainly to compensate for the comparator offset, dynamic amplifier gain, and dynamic amplifier offset. To calibrate for comparator offset, we use split source comparators [17]. That allows for offset

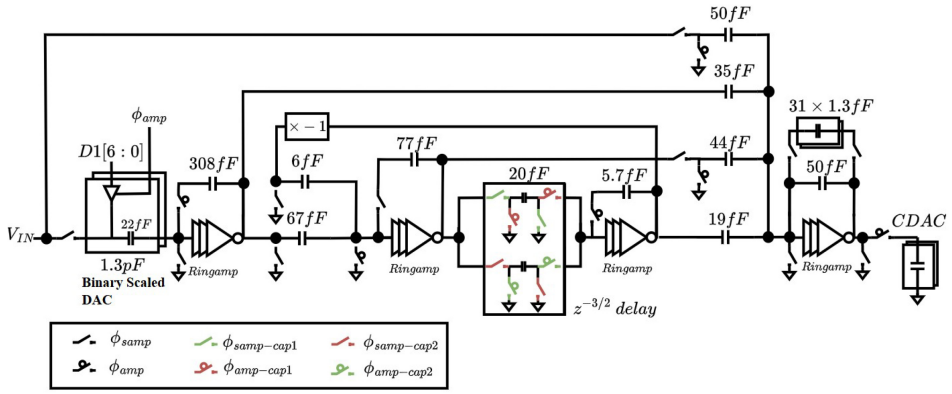

FIGURE 9. Loop filter top-level description (single-ended representation).

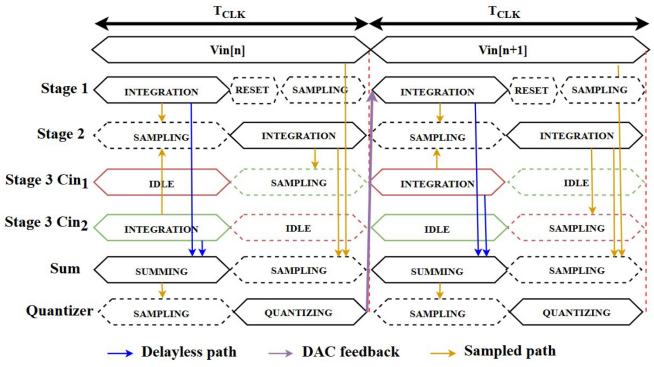

FIGURE 10. Timing dependencies across a single-channel loop filter.

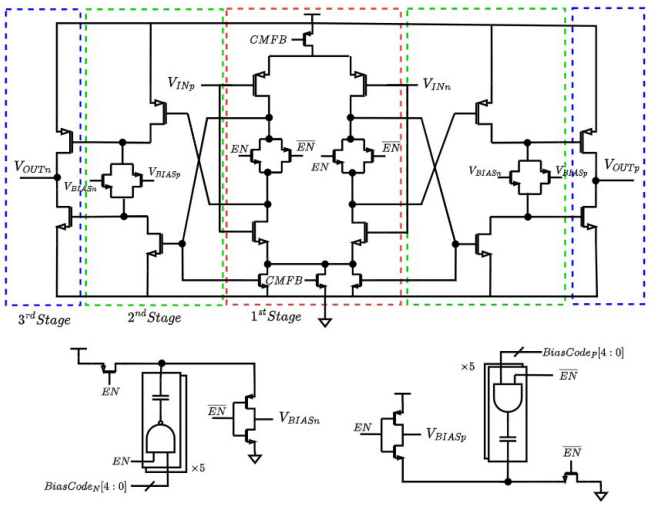

FIGURE 11. Schematic of the ringamp used in the second and third stages and summation node. In the input stage, the bias DAC is removed, and that node is tied directly to a pad for testing purposes.

correction with little to no increase in the comparison time versus the standard design [18].

Each comparator in the loop-unrolled structure is foreground calibrated at its appropriate CM level to emulate the voltage condition from the step-down DAC. Tri-state gates

TABLE 1. Sizing of ring amplifiers for all stages.

	Amplifier stage	1^{st}	2^{nd}	3^{rd}
Integrator 1	$W_{PMOS}(\mu m)$	274.6	6.24	6.24
	$W_{NMOS}(\mu m)$	237.6	5.4	5.4
	$A_V^*(dB)$	49		
	$I_{slew,stg3,diff}(mA)$	9		
Integrator 2	$W_{PMOS}(\mu m)$	1.84	0.92	0.92
	$W_{NMOS}(\mu m)$	1.6	0.8	0.8
	$A_V^*(dB)$	46		
	$I_{slew,stg3,diff}(mA)$	1.5		
Integrator 3	$W_{PMOS}(\mu m)$	1.38	0.69	0.69
	$W_{NMOS}(\mu m)$	1.2	0.6	0.6
	$A_V^*(dB)$	46		
	$I_{slew,stg3,diff}(mA)$	1		
Summing	$W_{PMOS}(\mu m)$	4.16	2.08	2.08
	$W_{NMOS}(\mu m)$	3.6	1.8	1.8
	$A_V^*(dB)$	46		
	$I_{slew,stg3,diff}(mA)$	3		

* DC gain is the small signal gain at zero differential input

control the DAC's bottom plate to enable the calibration and MSB averaging modes (see Fig. 12). The common mode is changed after every comparison using the *VALID* signal from the comparators, which are generated by a XOR operation of the output and the inverted output of the latch. The variations in the common mode for the last two comparisons of the front-end SAR are small enough that they use the same common-mode value to calibrate for comparator offset. The same procedure is done for the back-end comparators, where the input common mode will be generated by shorting the dynamic amplifier outputs after amplification. The small common-mode variation is also valid for the back-end SAR due to the small step sizes of the DAC. Thus, the DAC drivers are just disabled using an AND operation on its path.

After the comparator calibration and still in the foreground, the gain and offset of the dynamic amplifier are calibrated by applying an offset voltage equal to an LSB step in the front-end SAR DAC just before the amplification.

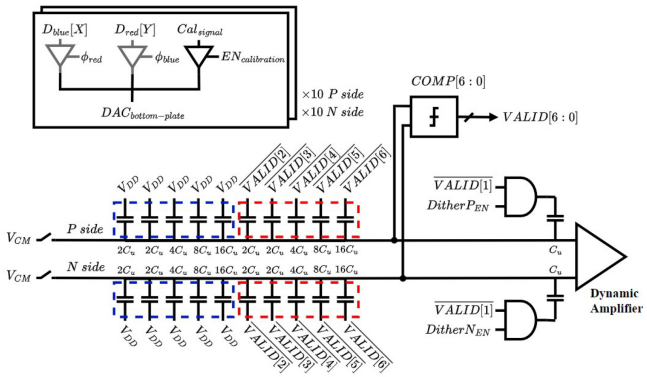

FIGURE 12. DAC configuration for calibration of comparator offset.

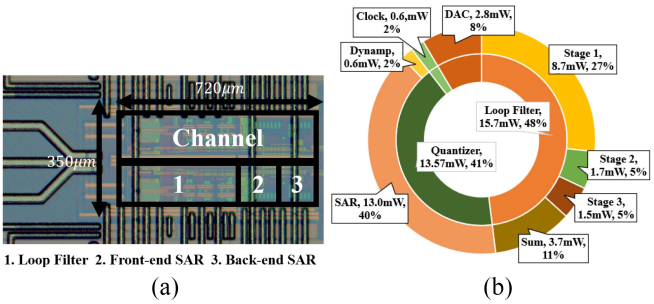

FIGURE 13. (a) Die photograph describing the top-level blocks and dimensions. (b) Doughnut chart showing the measured power breakdown (inner circle) and overplayed with an estimated power consumption per component (outer circle).

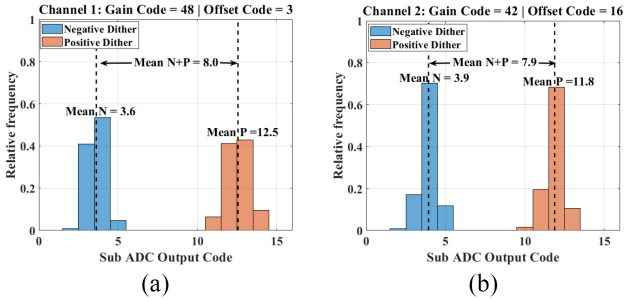

FIGURE 14. Histogram curves for a set of dynamic amplifiers in a sample board showing the concurrent calibration of gain and offset. (a) Channel 1—Dynamp. (b) Channel 2—Dynamp.

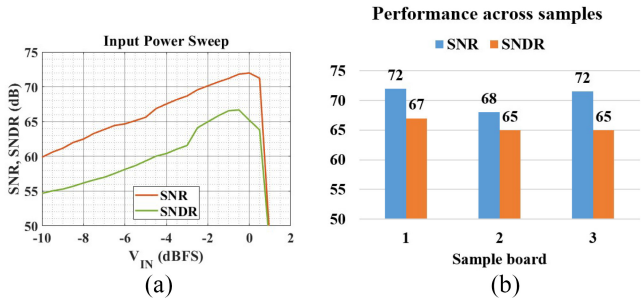

FIGURE 15. (a) Peak SNR and SNDR for sample 1 close to the maximum stable amplitude. (b) Peak SNR and SNDR achieved across samples.

It can be either positive (controlled by DitherP_{EN}) or negative (controlled by DitherN_{EN}) and the quantization of this voltage by the back-end SAR gives information on the amplifier parameters.

IV. MEASUREMENT RESULTS

The ADC was fabricated in 28-nm CMOS technology with a core area of 0.72×0.35 mm^2, as shown in Fig. 13(a). An on-chip per-channel serializer was designed to provide full rate capture of the two channels' output via a dedicated FPGA. Still, a post-tapeout PEX validation showed some timing problems in the timing of the MUX tree, limiting the speed to 6.4 Gb/s instead of the intended 8 Gb/s. With 7-b data and 1-b parity bit without encoding, the maximum achievable rate of the serializer in measurement was 5.6 Gb/s (1.4 GS/s on the ADC), rendering the actual speed limit of the core ADC unknown.

Fig. 13(b) shows the power breakdown. As explained in the previous sections, foreground calibration was performed in the comparator offsets first, and then in the dynamic amplifier. The dynamic amplifier was calibrated for offset and gain concurrently since those two dimensions are not orthogonal; thus, their codes interfered in each other results. The calibration codes were swept until a histogram like the one in Fig. 14 could be plotted for a calibrated sample. The amplifier calibration could also be done with a free-running ADC with noise coupling and dither signals disabled. In this case, the code distribution should reflect the quantization residue distribution which is uniform between all codes for a correctly calibrated and bounded design. Too much gain would increase the frequency of high and low codes, not enough gain would reduce the frequencies of high and low codes. Offsets would shift the center of the histogram for one direction or the other depending on the polarity. This also converged to optimal codes where the difference to the foreground calibrated code in the SQNR could not be measured since it was way below the thermal noise floor.

Fig. 15(a) shows the performance of a calibrated sample across the input power sweep near the MSA, achieving a peak performance of 72-dB SNR and 67-dB SNDR over a 70-MHz bandwidth. Fig. 15(b) shows the peak performance across different samples using the same calibration codes for the loop filter, indicating the robustness of the DT loop filter and the ringamps across die-to-die variations. A zooming out from the performance close to the MSA shows a different behavior than expected. As it can be seen in Fig. 16, there is a change in the performance slope at smaller input amplitudes, leading to a smaller achievable dynamic range (distance between the 0-dB SNDR crossing point and 0 dBFS). The DAC averaging causes this effect, and it is conjectured as follows: at higher input amplitudes, the input signal power surpasses the high-frequency noise and provides multiple consecutive cycles of MSB equal to 0 or 1; this enables a true averaging since the capacitor banks will swap every other cycle to generate that stream of equal sign. At smaller amplitudes, the broadband quantization noise takes

TABLE 2. Comparison with state-of-the-art TI NS ADCs.

	This work	K. Lee [4]	D. Jiang [2]	L. Jie [13]	C. Lin [19]	T. Caldwell [20]	S. Lee [21]
Architecture	**2xTI DT DSM**	2xTI DT DSM	4xTI DT DSM	4xTI NS-SAR	2xTI NS-SAR	2xTI CT DSM	2xTI CT DSM
Node	**28nm**	$180nm$	$28nm$	$40nm$	$22nm$ $FDSOI$	$180nm$	$28nm$
Power (mW)	**32**	28	23.1	13	2.5	103	6.4
Sampling Rate (MS/s)	**1400**	100	520	400	640	400	500
OSR	**10**	12	208	4	4	10	16
Bandwidth (MHz)	**70**	4.2	5	50	80	20	15.625
$SNDR$ (dB)	**67**	79	86.1	70.4	66	49	81.6
SNR (dB)	**72**	81	89	71	67	49.7	84
DR (dB)	**64[1]/70[2]**	81	90	71.7	67	55.2	84.8
FoM_{S-SNDR} (dB)	**160.1**	160.8	169.5	166.3	171.2	131.9	175.5
FoM_{S-DR} (dB)	**160.4[1]/163.4[2]**	162.8	173.4	167.6	172.2	138.1	178.7
FoM_W $(fJ/c.s.)$	**143.2**	480	159.1	48.1	9.48	12095.2	23.5

[1]Measured value with DAC averaging ON, [2]Peak value with DAC averaging OFF

FoM_S = (SNDR or DR) – 10*log10(Power/BW); FoM_W = Power/((2*BW)*2^(ENOB))

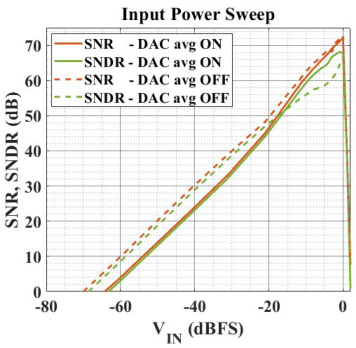

FIGURE 16. Measured performance sweep with DAC averaging ON and OFF showing the linearity and dynamic range tradeoff.

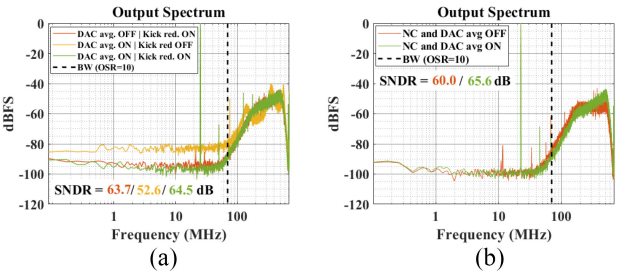

FIGURE 17. Sample 16k points FFT with 8× averaging showing the effects of (a) kickback noise reduction and DAC averaging, and (b) noise-coupling and DAC averaging.

over and creates a condition where the MSB value can switch every cycle. As the capacitor bank changes every other cycle, in this condition, the mismatches are not appropriately averaged, but rather, they create mixing conditions that raise the noise floor, decreasing the SNR and DR when below −20-dBFS input.

Fig. 17(b) presents the effect of noise coupling and DAC averaging in the spectrum when the input amplitude is close to MSA, adding almost 1 extra bit of resolution. It is seen that the DAC averaging reduces the in-band noise by virtually increasing the matching of the input DAC and the quantizer DAC. Implementing kickback noise reduction in the loop filter input DAC also shows more significant performance improvement [see Fig. 17(a)] in the measurements than was predicted by simulations, most likely due to the simplified modeling of the input network used in the simulation, which was also differentially matched. The measured peak SNDR is smaller than predicted, mainly due to an increased HD2 tone arising from the not sufficient gain of the common-mode feedback loop. The SNR is smaller because the increase in the size of the first ringamp of the first integrator also increased the amount of parasitic coupling to the virtual ground of that integrator, degrading the integrator transfer function. The sweep of the noise coupling factor (G) in the measurements had little impact on the performance since SQNR was designed to be 12 dB below the thermal noise level, thus rendering the fine-tuning of the NTF undetectable.

The prototype achieves $\text{FoM}_{S-\text{SNDR}}$, FoM_{S-DR}, and FoM_W of 160.1 dB, 160.4 dB, and 143.2 fJ/c.s., respectively. Table 2 compares this design with the state-of-the-art TI oversampling ADCs. Fig. 18(a) shows the design achieves one of the highest bandwidths for a DT DSM ADC or TI NS ADC and, at an OSR of 10, the highest sampling rate by a factor of 2× for designs with over 60 dB of linearity.

V. CONCLUSION

This work successfully showed the design of an NC NS SAR-assisted TI delta–sigma ADC and its measurement. It offered an alternative to implement noise-coupling such that

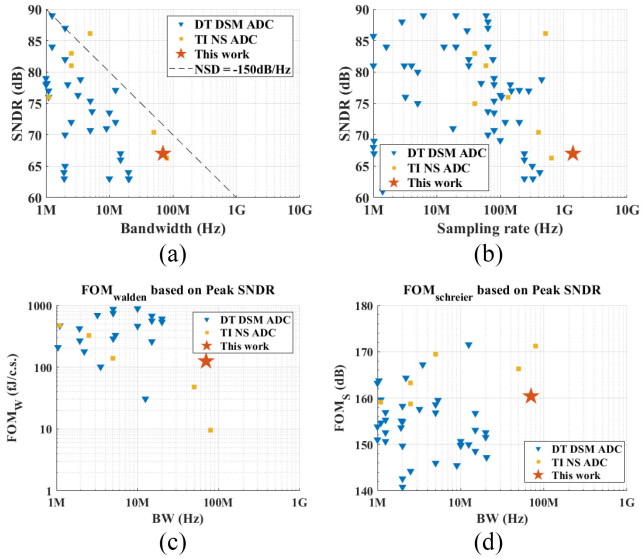

FIGURE 18. Plotting of this work performance in comparison with similar architectures in the state of the art in [22]. (a) SNDR versus bandwidth. (b) SNDR versus sampling rate. (c) Walden figure of merit. (d) Schreier figure of merit.

it does not degrade the timing and maximizes the sampling rate and bandwidth. Ringamps are still a main component in achieving high efficiency at stringent noise requirements. Mid-quantization digital noise coupling was developed to increase robustness and prevent timing degradation in the DT DSM ADC quantizer. Calibration techniques were implemented in the quantizer without adding more propagation delay to the critical paths and enabled a near-running mode condition for robust calibration code convergence. And finally, the loop filter implementation with no hold amplifiers that are turned off for power savings and suitable for GHz range clocking speed. Despite the successful measurements, a gap still exists between them and the simulations that could be recovered in a future implementation. Modifications in the data acquisition, the clock paths, and the first integrators could help increase the maximum sampling rate and SNDR to the expected values. Circuit-level techniques to reduce the noise of the first amplifier with higher efficiency would also significantly impact the complete ADC power efficiency.

ACKNOWLEDGMENT

The authors would like to acknowledge the help of L. Pauwels, H. Suys, S. van Winckel, A. Parisi, N. Marculic, A. Cooman, and A. Dewilde for support with tests and measurements, and the support of Europractice in providing design tools and MPW fabrication services.

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