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Understanding the Slow Erase Operation in IGZO-Channel FeFETs: The Role of Positive Charge Generation Kinetics

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ABSTRACT This work systematically investigates the programming and erasing dynamics of IGZO-channel back-gated FeFETs, uncovering that erase operation is significantly slower than programming. PUND measurements in ferroelectric capacitors with IGZO top electrodes reveal that the ferroelectric switching kinetics under negative bias are limited by the generation of positive charges. Two underlying physical mechanisms are identified: (1) IGZO-bandgap donor states, which can get positively charged by emitting electrons to Conduction Band and reversibly neutralized during programming, help ferroelectric switching and limits the switching kinetics; and (2) hydrogen doping into IGZO, which proceeds at a much slower rate and is irreversible, thus incapable of supporting ferroelectric switching. This work emphasizes the importance to deepen the understanding of erasing kinetics to enable low-latency, and high-endurance applications of oxide-semiconductor-channel FeFETs.

INDEX TERMS IGZO, oxide semiconductor, ferroelectric, HZO, switching kinetics.

I. INTRODUCTION

Since the discovery of ferroelectricity in doped HfO_2 material [1], the Ferroelectric Field-Effect Transistor (FeFET) has gained significant research interests due to its CMOS-compatibility, low writing energy, and high compatibility with monolithic 3D integration. Unlike the 1T1C Ferroelectric Random Access Memory (FeRAM), which suffers from the drawback of destructive readout, FeFET offers not only a simpler memory cell with only 1-Transistor (1T) structure but also Non-Destructive Read-Out (NDRO). These advantages make FeFETs a promising candidate for the low-power, high-density Non-Volatile Memories (NVMs) [2], as well as energy-efficient Compute-in-Memory applications.

In Si-channel FeFETs, the significant charge trapping into a SiO_2 interlayer between ferroelectric (FE) and Si channel plays an important role in balancing the huge ferroelectric polarization (P_{FE}) [3]. Not only does this low-κ SiO_2 interlayer result in a depolarization field and voltage loss [4], the charged interface states also screen the polarization and result in endurance degradation [5]. These limitations have driven interest in FeFETs with Oxide Semiconductor (OS) channels, such as InGaZnO (IGZO) [6], [7], InWO (IWO) [8], InZnO (IZO) [9], and In_2O_3 [10]. By eliminating the SiO_2 interlayer, OS-channel FeFETs achieving significantly higher endurance has been extensively reported [7], [9], [10].

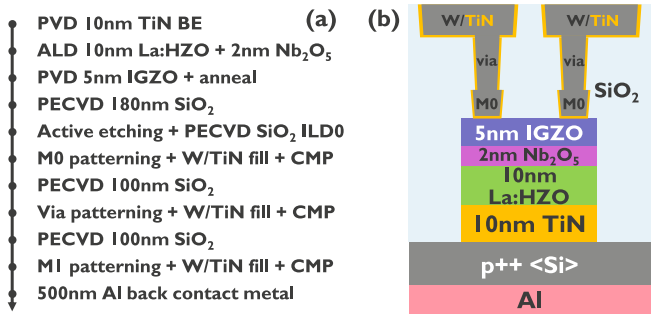

FIGURE 1. Process flow (a) and device structure (b) of the IGZO-channel BG FeFETs in this work.

Despite these advancements, the switching mechanisms of OS-channel FeFETs remains to be unclear. To meet the charge-balance condition, during the erase operation, in which a negative V_g is applied to switch P_{FE} to a negative state, resulting in a higher-V_{th}, sufficient amount of positive charges in the channel side is needed to support the negative P_{FE}. While in the in wide-bandgap OS materials, the lack of holes make this process inherently difficult [3], [11].

This work aims to address the asymmetric programming/erasing operation, with a special focus on the switching dynamics of the erase operation in IGZO-channel FeFETs. Using FeFET devices fabricated on 300-mm wafers, we firstly evaluate the writing performance by implementing Incremental-Step-Pulse Programming and Erasing measurements on FeFETs. To further understand the slower erasing kinetics, we extend our analysis to ferroelectric capacitors with IGZO top electrodes, enabling a direct examination of the charges that are generated during negative erasing pulses. These investigations reveal the underlying mechanisms governing ferroelectric switching kinetics in IGZO-channel FeFETs.

II. DEVICE FABRICATION

IGZO-channel Back-Gated (BG) FeFETs were fabricated in 300-mm wafer platform. A 10-nm TiN layer was deposited on top of p^{++} Si substrate as the bottom electrode, followed by an ALD-grown 10-nm La-doped HfZrO (La:HZO) ferroelectric layer and a 2-nm Nb_2O_5 capping layer. As it is reported in our recent publication [12], Nb_2O_5 interfacial engineering is crucial to facilitate the Tetragonal-to-Orthorhombic phase transformation and improve the memory window.

Afterwards, a 5-nm IGZO layer was deposited as both channel layer and ferroelectric top electrode, and was then annealed in Oxygen ambient at 350°C for 1 hour to crystallize the ferroelectric phase. Active etching and SiO_2 Interlayer Dielectric (ILD0) deposition were then taken to form the mesa. After the Metal-0 (M0) patterning and ILD0 etching, TiN and W were deposited and thinned down by CMP to form the contact with IGZO channel. Then the Via was patterned and filled with W/TiN to be connected with the M0 S/D regions, followed by W/TiN Metal-1 (M1) contact pad deposition and CMP. Finally, 500-nm Aluminum was formed on the backside to serve as back gate contact.

III. RESULTS AND DISCUSSION

A. PROGRAMMING AND ERASING CHARACTERISTICS ON IGZO-CHANNEL FEFETS

Incremental Step Pulse Programming (ISPP) and Incremental Step Pulse Erasing (ISPE) measurements were taken on the fabricated IGZO-channel FeFETs, after the device was woken up as described in [12]. The measurement pulse trains, shown in Fig. 2 (a), are applied to the back gate. Before the ISPP/ISPE writing pulses, a reset pulse of either $-4V/500\mu s$ or $+4V/1\mu s$ is firstly applied to preset the FeFETs into erased or programmed state, respectively. After incremental program/erase pulses, fast $I_d - V_g$ measurements featured with $40\mu s$ settling time and $2\mu s$ averaging time per V_g step are applied to detect the V_{th}. The $I_d - V_g$ sweeps are limited within a short range, starting from $V_g = +1V$ and ending with $V_g = -1V$ to prevent the potential read disturb to the programmed state, as is reported in our recent work [12].

The $I_d - V_g$ curves obtained from ISPP measurement are shown in Fig. 2 (b): V_{th} becomes lower with both larger programming voltage (V_{PRG}) and longer programming pulse width (t_{PRG}). Thanks to the elimination of the low-κ interlayer (i.e., SiO_2 in Si FeFETs), low-voltage ($<= 4V$) and short-duration ($< 1\mu s$) programming is shown to be possible for IGZO-channel FeFETs. Although going to very high programming voltage ($> 4V$) and long programming time ($> 10\mu s$) can push the V_{th} to even lower value, this ultra-low V_{th} is believed to be an extrinsic V_{th} negative shift related to hydrogen under positive bias stress, which is a known reliability issue in IGZO transistors [13].

However, the ISPE results, in Fig. 2 (c), show that the erase operation is more difficult. It could be seen that the erased high-V_{th} is highly dependent on the erasing pulse width (t_{ERS}), while almost not changing with the erasing voltage (V_{ERS}). If the V_{th} after program and erase are compared with respect to different writing pulse width, as is shown in Fig. 2 (d), it is found that the Memory Window (MW) is significantly dependent on the erasing pulse width. Only when the erasing pulse is no shorter than $100\mu s$, a saturated MW of 0.5V can be obtained.

B. UNDERSTANDING THE ERASE TIME DEPENDENCE BY PUND MEASUREMENT IN FECAPS WITH IGZO ELECTRODE

To deeply understand the mechanisms behind the difficulty of erasing in IGZO-channel FeFETs, we further studied the FE polarization switching kinetics from FE polarization reversal measurements. The measurements for the subsequent sections are conducted on IGZO-top-electrode Ferroelectric capacitors (FeCAPs), featuring the same TiN/La:HZO/Nb_2O_5/IGZO gate stack as our fabricated FeFETs but in a capacitor configuration, as shown in Fig. 3 (a). This one-dimensional (1D) structure allows a simplified charge-sheet approximation, providing clear insight

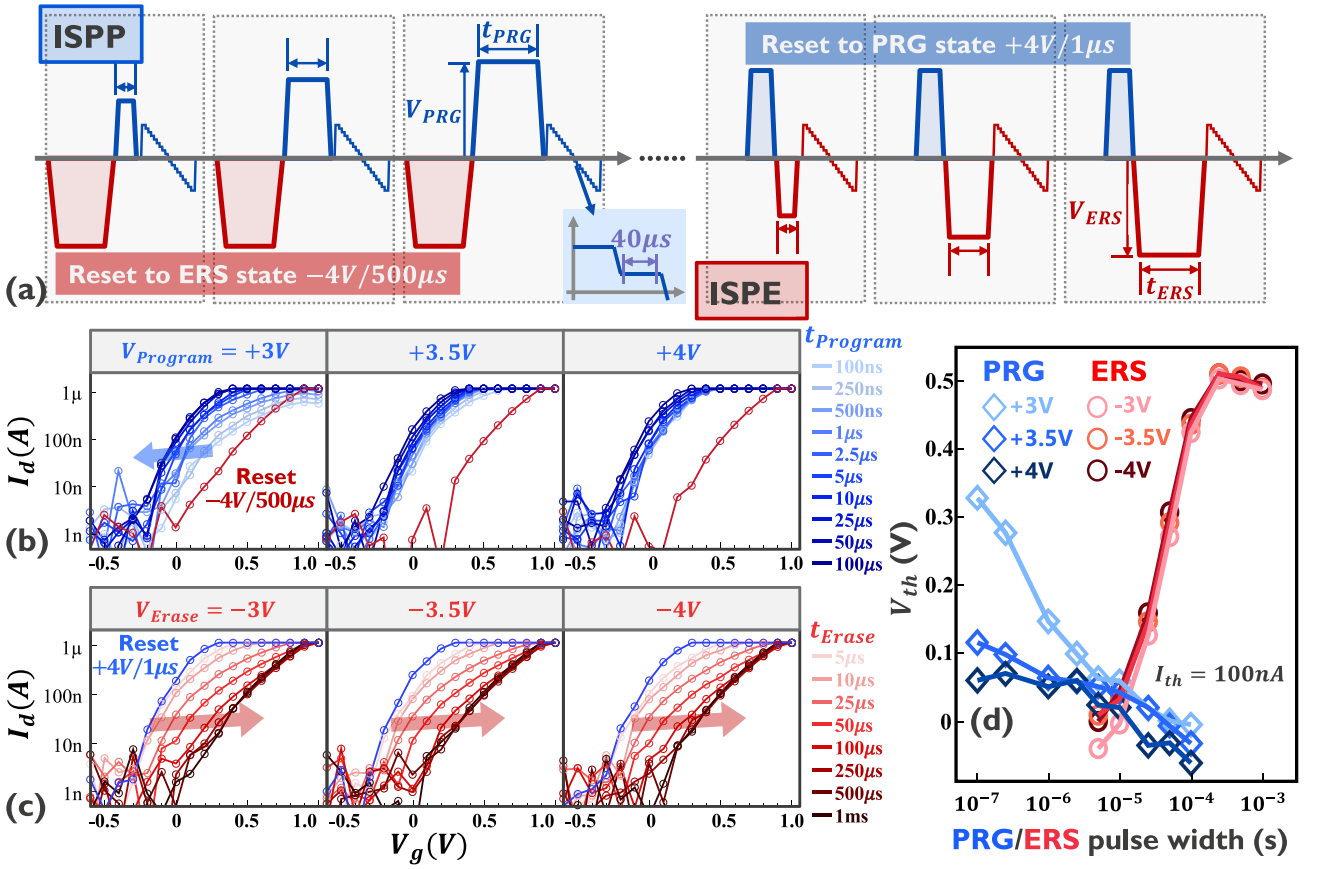

FIGURE 2. (a): Measurement waveforms applied to the BG during ISPP/ISPE measurements. (b), (c): I_d-V_g curves from ISPP and ISPE measurements. The amplitudes of program and erase pulses are denoted on top of each plots, while the pulse widths are distinguished with different colors. Faster programming operation ($< 1\mu s$) can be achieved by increasing the program voltage. While the erased high-V_{th} is always slowly increasing when a longer erase pulse is applied, and almost independent on the erase voltage applied. (d): An MW $> 0.4V$ can only be obtained when the erasing pulse width is no less than $100\mu s$.

into FE switching behavior under the source/drain regions. Although the FeFETs operate in a two-dimensional (2D) regime, with non-uniform fields and fringing effects from the source/drain, the FeCAP measurements still effectively capture the essential polarization dynamics.

The measurement waveform, which is generated by an arbitrary waveform generator and applied on the back gate, is composed of Reset, Writing, and then Reading pulses, as shown in Fig. 3 (b). After reset pulses of either $-4V/500\mu s$ or $+4V/1\mu s$ to switching back the ferroelectric polarization states, writing pulses with incrementally increased voltage and pulse width are then applied. After writing pulses with a positive gate bias, the reading stage is composed of Negative-Down-Positive-Up (NDPU) pulses; While after negative-bias writing pulses, reading pulses are Positive-Up-Negative-Down (PUND), in which the Positive (P) and Negative (N) pulses detect the total current (I_{total}) consisting of both Ferroelectric switching-only current (I_{SW}) and non-switching displacement current (I_{nsw}), while during Up (U) and Down (D) pulses only the non-switching current is measured. All of the reading pulses are triangular waveforms with a rising time of $40\mu s$ (i.e., frequency is 6.25kHz).

The measured I-V curves , from NDPU or PUND pulses, with respect to the writing pulse width are shown in Fig. 3 (c), with the writing voltage fixed to be $+4V$ or $-4V$. Upon applying positive writing pulses, which corresponds to the programming operation in FeFETs, the switching current is not increasing with longer writing pulse width, provided that the voltage is high enough ($+4V$). This indicates that the ferroelectric polarization is already saturated. However,for the negative writing pulses (corresponding to the erase operation), the switching current keeps increasing versus writing time, despite of the high negative writing voltage ($-4V$). Worth to note that the non-switching current is not increasing, indicating that the increased current is due to more switchable ferroelectric domains rather than any increase of leakage current.

The opposite-state switching-only polarization reversal ($\Delta P_{SW,os}$) can be calculated by:

$$\Delta P_{SW,os} = \frac{dt}{dV} \int_0^{\pm 4V} (I_{total} - I_{nsw})\, dV \tag{1}$$

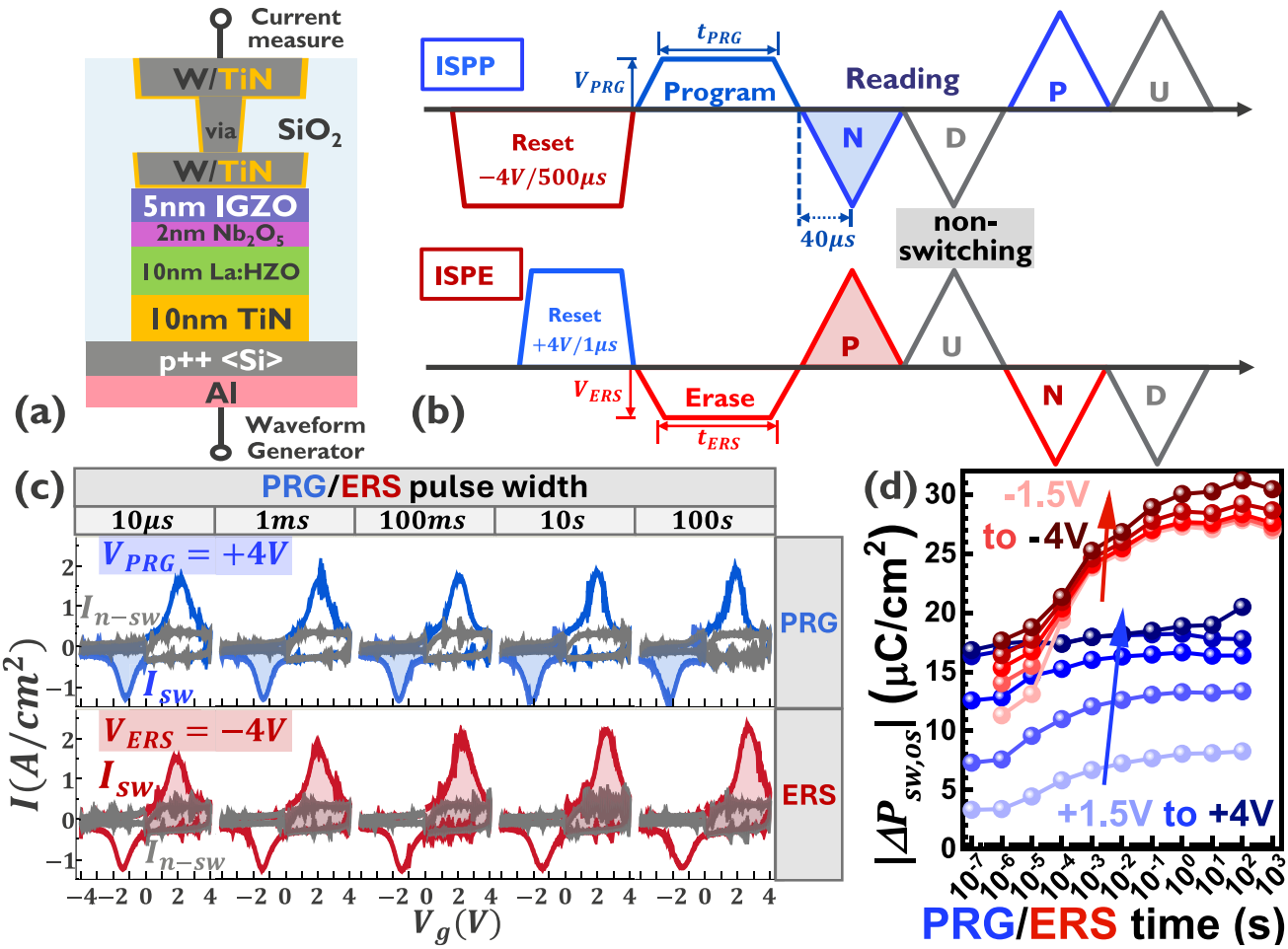

FIGURE 3. (a): Ferroelectric polarization switching is measured on FeCAPs with TiN/La:HZO/Nb_2O_5/IGZO stack. (b): Pulse waveforms applied to detect the opposite-state polarization reversal ($\Delta P_{SW,OS}$) as an indication of how much FE polarization can be flipped by the writing pulses with different pulse amplitude and width. (c): After a longer programming pulse with $V_{PRG} = +4V$ that is high enough to switch the dipoles, the FE switching current is saturated. However, a longer erasing pulse always results in a stronger FE switching current, suggesting non-saturated polarization switching. (d): The switchable $|\Delta P_{FE}|$ versus programming pulse V_{PRG} and t_{PRG} shows the NLS behavior; whereas after erase, the significantly increased $|\Delta P_{FE}|$ with longer erasing time indicates that the FE layer works in subloop, and can be switched to a more $-P_{FE}$ value with much longer erasing time.

where the I_{total} are measured from the first switching-pulses (P, and N), while the I_{nsw} are measured from the non-switching pulses (U, and D).

The dependence of $|\Delta P_{SW,os}|$ versus different write voltage and pulse width is shown in Fig. 3 (d). With positive writing voltage applied, the $|\Delta P_{SW,os}|$ shows the typical NLS behavior [14] with increased V_{PRG} and t_{PRG}. A saturated $|\Delta P_{SW,os}|$ of about $17\mu C/cm^2$ can be achieved after short programming pulses with an amplitude of +4V.

However, when erasing pulses with negative writing voltage are applied, the dependence of $|\Delta P_{SW,os}|$ versus the writing voltage and time no longer follows the NLS behavior. For one aspect, the $|\Delta P_{SW,os}|$ increases significantly with a longer erasing time, and this trend is almost independent of the erasing pulse amplitude. For another aspect, after a long erasing pulse, the detected $|\Delta P_{SW,os}|$ significantly exceeds the saturated polarization reversal of $17\mu C/cm^2$, which is obtained from the ISPP measurements with positive writing voltages.

These experimental observations suggest that in the Ferroelectric capacitors with IGZO electrode, the ferroelectric switching usually works in a sub-loop, because the IGZO channel is not capable of providing sufficient positive charges to balance the negative Saturated Polarization ($-P_S$) of La:HZO. Only when a long erasing pulse ($> 100\mu s$) is applied, additional positive charges are generated in IGZO, so that a more negative ferroelectric polarization can be achieved, and thus a more negative voltage can be dropped in Ferroelectric layer. This result is also aligning with the long erasing pulse width required for IGZO-channel FeFETs in Section III.A.

Fig. 4 shows the Polarization-Voltage (P-V) loop after erasing pulses with different erasing time. The erasing voltage is fixed at −4V, which is also the starting point of the triangular pulse for detecting the polarization (with the schematics shown in the inset). When the V_g is swept from $-4V$ to $+4V$, the ferroelectric polarization reversal (ΔP_{FE}) is significantly increasing with the writing pulse width.

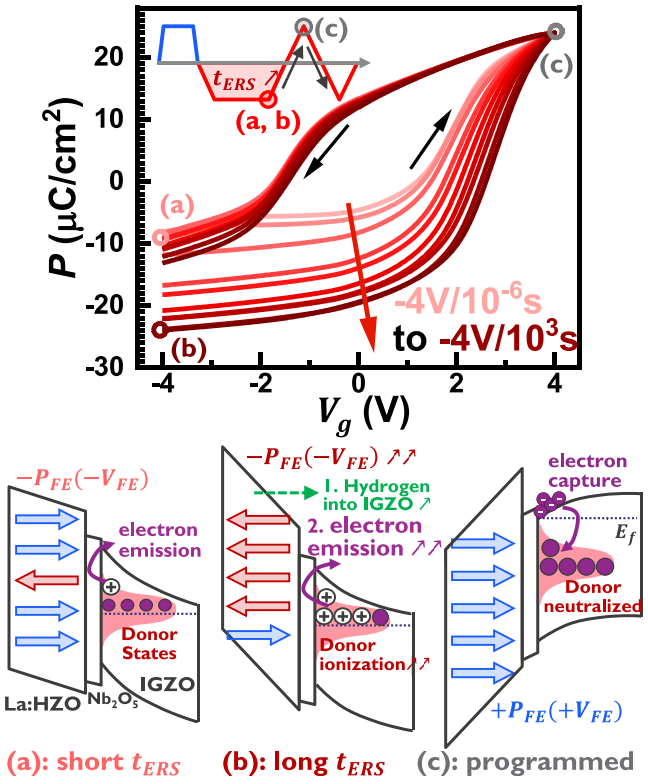

FIGURE 4. P-V loops measured on IGZO-capped FE capacitors after longer erasing pulses ($1\mu s$ to 1000s) with a fixed erasing voltage of $-4V$. (a): During short erasing pulse, only a small fraction of donor states can be ionized and become positively charged, resulting in an insufficiently erased state with a less negative P_{FE}. (b): When the erasing pulse width is increased to 1000s, a much more negative P_{FE} can be reached due to more ionized donor states, as well as Hydrogen ion drift from gate oxide into IGZO. (c): When switched back from erased to programmed state, CB electrons get re-captured by the ionized donor states, and the ΔP_{FE} represents how much additional positive charges get generated during erasing and then re-filled during reading.

This erasing-time-dependent ferroelectric switching can be well explained by the mechanisms of IGZO donor state ionization that was reported in our recent work [15], in which we proposed that, despite the hole scarcity in IGZO material, the donor states in IGZO can become positively charged by emitting electrons into Conduction Band (CB) and then balance the negative P_{FE}.

When IGZO is depleted due to a negative V_g, under the thermally equilibrated state, the donor states above the Fermi Level (E_f) should be empty according to the Fermi-Dirac distribution. However, the electron emission time constant can be quite long due to the deep energy level of IGZO donor states from its CB edge [16]. Within a short erasing pulse, only a small portion of donor states can get ionized as the system is in a non-equilibrium state (shown in Fig. 4 (a)). With very limited positive charges available to support the negative P_{FE}, FE layer voltage drop (V_{FE}) is so small that some domains are not switchable. As a result, ferroelectric layer works in a sub-loop, with a limited value of switchable ΔP_{FE} from $V_g = -4V$ to $V_g = +4V$.

With the erasing pulse width increased up to 1000s, the IGZO layer is in a depleted state for a longer time, so that more electrons will be emitted from the donor states into CB to further approach towards the thermally equilibrated state. More positive charges generated by this donor ionization process can balance more negative P_{FE}, so that a much more negative V_{FE} can be achieved to flip more FE domains into erased state. When the V_g is swept from $-4V$ to $+4V$, accumulated electrons in IGZO CB are then captured and neutralizing the donor states in IGZO bandgap (Fig. 4 (c)). Consequently, the ΔP_{FE} from this "sufficiently erased state" (Fig. 4 (b)) to the programmed state (Fig. 4 (c)) is much larger than that from the "insufficiently erased state" (Fig. 4 (a)).

Overall, the significant erasing-time dependence of the ferroelectric polarization reversal measured in Ferroelectric capacitors with IGZO electrode aligns quite well with the ISPP/ISPE measurement results in Section III.A, and it provides an in-depth insight into the physical origins of the time-dependent erasing performance.

However, it's worth to note that during the long negative writing pulses, despite that no gate leakage increasing is seen in the non-switching current curves, the ion drift from gate oxide into IGZO layer can still happen, as shown in the schematics of Fig. 4 (b). Once more positive ions are injected into IGZO, it will also balance the negative P_{FE} by acting as positive fixed charges. This will be discussed in the next Section III.C.

C. DECOUPLING THE DONOR IONIZATION AND HYDROGEN INJECTION UNDER NEGATIVE BIAS STRESS

Previous researches have attributed the Negative-Bias-Temperature Instability (NBTI) of IGZO transistors to the Hydrogen doping process. During Negative Bias Stress (NBS), protons (H^+) gain enough energy and get released as H_0 from the gate side, are then injected into IGZO under E-field, and finally get incorporated into IGZO film as an additional donor doping by releasing an electron [17]. This Hydrogen doping process makes IGZO film to be more conductive after NBS, provide more positive depletion charges, and thus can also result in a more negative P_{FE} reached after a longer negative stress pulse.

However, it can be noticed the kinetics and reversibility are quite different between the two mechanisms to supply positive charges:

- Hydrogen injection based on ion drift and diffusion: Due to the energy barrier of H_0 release and diffusion, this process only happens after a very long stress time. Besides, the Hydrogen doping effect makes IGZO being more conductive, resulting in a negative V_{th} shift, which is irreversible once Hydrogen ions are already incorporated in the IGZO film.
- Donor ionization based on electron emission and capture: between bandgap donor states and IGZO CB, so it's fast-switchable and reversible, as the electron re-capture into the ionized donor states is quite fast. (as shown in the schematics of Fig. 4 (c)).

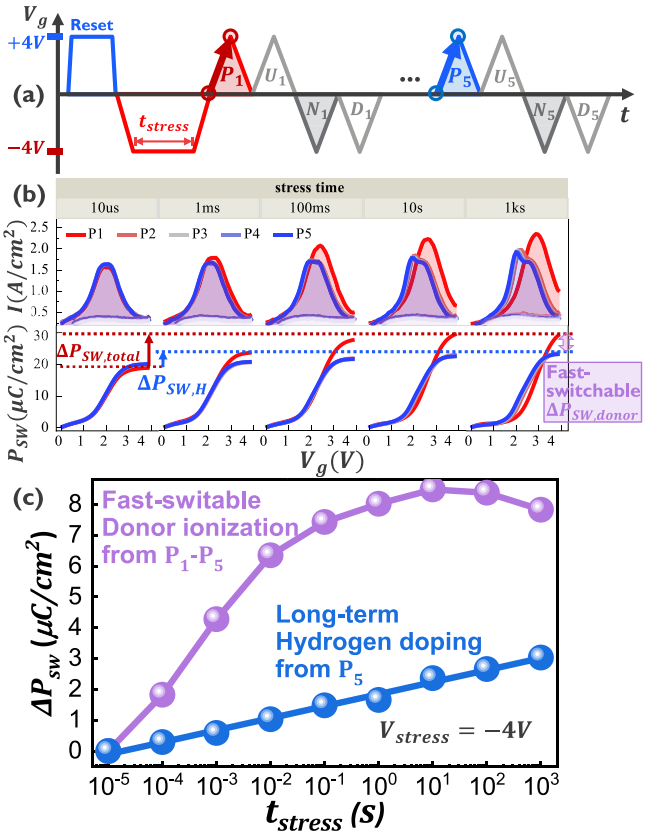

FIGURE 5. **(a): Schematics of the pulse waveforms applied on the back gate in the same stack as Fig. 3 (a). After a negative stress pulse, PUND reading waveforms are repeated for multiple times to detect the polarization reversal. (b): After the stress pulses, the P_1 pulse (curves in red) detects the charges that are generated by donor state ionization (reversible) and Hydrogen doping (not reversible) effects; While all the following pulse (P_2 to P_5), which are after re-neutralization of donor states, detect only the Hydrogen doping induced polarization increase. (c): After negative stress pulses, the blue curve shows the Hydrogen doping increase, exhibiting a slow kinetics and non-saturation. The violet curve shows positive charges generated due to donor state ionization, which is reversible by applying positive writing voltage and thus contributes to ferroelectric switching, exhibits a faster switching kinetics and gets saturated after long stress time.**

Based on the analysis above, we designed a measurement flow as shown in Fig. 5 (a), in which the triangular PUND reading waveforms are repeated for multiple times (from $P_1/U_1/N_1/D_1$ until $P_5/U_5/N_5/D_5$) after the NBS pulses with different negative stress time. The stress voltage in this measurement is fixed to be $-4V$.

After a longer NBS pulse, during the first Positive reading pulse (denoted as P1 pulse in Fig. 5 (a,b)), both ionized positively charged donors and the Hydrogen doping will contribute to the total increment of switching-only polarization reversal ($\Delta P_{SW,total}$, as plotted as the red curves in Fig. 5 (b)), which is calculated by:

$$\Delta P_{SW,total} = P_{sw,P_1}(t_{stress}) - P_{sw,P_1}(t_0) \tag{2}$$

where $P_{sw,P_1}(t_0)$ and $P_{sw,P_1}(t_{stress})$ are the switching-only polarization reversal (as calculated by eq. (1)) measured in the first reading pulse (P_1) at the initial state and after NBS pulses, respectively.

However, when the V_g is swept to a positive value during the reading pulses, the ionized donor states will re-combine with the electrons in IGZO CB, as shown in Fig. 4 (c). these neutralized donor states can not be emptied again during the reading pulses, in which the time under negative bias is too short for the electrons to emitted into CB. So that all the following PUND reading pulses (P_2 to P_5) give identical transient current and polarization curves, as shown in Fig. 5 (b). With the ionized donor states component being eliminated, the non-reversible (due to H drift only) increment of switching-only polarization reversal ($\Delta P_{SW,H}$, as plotted as the blue curves in Fig. 5 (b)), can be estimated by:

$$\Delta P_{SW,H} = P_{sw,P_5}(t_{stress}) - P_{sw,P_5}(t_0) \tag{3}$$

where $P_{sw,P_5}(t_0)$ and $P_{sw,P_5}(t_{stress})$ are the switching-only polarization reversal (as calculated by eq. (1)) measured in P_5 pulse at the initial state and after NBS pulses, respectively.

The polarization increment due to donor ionization can thus be evaluated by:

$$\Delta P_{SW,donor} = \Delta P_{SW,total} - \Delta P_{SW,H} \tag{4}$$

The $\Delta P_{SW,H}$ and $\Delta P_{SW,donor}$ components versus NBS pulse time are shown in Fig. 5 (c):

- Long-term Hydrogen-doping component (not helping FE switching): logarithmically dependent on the NBS t_{stress}, exhibiting a slow injection kinetics and no saturation up to 1000s stress.
- Fast-switchable and reversible donor-ionization component (thus helping FE switching): exhibits a much faster kinetics at the initial stage and the electron emission kinetics goes slower (which indicates saturation of ionized donors) when the NBS $t_{stress} > 10ms$. This component contribute much more positive charges ($\approx 8\mu C/cm^2$) than the Hydrogen-doping component.

IV. CONCLUSION

In this work, we provide a comprehensive analysis of the switching dynamics of IGZO-channel FeFETs and capacitors. We report that achieving a reliable erased state (as well as MW) requires long negative pulses during the erase operation, as confirmed by both V_{th} measurements on FeFETs with IGZO channel and polarization reversal measurements on FeCAPs with IGZO electrodes. The slow erase is attributed to the time-evolutionary donor state ionization, which emits electrons into IGZO Conduction Band during negative pulses, generating positively charged donors to support the P_{FE} being switched to a negative state. Furthermore, through repetitive reading experiments, the permanent increase of polarization after long negative bias pulses is attributed to IGZO doping by hydrogen, which is irreversible and does not contribute to ferroelectric switching. We propose that the electron emission mechanisms to supply positively charged donor states, which has a faster kinetics

and can be re-neutralized during programming operation, plays a vital role in enabling ferroelectric switching with IGZO channel. Future studies that take into consideration of field emission and tunneling of electrons from occupied donor states are needed to better understand the positive charge generation kinetics and then improve the erase efficiency.

REFERENCES

[1] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Appl. Phys. Lett.*, vol. 99, no. 10, Art. no. 102903, 2011. [Online]. Available: http://aip.scitation.org/doi/10.1063/1.3634052

[2] K. Florent et al., "Vertical ferroelectric HfO2 FET based on 3-D NAND architecture: Towards dense low-power memory," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2018, pp. 2.5.1–2.5.4. [Online]. Available: https://ieeexplore.ieee.org/document/8614710/

[3] M. Si and P. D. Ye, "The critical role of charge balance on the memory characteristics of ferroelectric field-effect transistors," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 5108–5113, Oct. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9528838/

[4] N. Gong and T.-P. Ma, "Why is FE–HfO_2 more suitable than PZT or SBT for scaled nonvolatile 1-T memory cell? A retention perspective," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1123–1126, Sep. 2026. [Online]. Available: http://ieeexplore.ieee.org/document/7517403/

[5] E. Yurchuk et al., "Charge-trapping phenomena in HfO_2-based FeFET-type nonvolatile memories," *IEEE Trans. Electron Devices*, vol. 63, no. 9, pp. 3501–3507, Sep. 2016. [Online]. Available: https://ieeexplore.ieee.org/document/7519093/

[6] F. Mo et al., "Experimental demonstration of ferroelectric HfO_2 FET with ultrathin-body IGZO for high-density and low-power memory application," in *Proc. Symp. VLSI Technol.*, 2019, pp. T42–T43. [Online]. Available: https://ieeexplore.ieee.org/document/8776553/

[7] M. Zeng et al., "First demonstration of annealing-free top gate la: HZO-IGZO FeFET with record memory window and endurance," in *Proc. Int. Electron Devices Meeting (IEDM)*, 2023, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/10413682/

[8] S. Dutta et al., "Lifelong learning with monolithic 3D ferroelectric ternary content-addressable memory," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2021, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/9720495/

[9] M.-K. Kim, I.-J. Kim, and J.-S. Lee, "CMOS-compatible ferroelectric NAND flash memory for high-density, low-power, and high-speed three-dimensional memory," *Sci. Adv.*, vol. 7, no. 3, 2021, Art. no. eabe1341. [Online]. Available: https://www.science.org/doi/10.1126/sciadv.abe1341

[10] Z. Lin, M. Si, and P. D. Ye, "Ultra-fast operation of BEOL-compatible atomic-layer-deposited In_2O_3 Fe-FETs: Achieving memory performance enhancement with memory window of 2.5 V and high endurance $>10^9$ cycles without V_T drift penalty," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, 2022, pp. 1–2. [Online]. Available: https://ieeexplore.ieee.org/document/9830156/

[11] M. Si, Z. Lin, J. Noh, J. Li, W. Chung, and P. D. Ye, "The impact of channel semiconductor on the memory characteristics of ferroelectric field-effect transistors," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 846–849, 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9152049/

[12] Z. Chen et al., "Improved MW of IGZO-channel FeFET by reading scheme optimization and interfacial engineering," in *Proc. IEEE Int. Memory Workshop (IMW)*, 2023, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/10145930/

[13] A. Chasin et al., "Understanding and modelling the PBTI reliability of thin-film IGZO transistors," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2021, pp. 31.1.1–31.1.4. [Online]. Available: https://ieeexplore.ieee.org/document/9720666/

[14] N. Gong, X. Sun, H. Jiang, K. S. Chang-Liao, Q. Xia, and T. P. Ma, "Nucleation limited switching (NLS) model for HfO_2-based metal-ferroelectric-metal (MFM) capacitors: Switching kinetics and retention characteristics," *Appl. Phys. Lett.*, vol. 112, no. 26, 2018, Art. no. 262903. [Online]. Available: https://pubs.aip.org/apl/article/112/26/262903/35554/Nucleation-limited-switching-NLS-model-for-HfO2

[15] Z. Chen et al., "A theoretical analysis of ferroelectric switching physics in metal/ferroelectric/IGZO stack toward Interlayer-free FeFETs," *IEEE Electron Device Lett.*, vol. 45, no. 8, pp. 1453–1456, Aug. 2024. [Online]. Available: https://ieeexplore.ieee.org/document/10551860/

[16] M. Bae, Y. Kim, S. Kim, D. M. Kim, and D. H. Kim, "Extraction of subgap donor states in a-IGZO TFTs by generation–recombination current spectroscopy," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1248–1250, Sep. 2011. [Online]. Available: http://ieeexplore.ieee.org/document/5976998/

[17] Y. Zhao et al., "Fundamental understanding of NBTI degradation mechanism in IGZO channel devices," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2024, pp. 1–7. [Online]. Available: https://ieeexplore.ieee.org/document/10529352/