Micro-Transfer Printing on Silicon Photonics: Tutorial, Recent Progress and Outlook

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***Abstract*—This paper highlights micro-transfer printing (MTP) as a promising scalable approach to heterogeneous integration for silicon photonics. MTP uniquely achieves high integration density, high throughput, and high material efficiency through a low-temperature, back-end integration process. Current demonstrations, including integrated III-V lasers and thin-film electro-optic modulators, confirm MTP's potential. Industrial adoption requires resolving challenges related to final integration yield and throughput, device reliability, and supply chain maturity.**

***Index Terms*—Heterogeneous integration, micro-transfer printing, silicon photonics.**

I. Introduction

INTERCONNECT technology plays a critical role in enabling system scalability. As AI computing architectures continue to evolve—whether through scale-up or scale-out approaches—limitations in data transmission bandwidth and efficiency have emerged as key bottlenecks to overall system performance. Silicon photonics enables high-bandwidth, low-latency optical interconnects, which are essential for overcoming the limitations of traditional electrical links in data-intensive computing environments. Over the past two decades, driven by technological advancements and the interest from industry, silicon photonics has transitioned from laboratory research to full-scale foundry manufacturing, becoming an established platform for photonic integrated circuits (PICs), particularly in telecom and datacom applications [1], [2], [3], [4]. This is largely due to its compatibility with O-band and C-band optical wavelengths and its unique advantage of CMOS foundry process compatibility [5], [6]. Today, the silicon photonics platform represents not merely an incremental technological upgrade but also a structural response to cross-generational demands in artificial intelligence (AI) and high-performance computing (HPC), through pluggables and co-packaged optics (CPO).

The most significant strength of silicon photonics lies in its compatibility with standard CMOS technology, which enables seamless integration with electronic components and leverages the mature, high-volume semiconductor manufacturing ecosystem. This compatibility allows for scalable production of PICs using existing foundry infrastructure, dramatically reducing per-unit cost and accelerating commercialization. However, this advantage also introduces a fundamental constraint: CMOS fabrication requires extremely capital-intensive infrastructure, optimized for producing highly sophisticated chips at minimal marginal cost. As a result, most CMOS foundries are highly conservative in their process flows and are generally unwilling to incorporate non-standard materials—such as Lithium Niobate ($LiNbO_3$) or III-V semiconductors—that are often classified as contaminants in CMOS environments, despite their superior properties. This reluctance limits the potential for heterogeneous integration, which could otherwise enhance the performance and functionality of silicon photonic devices. Consequently, while CMOS compatibility has enabled the rapid scaling of silicon photonics, it also imposes boundaries on material and device innovation.

Despite the advantages of CMOS compatibility, the Group IV material system used in silicon photonics cannot fulfill all functional requirements for advanced photonic applications. Silicon and silicon nitride [7] are well-suited for passive components

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TABLE I
MISSING BUILDING BLOCKS FOR FULLY INTEGRATED PHOTONIC SYSTEMS-ON-CHIP

Desired devices&functionality	Required material platform
Gain elements and lasers	GaN, GaAs, InP, GaSb, Ti:Sapph
Detection beyond 1600 nm	InP, GaSb
Electro-optic modulator	LN, LT, PZT, BTO, InP
Electro-absorption modulator outside C+L	InP, 2D material
Optical isolators and circulators	Ce:YIG, BIG
Single photon sources & detectors	InAs/GaAs QDs, cQDs, NbTiN
Electronics	Si, SOI, III-V

III-V semiconductors; Thin film materials (X-on-insulator, X-on-silicon); Bulk.

and certain modulation and detection tasks—often relying on Germanium (Ge) for photodetection. However, neither silicon nor silicon nitride can support efficient optical gain or lasing, which are typically achieved using III-V compound semiconductors [8], [9]. Furthermore, silicon modulators based on the plasma dispersion effect suffer from relatively high optical losses and bandwidth limitations. In contrast, low-loss, high bandwidth electro-optic modulation is achievable with materials such as lithium niobate [10], [11], [12] ($LiNbO_3$), lithium tantalate [13], [14], [15] ($LiTaO_3$), barium titanate [16] (BTO), and lead zirconate titanate [17], [18] (PZT), which are not natively compatible with CMOS processes. Additional functionalities such as electro-absorption modulation beyond the C+L band [19], non-reciprocal devices like optical isolators [20] based on magneto-optic materials (e.g., Yttrium Iron Garnet and Bismuth Iron Garnet), and quantum photonic components including single-photon sources [21] and detectors [22], also fall outside the capabilities of standard silicon-based platforms. These limitations highlight the need for heterogeneous integration methods to expand the functional scope of silicon photonics and enable next-generation photonic systems, for AI, quantum computing and beyond by introducing multiple material systems. An overview of the missing building blocks is given in Table I.

II. HETEROGENEOUS INTEGRATION APPROACHES FOR SILICON PHOTONICS

To fully utilize the advantages of non-CMOS-native materials in silicon photonics, several approaches are being pursued to enable wafer-scale heterogeneous integration: 1) flip-chip bonding of III-V and electronic integrated circuit dies; 2) die-to-wafer or wafer-to-wafer bonding of e.g. III-V, $LiNbO_3$ and $BaTiO_3$; 3) III-V epitaxial growth on silicon and 4) micro-transfer printing (MTP). This section will detail the four integration methods, including their process flow, integration level, material utilization efficiency, advantages and disadvantages, and current maturity, which are summarized in Table II. For clarity, in this paper we define front-end-of-line (FEOL) processes as those processes that define the waveguide layer including active and passive Si/SiN waveguides, back-end-of-line (BEOL) processes as all processes following the active or passive waveguide layers, and far-back-end-of-line (FBEOL) processes as non-standard or custom processes following all standard silicon photonics processes.

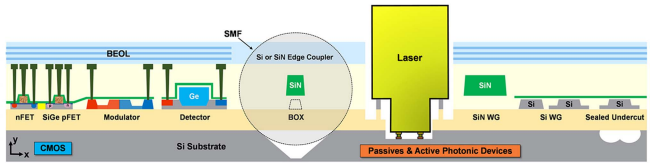


Fig. 1. III-V semiconductor laser integration on Silicon photonics platform based on flip-chip (GlobalFoundries Fotonix [23]).

A. Flip-Chip Bonding

Flip-chip bonding is a classical and mature integration method extensively employed in electronic IC assembly that has been successfully adapted for photonic integration (as presented in Fig. 1). The fundamental concept involves mounting integrated circuit (IC) dies, often referred to as chiplets, face-down onto a substrate to establish direct electrical and thermal connections. This technique is highly valued because it minimizes interconnection length and significantly reduces parasitic resistance and inductance compared to conventional wire-bonding. The process begins with the precise deposition of solder bumps or micro-bumps on the bond pads of the dies. During assembly, the dies are flipped so their bond pads align with corresponding pads on the substrate, followed by a reflow step to melt the solder and form robust electrical and mechanical joints.

Two primary alignment strategies are commonly utilized in flip-chip assembly. Self-alignment leverages the surface tension of molten solder bumps during reflow to achieve enhanced positional accuracy, often surpassing the initial placement precision of the assembly tool. Conversely, marker recognition relies on pre-patterned fiducial markers on both the die and the substrate, which are utilized by an optical vision system for precise placement.

For photonic devices, additional and significant challenges arise during flip-chip integration that restrict its application. The integration of components like lasers typically requires precise patterning of local recesses and waveguide facets on the substrate for low-loss butt-coupling. Integrating in-line waveguide devices—such as semiconductor optical amplifiers (SOAs) and modulators—is particularly problematic as two waveguide interfaces are involved, resulting in coupling efficiency reduction. These inefficiencies stem from several factors, including vertical misalignments introduced by the solder bumps, mechanical stops or III-V layer thickness variations, lateral and rotational misalignment, and unwanted free-space propagation losses across the gap between the III-V die and the substrate waveguide. The parasitics introduced by the bumps preclude the integration of ultra-high speed thin-film electro-optic chiplets (e.g., LiNbO3-on-insulator modulator chiplets). These inherent limitations underscore the need for alternative, more precise integration strategies, such as die-to-wafer bonding or micro-transfer printing, to realize complex, high-density photonic systems.

TABLE II
COMPARISON OF HETEROGENEOUS INTEGRATION APPROACHES FOR PHOTONIC SYSTEMS-ON-CHIP

Tech	Integration Density	Coupling Scheme	Alignment Accuracy	KGD Testing	Throughput Scalability	Material Efficiency	CMOS Platform Compatibility	Cost	Maturity
Flip-Chip	Low	Butt/Grating	Medium	Yes	Low	Medium	Back-end	High	Mature
Die-to-Wafer Bonding	High	Evanescent/Butt	High	No	High	Medium	Front-End or Back-end	High	Mature
Epitaxial Growth	High	Evanescent/Butt	High	No	High	Very high	Front-end	Low	R&D
MTP	High	Evanescent/Butt	High	Yes	High	High	Back-end	Low	Pilot Production

B. Die-to-Wafer Bonding

Die-to-wafer (D2W) bonding is a commercially deployed heterogeneous integration technique that enables the attachment of individual dies onto a full wafer, thereby facilitating the crucial co-integration of dissimilar material systems such as III-V semiconductors and silicon photonics. The process requires meticulous surface preparation, typically including polishing, cleaning and plasma activation to ensure the formation of high-quality bonding interfaces. Dies are placed onto the target wafer with moderate precision, followed by the actual bonding step. This bond is achieved through several established methods, including the use of adhesive layers (e.g.DVS-BCB), dielectric interface layers (e.g. AlO_x, SiO_x) or metallic interface layers (Cu-Cu or Au-Au). Post-bond processing typically involves substrate grinding and subsequent wet etching to expose the device layer stack for the final photonic device fabrication.

Die-to-wafer (D2W) bonding presents significant advantages for photonic integration, notably enabling efficient optical coupling between the bonded dies and the silicon waveguides, alongside compatibility with subsequent wafer-scale processing. This approach is highly attractive for integrating critical active and passive components—including lasers, SOAs, thin-film modulators ($LiNbO_3$, $LiTaO_3$, BTO, PZT), and photodetectors—onto silicon photonic platforms, especially for those devices requiring precise waveguide input/output coupling.

Despite its benefits, this technology requires substantial post-bond processing on the target wafer, which inherently increases the overall complexity of the silicon wafer fabrication, particularly when integrating multiple heterogeneous materials. Furthermore, the inability to test the heterogeneous integrated dies until they are fully processed poses a potential risk for yield reduction. Nevertheless, D2W bonding has achieved medium-to-high maturity and is now widely employed in commercial silicon photonics platforms (as presented in Fig. 2). Representative demonstrations include III-V laser arrays bonded on SOI wafers for datacom transceivers [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35] and $LiNbO_3$ / $LiTaO_3$ modulators integrated on silicon for high-speed optical communication [36], [37].

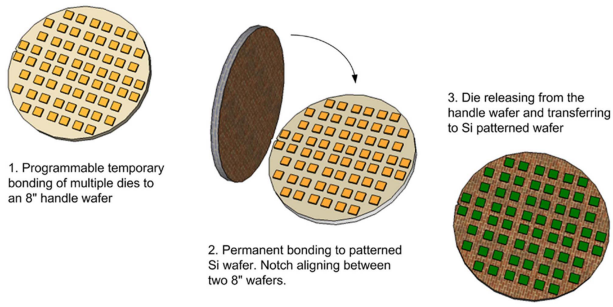


Fig. 2. Schematic of die to wafer bonding process flow.

C. Epitaxial Growth

Epitaxial growth represents a monolithic integration strategy wherein III-V materials are directly grown on silicon substrates using advanced techniques such as metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). This process is highly challenging and necessitates the deposition of specialized buffer layers and the implementation of sophisticated defect mitigation strategies, including selective area growth, dislocation filtering layers, the use of quantum dot active regions, etc. to effectively address the critical issues of lattice mismatch and thermal expansion differences between the III-V layers and the silicon substrate. Following successful epitaxial growth, active photonic devices such as lasers, amplifiers, and photodetectors are fabricated directly on the grown layers (or structures in the case of selective area growth), which critically eliminates bonding interfaces and thereby enables the highest level of integration density.

As a monolithic integration strategy, epitaxial growth offers several primary advantages for photonic integration. These benefits include achieving compact device footprints and the absence of mechanical bonding interfaces. Furthermore, this method holds the potential for low-cost, high-volume manufacturing once complex defect control challenges are fully overcome. Material utilization efficiency is inherently excellent in the case of selective area growth, as growth is precisely confined only to the areas where the III-V material is functionally required.

However, epitaxial integration faces significant challenges that currently limit its commercial adoption. These challenges include the pervasive issue of high defect densities caused by the fundamental lattice mismatch and thermal expansion differences between the III-V material and the silicon substrate. The required growth conditions are complex and highly sensitive. Critically, the technique suffers from incompatibility with established CMOS back-end processes due to the inherently high temperatures required for epitaxial deposition, requiring a re-engineering of the silicon photonics stack and process flow from the ground up. Consequently, the current maturity level of

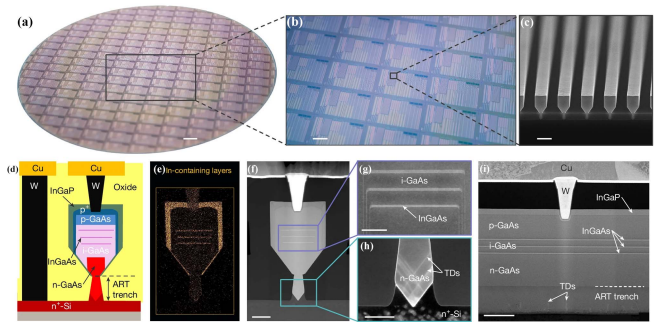


Fig. 3. (a) Photograph of a fabricated 300-mm Si wafer containing thousands of GaAs devices; (b) Close-up view of a fabricated 300-mm wafer showing several dies; (c) Cross-sectional scanning electron micrograph of a GaAs NR array after epitaxy and before encapsulation in oxide; (d) Sketch of the cross-section of a GaAs Nano-ridge (NR) device highlighting the various layers; (e) Energy-dispersive X-ray spectroscopy image of a NR cross-section highlighting the In-containing layers; (f) High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of a transverse cut of a GaAs NR device; (g) Dark-field scanning transmission electron microscopy (DF-STEM) close-up view of the InGaAs quantum wells embedded in the non-intentionally-doped GaAs; (h) DF-STEM close-up view of the n-GaAs–n-Si interface: (i) HAADF-STEM image of a longitudinal cut of a NR device. Figure reproduced from [38].

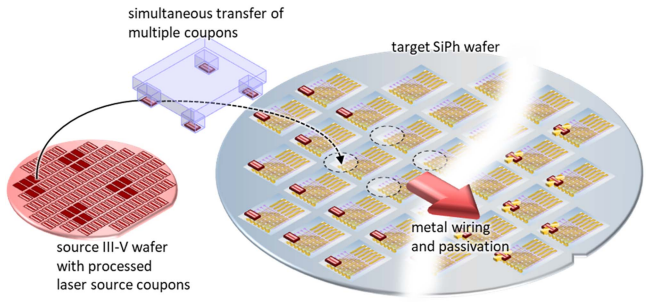


Fig. 4. Schematic of wafer-level micro-transfer printing.

epitaxial growth remains low to medium, with most successful implementations confined primarily to research and development environments. Notable demonstrations include quantum dot lasers grown on silicon for datacom applications and III-V nanoridge lasers integrated on SOI platforms [38], [39], [40], [41], [42], [43], [44], [45], showcasing the promise of monolithic integration for future photonic systems. Nanoridge laser structures are illustrated in Fig. 3.

D. Micro-Transfer Printing

Micro-transfer printing, a technology available under license from X-Celeprint Ltd., is an emerging, highly versatile heterogeneous integration technique that uniquely combines the benefits of die-level assembly and wafer-scale processing [46], [47], [48], [49], [50]. The MTP process begins with the fabrication of thin-film devices, or coupons, on a source wafer arranged in a dense array (typically with a 70 μm pitch), followed by the selective etching of a sacrificial release layer to free the devices from their native substrate. An elastomeric stamp, generally made of polydimethylsiloxane (PDMS), is then utilized to pick up multiple devices simultaneously and subsequently print them onto a target wafer with high placement accuracy, as illustrated in Fig. 4. Adhesive or direct bonding secures the devices permanently in place, which enables the seamless co-integration of diverse material systems, such as III-V semiconductors and $LiNbO_3$, onto large-area silicon photonic platforms.

MTP offers exceptional material utilization efficiency and versatility, allowing for the dense co-integration of multiple functional components while allowing for known-good die (KGD) integration. The key operational advantages of MTP include its inherent scalability for parallel printing, leading to high throughput (achieving rapid cycle times, such as 45 seconds per printing cycle), and its demonstrated sub-micron level alignment precision ($\mathbf{0.5}$ μm $\mathbf{3}\sigma$). The most significant advantage of MTP lies in its versatility and broad material compatibility for heterogeneously integrating two or more material systems. This versatility extends to both optical coupling schemes—supporting high-efficiency evanescent or butt coupling for photonic devices—and electrical interconnection via a redistribution layer (RDL). This architecture is highly flexible because the individual chiplets of any material system are not forced to compromise their unique fabrication processes or suffer from incompatibility with stringent CMOS requirements; they can continue to utilize the most advanced technologies of their respective material systems since the transfer printing integration occurs entirely at the far-back-end-of-line of the silicon photonics wafer processing.

However, despite its operational advantages, the MTP technology is still in its early stages of commercial application, facing unresolved challenges related to overall yield, long-term reliability, and supply chain maturity. Current research effectively demonstrates MTP's vast potential for next-generation photonic systems through several successful realisations. These include the printing of III-V semiconductor optical amplifiers/lasers [48], [51], [52], [53], [54], [55], [56], [57], [58], EAMs [59], [60] and photodiodes [61], [62], [63], [64], [65] onto silicon photonic wafers for active light manipulation and detection, as well as the integration of thin-film $LiNbO_3$ [66], [67], [68], [69], [70], [71], [72] and $LiTaO_3$ [73], [74] high-speed modulators. Such diverse and promising demonstrations clearly highlight MTP's capability to realize complex, high-performance heterogeneous photonic integrated circuits.

III. Micro-Transfer Printing Process and Demonstration

This section provides a detailed overview of the transfer printing process, including transfer-printing-compatible source wafer technology, wafer-level printing, and post-processing. It also introduces the latest transfer printing demonstrations from the Photonics Research Group (UGent - IMEC).

A. Source Wafer Fabrication

The preparation of the source wafer for micro-transfer printing involves several critical steps to fabricate suspended thin-film devices (coupons) that can be reliably picked and printed onto a target substrate. Here the fabrication of a thin-film slab on insulator ($LiNbO_3$) source coupon was used as an example,

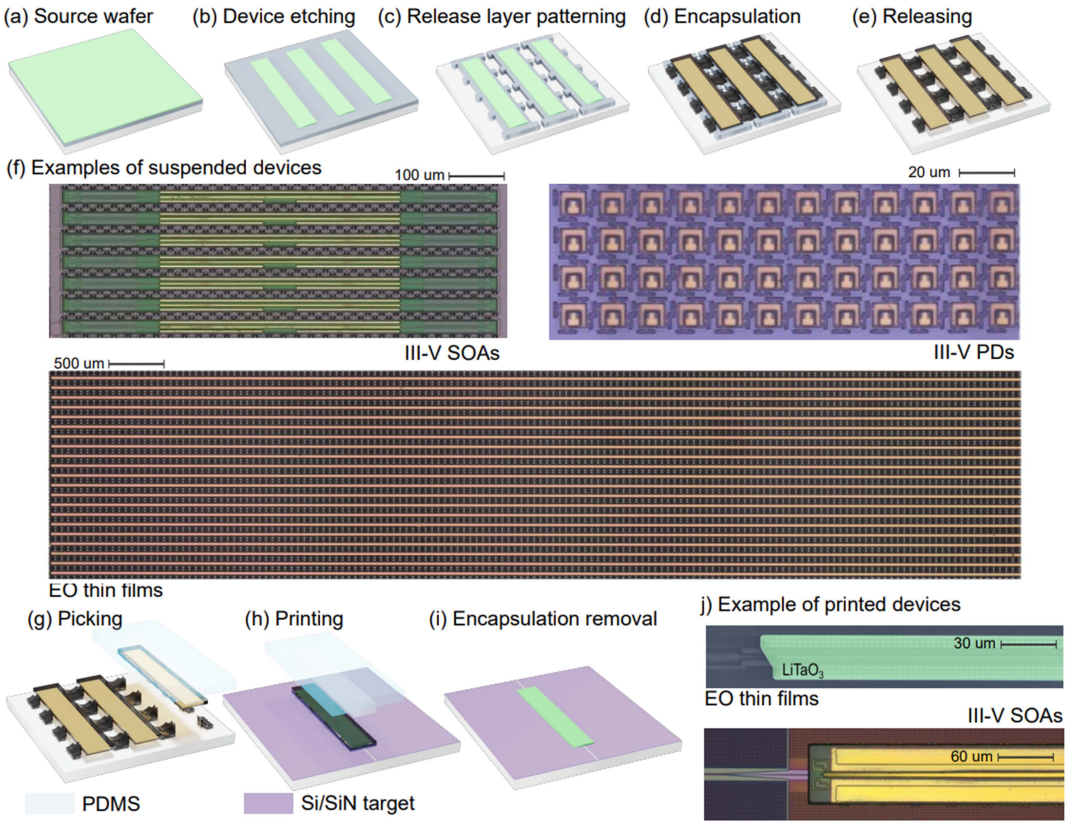


Fig. 5. Examples of coupon fabrication and printing process: (a) Source wafer of Thin flim devices; (b) Thin film devices coupon definition by dry etching; (c) Release layer pattern to define the sacrificial layer during undercut etching; (d) Tether definition and encapsulation as protection during undercut etching; (e) Undercut etching to suspend the device coupons; (f) Examples of released device coupon, including semiconductor optical amplifier (left), photodiode (right), Thin film modulator (bottom); (g) Coupon picking based on PDMS stamp; (h) Coupon printing onto target circuits; (i) Resist encapsulation removal; (j) Example of printed devices, including $LiTaO_3$ and SOAs.

but can be readily extended to III-V materials. The process flow is shown in Fig. 5 and summarized as follows:

1) *Starting Material:* Begin with thin-film-on-insulator (TFOI) wafers or dedicated III-V epi wafer consisting of functional layers on a sacrificial layer.
2) *Patterning of Functional Layer:* According to the specific functionalities of the to-be-printed coupons, the patterning of the functional layer consists of waveguide etch, metal/electrodes deposition, passivation and planarization.
3) *Release Layer Pattern:* Pattern the underlying release layer through UV lithography and perform a dry/wet etch to define the release regions.
4) *Resist Encapsulation:* Spin-coat photoresist and pattern it to form tethers that hold the coupons during release undercut etching. This encapsulation ensures mechanical stability and protects the devices during picking and printing.
5) *Undercut of Release Layer:* Remove the release layer beneath the coupons using wet etch or vapor etch, creating suspended coupons anchored by resist tethers.

The source wafer features tens of thousands of densely integrated, suspended LN coupons ready for PDMS stamp pick-up, maximizing material utilization through wafer-scale fabrication. To ensure an effective release from the native substrate, the coupons must be sufficiently narrow in one dimension. However, device length is of secondary importance; modulators up to 1 cm long can be transferred with high yield, which satisfies the dimensional requirements for thin-film LN applications. Device thickness is similarly non-limiting, with successful transfers demonstrated for coupons exceeding 10 μm in thickness. For ultra-thin devices, resist tethers serve a dual purpose: they act as an encapsulation layer that artificially thickens the coupon for improved stamp adhesion and provide crucial structural support to prevent the suspended thin-film structures from collapsing prior to transfer.

Any device or material that can be released from its substrate can be transfer-printed, including other electro-optic materials, III-V semiconductor materials, magneto-optic materials, 2D materials, thin film gain crystals, electronic chiplets, etc. The release layers and the release etching processes need to be considered carefully for the different material systems. Table III summarizes the current material systems that have been successfully heterogeneously integrated on silicon photonics by micro-transfer printing.

B. Wafer-Level Printing

As illustrated in Fig. 6, the micro-transfer printing process is governed by the rate-dependent adhesion strength between the

TABLE III
MATERIAL SYSTEMS AND RELEASE ETCH APPROACHES

Device layer	Release layer	Substrate	Wet etch	Vapour etch
GaN	Doped GaN	GaN	Oxalic	-
GaAs	AlGaAs/InGaP	GaAs	HCl:H_2O	-
InP	InGaAs/AlInAs	InP	$FeCl_3$:H_2O	-
GaSb	InAsSb	GaSb	Citric: H_2O_2	-
Thin Film*	SiO_2	Si	HF	HF
Thin Film*	Si	Si	TMAH	XeF_2

* LN, LT, PZT, BTO, 2D materials, Ce:YIG, cQDs, NbTiN, Ti:sapphire, SOI electronics,...

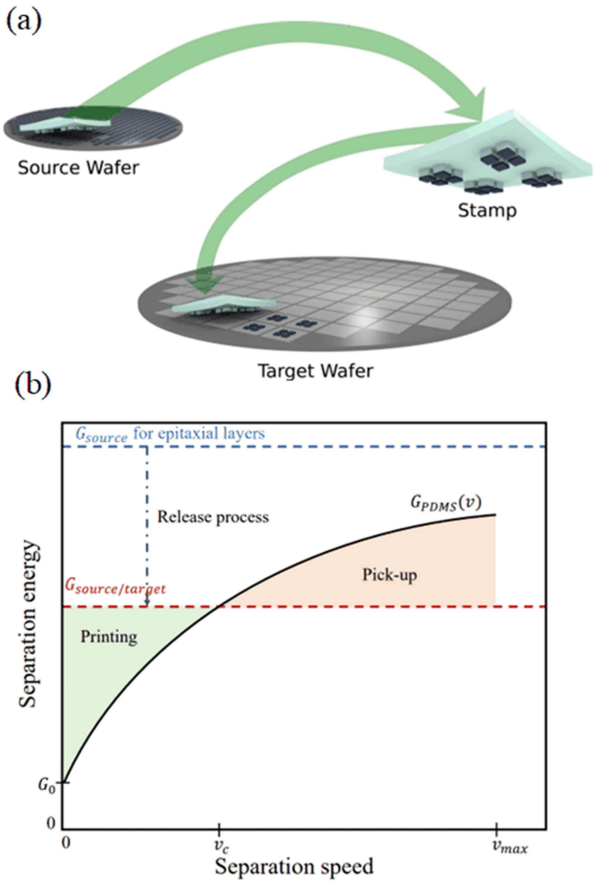


Fig. 6. PDMS-based stamp for micro transfer printing: (a) schematic of the picking and printing process; (b) schematic illustrating rate-dependent pick-up and print behavior.

transferred coupon and the elastomeric stamp. A high-velocity peel generates sufficient adhesion to detach the object from its native substrate, while a slow stamp retraction reduces this adhesion, allowing the coupon to release onto the target substrate. This kinetically controlled mechanism operates entirely at room temperature without requiring specific applied force. To secure the printed coupon, an adhesive bonding agent, such as DVS-BCB, is utilized; this agent inherently relaxes the target substrate's surface roughness and topography requirements depending on the applied thickness. Consequently, the maximum allowable post-printing temperature excursion is strictly dictated by the thermal degradation limits of the selected bonding agent, which is typically 350 °C for DVS-BCB.

The alignment accuracy between the coupon and the target wafer is critical for the optical and electrical performance of transfer-printed devices, particularly for components that rely on efficient light coupling. This sensitivity is heightened for coupons with a waveguide interfaces, such as waveguide-integrated active components including III-V lasers, SOAs and EAMs, where light must be efficiently transferred from the passive silicon or silicon nitride waveguide into the active material, and ridge-patterned thin-film electro-optic devices, such as $LiNbO_3$ modulators, where misalignment directly translates to high optical insertion loss at the coupling interface. In comparison, the slab thin-film coupon, presented in Fig. 5 normally has a relatively large tolerance to lateral misalignment.

Achieving the required sub-micron alignment relies fundamentally on the design and quality of the printing alignment markers. The markers on both the source and target wafer must be meticulously designed to fit the specific pattern/image recognition and illumination system of the micro-transfer printer. Optimal marker design involves (a) high contrast and clarity: ensuring clear definition and high contrast between the marker feature and the surrounding material to minimize uncertainty during image processing and (b) geometric robustness: using robust geometries (e.g., hierarchical or nested patterns) that minimize distortion and allow the system to average out local fabrication non-uniformities. Meanwhile, the process compatibility also need to be taken into account. The marker materials, structure, etching depths must not compromise the integrity of the underlying waveguides or the transfer printing process itself (e.g., must not interfere with the optical confinement and release layer). The use of these markers allows the system to calculate and correct the relative position and orientation ($\mathbf{x}, \mathbf{y}$, and θ) between the coupon and the target substrate before final contact.

Despite the complexity of handling flexible coupon materials and the inherent limitations of standard photolithography markers, significant progress has been demonstrated. Even with imperfect markers from early-stage development, the 3σ alignment accuracy achieved has been very close to the benchmark set by the printing tool vendor, which typically falls around $\pm\mathbf{0.5}$ μm. The 3σ value indicates that 99.7% of all printed coupons fall within this specified tolerance range. Further optimization of marker design, moving toward dedicated metrology-grade markers tailored for MTP systems, is expected to tighten this 3σ distribution significantly. This improvement is essential to fully exploit the transfer printer's capabilities and to simplify the design of the on-chip alignment-tolerant tapers, thereby reducing their physical length and optical loss. Fig. 7 presents the results of preliminary III-V printing alignment experiments, confirming that excellent alignment statistics can be approached even before full marker optimization.

C. Post-Processing

Post-MTP processing transforms individual transfer-printed coupons into fully functional heterogeneous integrated chiplets by establishing electrical interconnection and defining final device structures. This process fundamentally involves patterning the RDL, typically composed of thick, low-resistance metals like gold (Au) or aluminum (Al), to connect the chiplet to the

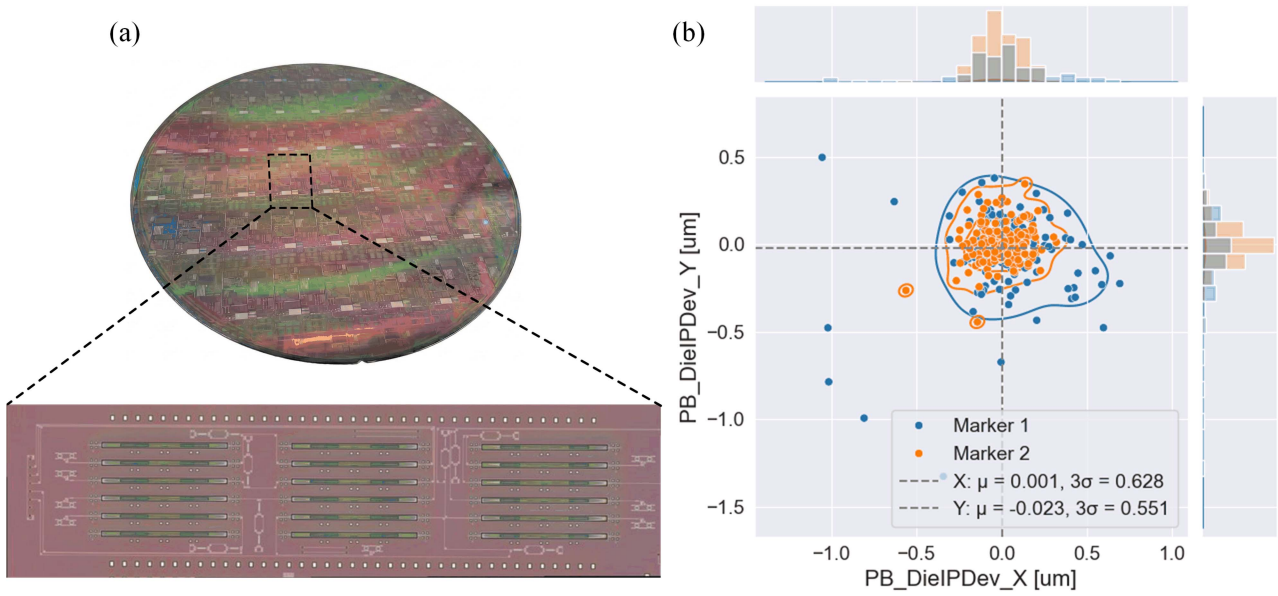


Fig. 7. Printing results: (a) Microscope photos of III-V SOAs on IMEC ISIPP200 SiPh wafer; (b) Alignment accuracy of III-V printing.

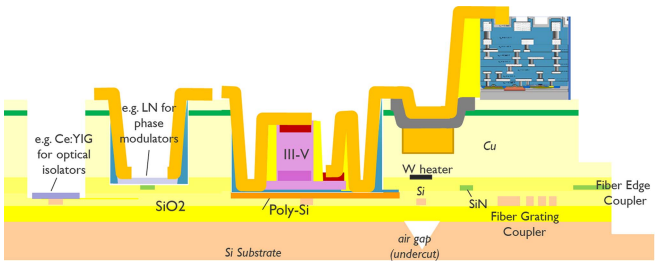


Fig. 8. Schematic: Dense co-integration of different types of chiplets on IMEC silicon photonics platform by micro-transfer printing.

back-end stack of the SiPh wafer. The metal chosen must ensure low RC delay, good adhesion to all surfaces, and complete process compatibility.

The specific post-processing requirements are determined by the printed material. For active III-V components (such as SOAs, EAMs, and PDs), the RDL serves to land directly onto the coupon's pre-patterned native bond pads, connecting them to the electrical traces on the target wafer. Conversely, for thin-film devices like TFLN and TFLT modulators, the RDL often assumes a dual role: it is used to define the final, crucial high-speed electrodes (such as coplanar waveguides, CPW) directly onto the coupon's surface while simultaneously ensuring electrical connection to the peripheral circuitry on the target platform. In essence, post-MTP metallization is the step that ensures low parasitics and high-speed integration with the silicon photonics circuit, enabling the final heterogeneous circuit (as Fig. 8 presented) to operate at ultimate speed and efficiency.

D. Recent Demonstrations

1) InP Laser on the Imec iSIPP50 G Silicon Photonic Platform for Reconfigurable Microwave Photonics Engines: This

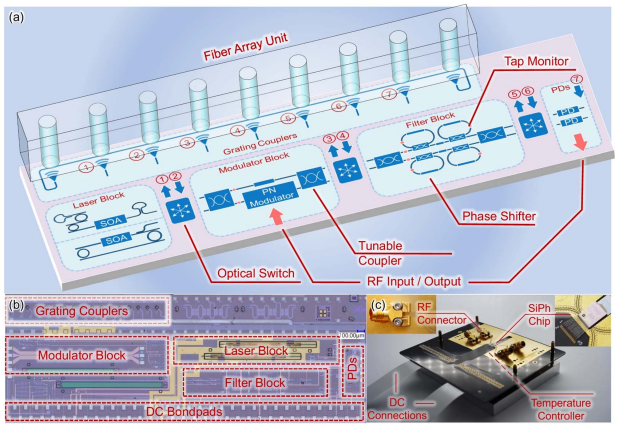


Fig. 9. (a) Schematic block diagram of the silicon photonic engine. (b) Microscope image of the fabricated chip; (c) A packaged demonstrator with wirebonded controls and microwave connectors (before fiber attachment). Reproduced from [75].

work demonstrates a fully integrated silicon photonic engine capable of processing both optical and microwave signals and performing bidirectional conversion between these domains. Fabricated on the IMEC ISIPP50 G platform, the chip integrates key components such as high-speed modulators, photodetectors, programmable optical filters, and tunable lasers achieved through micro-transfer printing of InP optical amplifiers. The engine operates as a black-box microwave photonics processor, allowing RF signal processing without external optical devices, while maintaining full programmability for hybrid optical-RF configurations.

The chip comprises four functional blocks as Fig. 9 presented:

- Tunable Laser Block (two lasers, 90 nm tuning range),
- Reconfigurable Modulator Block (intensity and phase modulation),

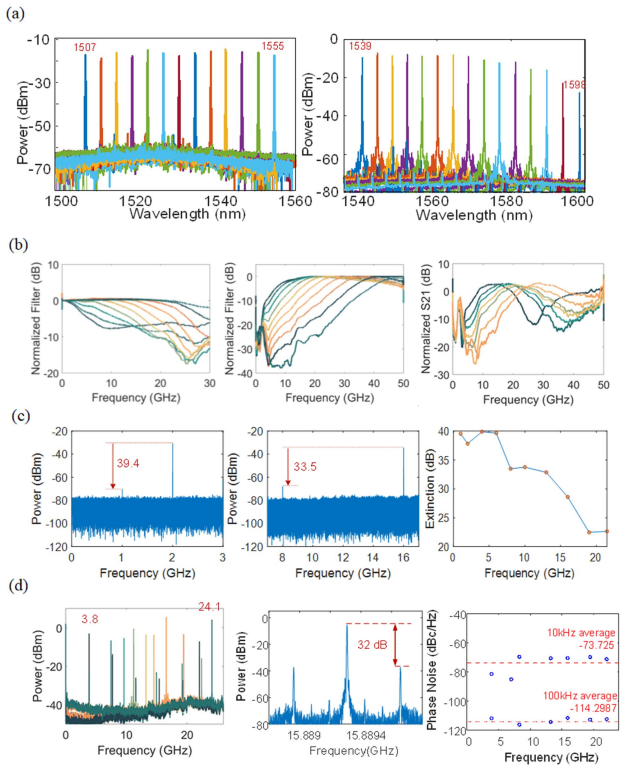


Fig. 10. (a) On-chip MTP InP tunable laser; (b) Microwave filtering: tunable low pass filter; Tunable high pass filter; Tunable bandpass filters. (c) Microwave frequency doubling: Frequency doubling results with off-chip PD; Frequency doubling results with on-chip PD; (d) Opto-electronic oscillator response: RF signal generation with 500 m fiber and off-chip PD. Reproduced from [75].

- Programmable Optical Filter Block (ring-loaded MZI for auto-regression/moving average (ARMA) filtering),
- High-Speed Photodetector Block (up to 25 GHz bandwidth after package).

Programmability is achieved via 52 thermo-optic phase shifters and optical switches, enabling dynamic configuration for diverse functionalities: optical and RF filtering, frequency conversion, RF equalization, and opto-electronic oscillation. Due to the reconfigurability, several demonstrations include:

- Optical-to-Electrical (O/E) and Electrical-to-Optical (E/O) conversion with bandwidth up to 26 GHz;
- Microwave photonic filtering using dual-sideband modulation;
- RF frequency doubling with 40 dB extinction ratio;
- Tunable opto-electronic oscillator (OEO) generating RF signals from 4-24 GHz with phase noise of -114 dBc/Hz at 100 kHz offset.

The chip footprint is 5 mm $\times$ 1.3 mm, consuming 1.1 W under full operation. Despite RF crosstalk and packaging limitations, the engine achieves competitive performance compared to state-of-the-art integrated microwave photonic systems (presented in Fig. 10), marking a significant advance toward compact, low-power, and programmable photonic processors for next-generation wireless and sensing applications.

Seamless integration of III-V lasers and complex silicon photonic integrated circuits is achieved through micro-transfer printing. The process enables heterogeneous integration of III-V devices without disrupting the silicon photonics process flow. Localized back-end openings allow efficient evanescent-coupling between transfer-printed SOAs and silicon waveguides, while the low-temperature bonding is compatible with the thermal budget of the silicon platform. The successful integration of tunable InP lasers in this work exemplifies how MTP can unlock full functionality for programmable photonic engines, paving the way for compact, low-power, and reconfigurable microwave photonic systems.

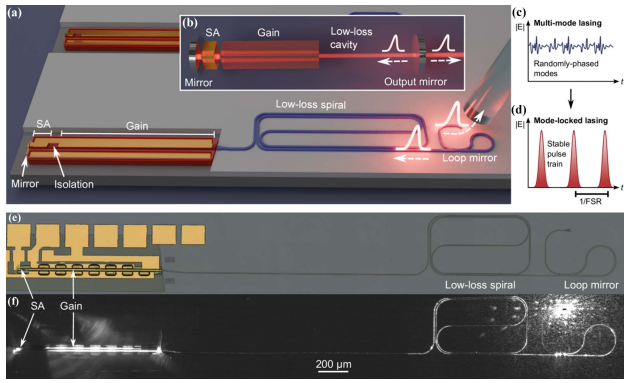


Fig. 11. Schematic and the properties of the integrated mode-locked laser (a) Illustration of a fully integrated extended-cavity mode-locked laser on silicon nitride. (b) (inset) Equivalent free-space mode-locked laser system. (c) Schematic time-dependent output field of Fabry-Perot laser without mode-locking. (d) Schematic time-dependent output field of a mode-locked laser with a saturable absorber. (e) Bright-field microscope image of a mode-locked laser. (f) Dark-field microscope image of the same laser under 50 mA gain current with forward-biased SA, showing side-wall scattering and emission from the grating coupler. Reproduced from [76].

2) GaAs on SiN Continuous Wave Laser and Mode-Locked Laser: We demonstrated the heterogeneous integration of III-V semiconductor lasers on a SiN photonic platform using MTP (Fig. 11), enabling compact and high-performance laser systems at near-infrared wavelengths (800 nm). The integration addresses critical challenges in coupling III-V gain materials to low-loss SiN waveguides, which are essential for applications such as quantum computing, optical atomic clocks, and nonlinear photonics. MTP enables a direct butt-coupling scheme with superior thermal characteristics and broadband coupling capability.

The process flow begins with the fabrication of GaAs-based laser coupons featuring quantum well gain sections and saturable absorbers on a source wafer. These coupons are under-etched and suspended for pick-up using an elastomeric stamp. After pick-up, the coupons are printed into the deep-etched recesses on the SiN wafer, aligned to the waveguide with sub-micron precision. A thin DVS-BCB layer ensures adhesion, followed by planarization and metallization for electrical contacts. This approach achieves a 96% mode overlap between the III-V and SiN waveguides, enabling efficient coupling without intermediate tapers. The integration is fully compatible with wafer-scale manufacturing, allowing selective placement of pre-characterized devices and efficient use of III-V material.

Using this integration method, extended-cavity continuous-wave (CW) and mode-locked lasers on the IMEC 300 nm

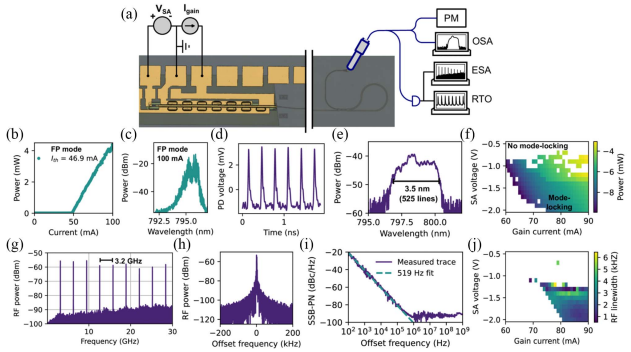


Fig. 12. Performance of the extended-cavity continuous-wave and mode-locked lasers. (a) Measurement setup with PM: power meter; OSA: optical spectrum analyzer; ESA: electrical spectrum analyzer; RTO: real-time oscilloscope. (b) CW LI curve of a 9.2 GHz FSR extended-cavity Fabry-Perot laser. (c) Optical FP spectrum at 100 mA gain current measured with a resolution bandwidth of 30 pm. (d) Pulse train of a 3.2 GHz MLL at 85 mA gain current and −1.3 V SA bias as measured on a 25 GHz photodiode. (e) Widest achieved mode-locked optical spectrum at 90 mA gain current and −1.3 V SA bias measured with a resolution bandwidth of 30 pm. (f) Mode-locking map showing average waveguide-coupled output power for different gain currents and saturable absorber bias voltages, where white data points correspond to laser operation modes without mode-locking, as determined from the RF spectrum. (g) RF comb at optimal mode-locking point of 85 mA gain current and −1.3 V SA bias. for a resolution bandwidth (RBW) of 100 kHz. (h) Fundamental RF line, measured with RBW of 100 Hz. (i) Single sideband phase noise (SSB-PN) measurement of fundamental RF line along with a 519 Hz Lorentzian fit. (j) Mode-locking map of fundamental Lorentzian RF linewidth as fitted from SSB-PN measurement, where white data points correspond to laser operation modes without mode-locking which was stable enough for a SSB-PN measurement. Reproduced from [76].

SiN platform were realized. As Fig. 12 presented, the CW Fabry–Perot lasers exhibit waveguide-coupled output powers exceeding 4 mW and thresholds around 48 mA, with potential for >50 mW waveguide-coupled power after optimization. Mode-locked lasers leverage saturable absorbers and low-loss SiN spirals to achieve long photon lifetimes and low repetition rates, resulting in pulse trains with free spectral ranges of 3.2 GHz, 7.5 GHz, and 9.2 GHz. The 3.2 GHz device demonstrated a 10-dB optical bandwidth of 3.5nm (≈1.7 THz) and a fundamental RF linewidth of 519 Hz, corresponding to a timing jitter of 51 fs, indicating excellent passive stability. Pulse energies up to 0.27 pJ were achieved, with projections of several pJ after coupling optimization.

Micro-transfer printing is highly compatible with advanced SiN photonic platforms and CMOS back-end processes. It avoids high-temperature bonding steps, preserving the thermal budget and integrity of the underlying photonic circuits. Compared to the silicon platform, silicon nitride lacks of any native active components, while the transfer printing technique supports heterogeneous integration of multiple material systems, enabling co-integration of lasers, amplifiers, modulators, photodetectors and nonlinear elements on the same wafer. By combining MTP with the ultra-low-loss advantage from SiN waveguides, this approach unlocks scalable, high-density photonic integration for next-generation AR/VR, quantum technologies, and microwave photonics.

3) InP on SiN Narrow-Linewidth Widely Tunable Laser: Heterogeneous integration of III-V gain materials on low-loss

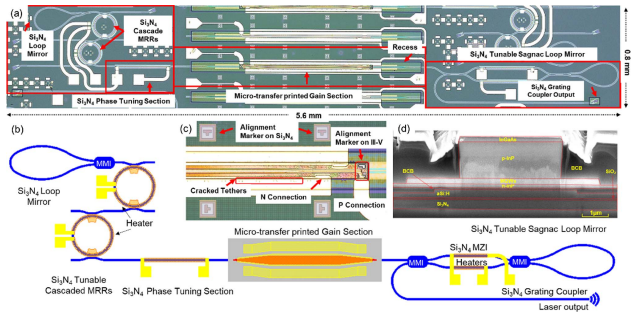


Fig. 13. (a) Microscope picture of the proposed tunable laser. (b) Corresponding schematic diagram of the cavity structure (MRR, micro-ring resonator; MMI, multimode interferometer). (c) A zoom-in view of the micro-transfer-printed III-V gain section on aSi:H/Si_3N_4 waveguides. (d) SEM image of a cross-section of the micro-transfer printed III-V gain element on the aSi:H/Si_3N_4 waveguide. Reproduced from [77].

Si_3N_4 platforms is a key enabler for next-generation PICs, particularly for applications requiring narrow-linewidth and widely tunable lasers. Si_3N_4 offers ultra-low propagation loss and high optical power handling, making it ideal for high-Q cavities and linewidth reduction. However, the large refractive index mismatch between III-V and Si_3N_4 waveguides poses significant integration challenges for evanescently coupled devices. This work demonstrates a widely tunable narrow-linewidth laser on IMEC's dedicated 200 mm Si_3N_4 platform (Fig. 13), which is compatible with micro-transfer printing, providing a scalable and CMOS-compatible solution for heterogeneous integration. The proposed laser employs a cascaded micro-ring resonator (MRR) mirror in Si_3N_4 to achieve wavelength tuning across multiple Vernier periods. The cavity consists of:

- A micro-transfer-printed InP gain section on an amorphous silicon (aSi:H) rib waveguide on Si_3N_4.
- Two Vernier MRRs combined with a Sagnac loop mirror for mode selection and extended tuning.
- A Mach–Zehnder interferometer (MZI) with tunable reflectivity for output coupling control.
- Integrated micro-heaters for thermo-optic tuning of MRRs and phase sections.

The Vernier MRR configuration leverages Si_3N_4 dispersion to extend tuning beyond the fundamental Vernier free spectral range (FSR), enabling continuous tuning across three Vernier periods.

Micro-transfer printing enables the integration of pre-fabricated III-V coupons onto the Si_3N_4 platform without high-temperature bonding steps, preserving the integrity of both material systems. The source wafer process includes:

- Patterning of ridge waveguides and multi-quantum well (MQW) mesas.
- Deposition of n- and p-side contacts and tether formation.
- Planarization with DVS-BCB and selective under-etching of release layers to suspend coupons.

The target wafer process involves:

- Fabrication of Si_3N_4 waveguides and aSi:H coupling layers.
- Planarization, micro-heater definition, and recess etching for evanescent coupling.

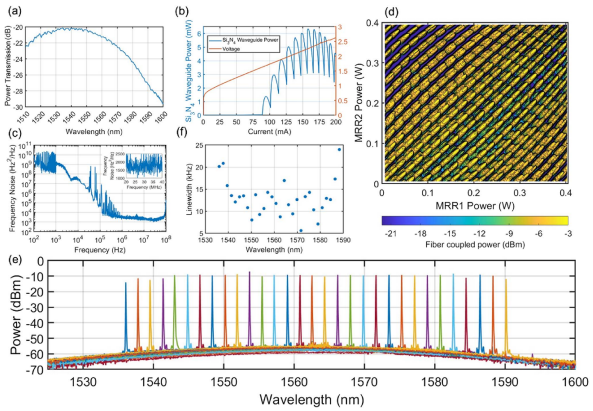


Fig. 14. (a) Transmission spectrum of the reference waveguide with grating couplers at both sides. (b) LIV curve of III-V on the Si_3N_4 tunable laser. (c) Laser frequency noise spectrum at 1571.56 nm (inset: zoom-in view of the spectrum from 20 MHz to 40 MHz). (d) Two-dimensional output power tuning map of the laser. (e) Optical spectra under different operation wavelengths. (f) Lorentzian linewidth as a function of wavelength.

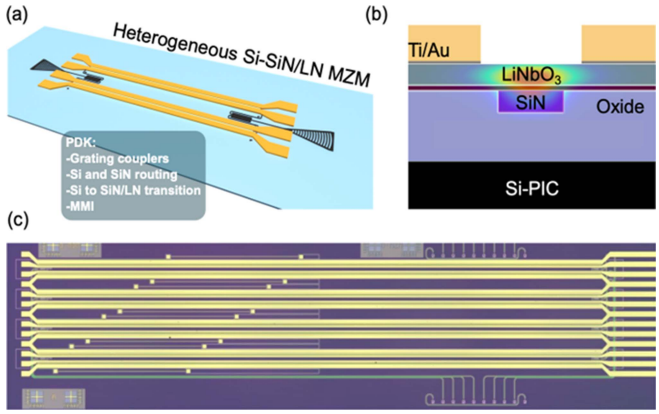


Fig. 15. Concept of a heterogeneous Si-SiN/LN modulator. (a) Schematic view of the heterogeneous Si-SiN/LN modulator. (b) Cross-section of the Mach–Zehnder modulator arm showing the hybrid SiN/LN optical mode. (c) Optical picture of a fabricated chip consisting of four modulators. Reproduced from [69].

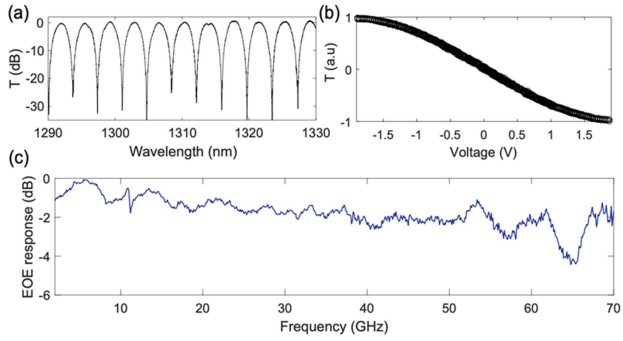


Fig. 16. Characterization of a typical heterogeneous Si-SiN/LN MZM. (a) Extinction ratio. (b) Half-wave voltage. (c) EOE bandwidth. Reproduced from [69].

- Spray-coating of a thin DVS-BCB adhesive layer, printing and post-printing metallization.

This approach ensures wafer-scale integration compatibility, selective integration of known-good dies, and efficient use of III-V material, making it suitable for high-volume manufacturing. As Fig. 14 presented, the integrated laser demonstrates a wavelength tuning range of 54 nm across C and L bands, an intrinsic linewidth $<$ 25 kHz over the entire tuning range, Side-mode suppression ratio (SMSR) $>$40 dB, an output power of 6.3 mW in the Si_3N_4 waveguide at 158.5 mA bias and a threshold current of about 90 mA

The detuned-loading effect is observed, where the lowest linewidth occurs slightly off the resonance peak. Micro-heater optimization enables efficient thermal tuning with minimal coupling ratio variation, ensuring stable operation. This demonstration highlights the compatibility of MTP with advanced Si_3N_4 platforms, enabling the heterogeneous integration of active III-V devices on passive silicon nitride waveguide circuits. By minimizing post-printing processes and leveraging foundry-level fabrication for both material systems, this approach paves the way for scalable, low-cost, and high-performance photonic systems-on-chip for coherent communications, LiDAR, and microwave photonics.

4) Wafer-Level Transfer Printed $LiNbO_3$ on SiN Modulator: Lithium Niobate is a key material for high-speed electro-optic modulation and nonlinear optical processes due to its large Pockels coefficient and intrinsic $\chi^{(2)}$ nonlinearity. However, CMOS-compatible platforms such as silicon nitride lack these active functionalities as LiNbO3 is not a CMOS-compatible material. To overcome this limitation, MTP has emerged as a versatile technique for integrating TFLN onto SiN photonic circuits (Fig. 15), enabling high-performance modulators and nonlinear devices while maintaining compatibility with mature foundry processes.

The MTP process begins with the fabrication of LN coupons on an LNOI source wafer, which has been discussed in the previous section. The steps include:

- Patterning of LN layer using UV lithography and reactive-ion etching (RIE) with an amorphous silicon hard mask;
- Release layer patterning to define regions for undercutting;
- Resist encapsulation to form tethers that suspend LN coupons during transfer;
- HF-based wet etching of the oxide layer to create suspended LN coupons;

The coupons, ranging from 1 mm to 1 cm in length, are picked up using a PDMS stamp and printed into etched recesses on the SiN target wafer. A thin DVS-BCB layer ensures adhesion. Printing is followed by metallization for electrode formation. This approach supports wafer-scale compatibility and efficient material utilization.

As a proof of concept, a 1 cm-long push-pull Mach–Zehnder modulator (MZM) was integrated on a SiN platform using MTP. As Fig. 16 presented, the modulator achieved a half-wave voltage ($V\pi$) of 3.2 V$\cdot$ cm, among the lowest reported for MTP-based LN devices, a bandwidth $>$ 70 GHz, verified through high-speed measurements, a propagation loss of 0.5 dB/cm for LN sections and a coupling loss of $\approx$0.25 dB per transition between SiN and LN.

The LN/SiN modulator demonstrated excellent electro-optic performance, confirming that MTP does not degrade LN's high-speed properties. Additionally, the technique enables complex

electrode configurations such as ground-signal-signal-ground (GSSG), improving linearity and reducing electromagnetic interference.

Micro-transfer printing offers several advantages over traditional bonding techniques in this case. By leveraging MTP, LN-based modulators and nonlinear devices can be seamlessly integrated with SiN photonic circuits, paving the way for compact, energy-efficient systems for high-speed data communication, quantum photonics, and microwave signal processing.

5) Transfer Printed EIC Chiplets for Electronics and Photonics Co-Integration: In [78] we demonstrate a heterogeneous electronic/photonic optical receiver that integrates a SiGe BiCMOS transimpedance amplifier (TIA) with a Ge PD on imec's 300 mm advanced silicon photonics platform (IMEC ISIPP300). This approach addresses the limitations of wire bonding and flip-chip integration by enabling massively parallel, wafer-scale heterogeneous integration with minimal parasitics.

The integration begins with the fabrication of 20 μm-thick SiGe BiCMOS TIA chiplets (200 μm $\times$ 300 μm footprint) on an SOI wafer. The chiplets are released using TMAH etching of the silicon substrate, then picked up by a PDMS stamp and printed onto a PIC that includes the Ge PD. A thin layer of DVS-BCB is spin-coated on the PIC prior to printing for adhesion, followed by a second spin-coated layer (after printing) to form ramps around the chiplet and overcome the 20 μm step height. Post-printing metallization is performed using Ti/Au deposition to create electrical interconnections between the TIA and the PD. This photolithographic approach enables bondpads as small as 20 μm $\times$ 20 μm, significantly reducing interconnect parasitics compared to wire bonding.

The heterogeneous receiver is optimized for O-band operation (1310 nm) and consists of a Ge photodiode on the imec 300 mm silicon photonics platform interfaced through a grating coupler for fiber interfacing and with electroless plated NiAu pads (Fig. 17). As Fig. 17 The 3D-integrated receiver achieves 224 Gb/s PAM4 (KP4FEC 2.4 $\times$ 10^{-4} at -5.2 dBm optical modulation amplitude) and consumes 0.51 pJ/bit @ 224 Gb/s (Fig. 18).

This approach is compatible with CMOS back-end processes and supports co-integration of diverse material systems, paving the way for compact, energy-efficient optical transceivers for data centers and AI-driven networks.

IV. Outlook and Challenges

To transition MTP from laboratory prototypes to an industrial reality, we established a 200 mm pilot line that develops five aspects to translate R&D demonstrators to volume manufacturing (Fig. 19).

1) *Design:* Co-design of source coupons and SiPh target circuits. This includes defining misalignment-tolerant optical interfaces (evanescent/butt coupling), standardized electrical pad stacks for post-print metallization, and machine-vision alignment markers. Process-control monitors (PCM) are embedded to track placement error, coupling loss, and interconnect parasitics.

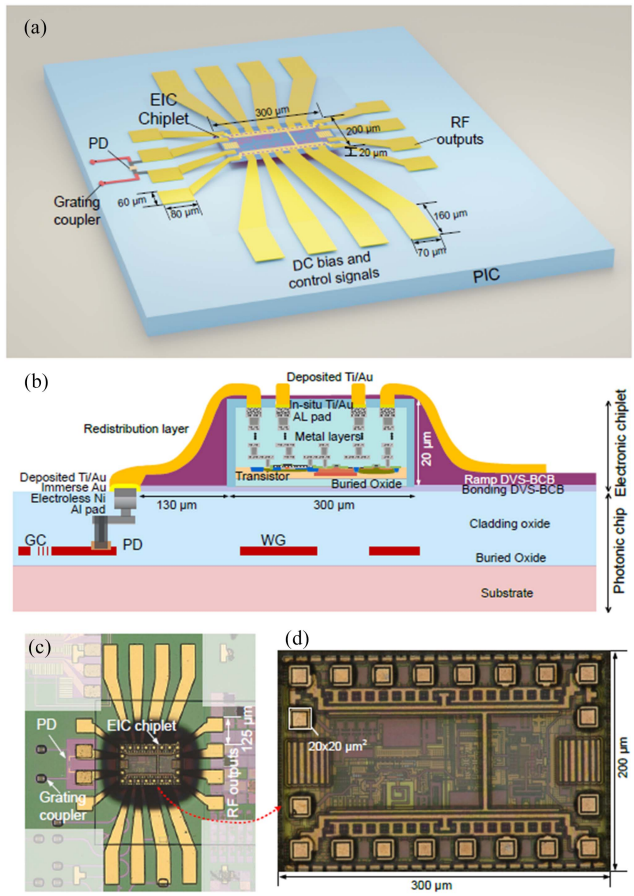


Fig. 17. (a) 3D diagram of the optical receiver consisting of an EIC chiplet micro-transfer printed on a Si PIC and metal traces (b) Cross-section diagram of the optical receiver (c) Micrograph of the optical receiver (d) Micrograph of the EIC chiplet. Reproduced from [78].

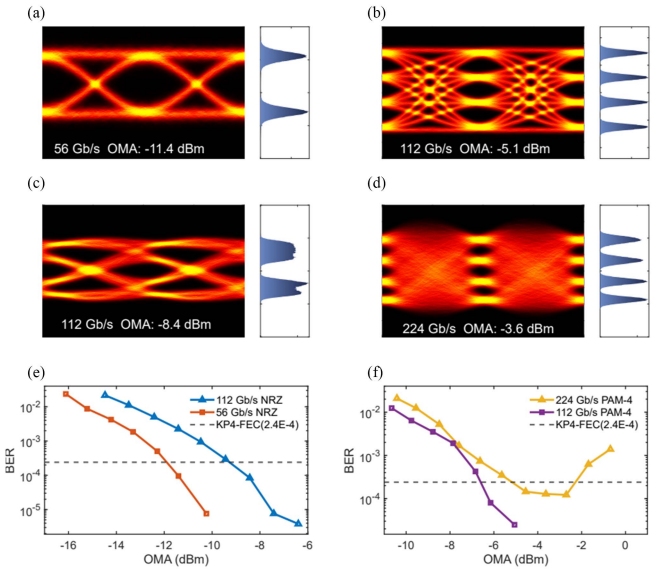


Fig. 18. Data transmission experiment results. (a) 56 Gb/s NRZ eye diagram measured at -11.4 dBm. (b) 112 Gb/s PAM-4 eye diagram measured at -5.1 dBm. (c) 112 Gb/s NRZ eye diagram measured at -8.4 dBm. (d) 224 Gb/s PAM-4 eye diagram measured at -3.6 dBm with 6-tap FFE. (e) Measured 56 Gb/s and 112 Gb/s NRZ BER curves.(f) Measured 112 Gb/s and 224 Gb/s PAM-4 BER curves. Reproduced from [78].

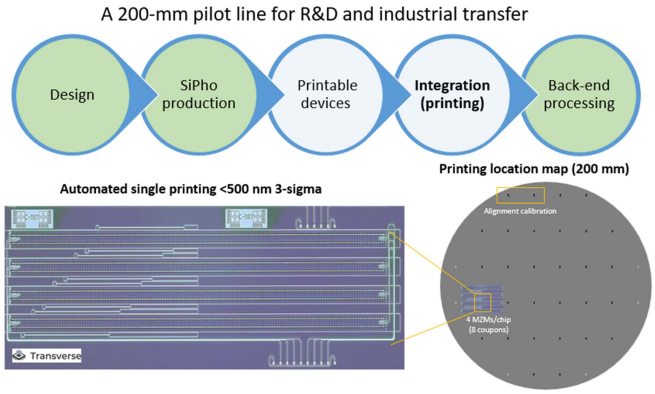


Fig. 19. Work flow of TRANSVERSE MTP pilot line (UGent - imec).

2) *Silicon photonics fabrication:* Foundry fabrication of the 200/300 mm target wafer with local recesses for coupon placement. Planarity and surface cleanliness are controlled to minimize bonding voids and ensure uniform adhesive thickness, enabling high-yield integration.
3) *Source wafer fabrication:* Source wafer preparation of coupons (e.g., III–V SOAs/EAMs/PDs, thin-film LN/LT, SiGe drivers/TIAs) with release layers, tether structures, and passivation. Electrical/optical pre-test enables known-good-die selection, which directly improves overall integration yield.
4) *Integration:* Automated MTP on predefined wafer sites with wafer-map driven alignment and periodic calibration. The tool achieves placement precision better than $\pm 0.5\,\mu$m (3σ) for arrays; adhesive deposition and cure (e.g., thin DVS-BCB) are tuned to balance coupling efficiency and void mitigation. Multi-coupon-per-die assembly is supported for complex PICs.
5) *Back-end processing:* Pad opening, metal interconnection to the target pads and passivation, followed by wafer-level optical/electrical testing. PCM readout feeds statistical process control loops. Now the wafers are ready for dicing, packaging, and final known good die selection.

Several challenges must be resolved for the commercial uptake of micro-transfer printing in the field of integrated photonics. The first and foremost aspect that needs to be tackled is the yield of MTP. The yield consists of several multiplicative aspects: (a) the yield of the coupons on the source wafer, including the yield of release; (b) the picking and printing process, where the former includes the tether break reproducibility, and the latter includes the alignment accuracy and bonding quality. As for the yield of the transfer-printing-compatible source wafers, established foundry techniques need to be utilized, including the design of customized layer stacks (for III-V, $LiNbO_3$, and other material systems) and the most advanced Front-End-of-Line fabrication. We are actively working with advanced III-V and LN foundries to address this.

One advantage of transfer printing is that the heterogeneous devices can be inspected and (partially) tested prior to integration, allowing only known-good dies to be picked and printed. This inherent strength can potentially significantly improve the overall system yield. However, it is actually an economic question whether the expense of the prior-integration test can make up for the cost of a lower yield without inspection/test. The yield of release processing is determined by the fraction of collapsed coupons on the source wafer after release layer etching. Wet chemical etching is currently employed to selectively etch the release layer in most material systems, which can induce coupon collapse due to stiction during the subsequent drying step due to liquid capillary forces. The number and mechanical strength of the tethers are also highly related to the yield; the tethers need to be strong enough to support the coupon during the release but must remain weak enough to be reliably broken during the picking operation.

Finally, the printing yield involves the printing alignment of the coupons and the bonding quality. Especially for evanescently coupled waveguide-in/out devices, including SOAs, EAMs, and thin-film modulators, the optical loss and device performance are susceptible to misalignment and the presence of voids at the bonding interface. Micro-transfer printing was originally envisioned purely as a mass transfer technology. The arrival of high-alignment-accuracy printing tools has unlocked the potential of the technology for heterogeneous silicon photonics integrated circuits. State-of-the-art MTP tools provide an alignment accuracy of $\pm\mathbf{0.5}\,\mu$m $(\mathbf{3}\sigma)$ while printing large arrays of devices. Consequently, the coupling interface between the coupon and the target waveguide needs to be designed with a misalignment tolerance to accommodate this tool limitation. The presence of voids at the bonding interface is a significant concern when the adhesive layer is required to be thin, which is necessary to maximize the coupling efficiency for evanescently coupled devices. Particles may already be present on the target wafer, necessitating a rigorous particle cleaning step before transfer printing. The second source of particles is debris generated during the coupon picking step when the tethers are broken. Therefore, ensuring a clean break and minimizing the overall number of tethers are potential solutions to mitigate particle-induced defects.

The second aspect is the performance and reliability of the transfer-printed devices. E.g. for the III-V transfer-printed lasers and SOAs, the performance and reliability needs to be optimized based on several elements: a) improvement of the III-V fabrication, which requires technology transfer to III-V foundries to utilize the most advanced and large-scale volume III-V processes; b) improvement of optical coupling efficiency between the III-V device and the silicon or silicon nitride waveguide, especially by using passive taper coupling structure with III-V regrowth; c) improvement of heat dissipation of transfer-printed devices. The several-micron-thick buried oxide layer of SOI and SiNOI wafers is the main source of thermal impedance, especially for evanescently coupled devices, which are printed on the front-end Si waveguide layer. This issue can be solved by connecting the heterogeneous active devices to the silicon substrate by thermal vias or flip-bonding the III-V/Si PIC onto a heat sink; d) bonding interface quality optimization to withstand thermal cycling and long-term high-temperature operation.

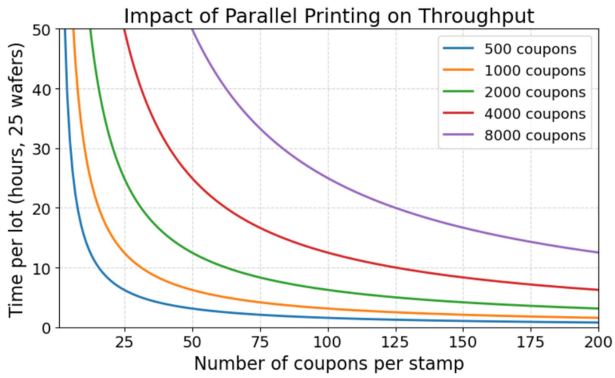


Fig. 20. MTP Throughput under different amounts of coupons per printing cycle.

The third aspect is the throughput of transfer printing. Micro-transfer printing has been widely used in μLED fabrication, where over 10,000 LED diodes can be integrated onto a substrate within one printing cycle, resulting in a volume of over millions of transfer-printed devices per hour. Fig. 20 presents the predicted throughput under different scaling of parallel printing, which reveals that parallel printing can significantly improve throughput. For the heterogeneous integration of various devices onto silicon photonics, the reasonable printing units are arrays up to reticle level. Meanwhile, multi-coupon printing not only requires the multi-post stamp fabrication with high accuracy but also requires a pitch and position match between the source and target wafers, which needs to be tackled during the design phase.

In order for micro-transfer printing technology to thrive and scale to industrial adoption, a comprehensive ecosystem must be established. This ecosystem should include:

- *Source wafer providers:* Suppliers of III-V, $LiNbO_3$, and other active material wafers prepared with release layers and tether structures for coupon fabrication.
- *Target wafer providers:* Foundries offering mature silicon photonics, silicon nitride, or other platforms with standardized recesses and metallization schemes for heterogeneous integration.
- *MTP processing lines:* Facilities equipped with high-precision micro-transfer-printing tools and wafer-level processing capabilities.

This ecosystem is currently under development through several EU-funded projects and bilateral engagement, aiming to enable high-volume manufacturing of heterogeneous photonic integrated circuits. Meanwhile, beyond infrastructure, standardization is critical to ensure interoperability between different vendors and platforms. Key areas for standardization include:

1) *Optical interface specifications:* Define coupling geometries, taper dimensions, and alignment tolerances between SiPh waveguides and transfer-printed coupons.
2) *Electrical interface specifications:* Standardize pad dimensions, metallization stack, and layout for electrical interconnection and on-wafer testing, especially for the high-speed devices.
3) *Coupon dimensions and array layout:* Establish uniform coupon sizes, and array pitch on source wafers to enable automated pick-and-place operations.
4) *Process Control Monitoring (PCM):* Define test structures and metrics for alignment accuracy, bonding quality, and optical/electrical performance verification.

Such standardization will allow coupons from different vendors to be integrated seamlessly onto SiPh wafers from multiple foundries using diverse MTP pilot lines. This approach will foster a multi-vendor supply chain, reduce integration complexity, and accelerate the commercialization of heterogeneous photonic systems-on-chip.

V. Conclusion

Micro-transfer printing is recognized as a promising and versatile heterogeneous integration technology crucial for the realization of advanced photonic systems-on-chip. MTP enables the deterministic, selective placement of pre-fabricated micro-components made from high-performance materials onto a large-scale, low-cost platform, such as silicon or silicon nitride photonics. Current demonstrations cover key proof-of-concept integrations, successfully merging materials with distinct functionalities onto a single platform, including InP, GaAs, $LiNbO_3$ and electronics. To transition MTP from the research laboratory to a commercially viable manufacturing process for high-volume production, several critical steps must be addressed to achieve technological maturity and industrial adoption. The primary challenges revolve around establishing a robust and scalable manufacturing ecosystem, and demonstrating yield, reliability and throughput. Standardization across these components is critical, including defining optical and electrical interface specifications and establishing common coupon dimensions and array layouts to ensure interoperability.

Acknowledgment

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