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Optimizing Pulse Conditions for Enhanced Memory Performance of Se-Based Selector-Only Memory

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ABSTRACT In this study, we investigated the effect of pulse falling time (T_{fall}) on the electrical characteristics of SiGeAsSe-based selector-only memory (SOM) devices. Our experimental results demonstrate that increasing the T_{fall} leads to an increased threshold voltage (V_{th}) and reduced V_{th} drift in SiGeAsSe devices. The optimized devices exhibit a remarkable memory window (> 1 V) and significantly suppressed drift characteristics (∼10 mV/dec.). Electrical measurements at high temperatures demonstrate that T_{fall} is one of the important factors in material relaxation, and these improvements are attributed to the intentionally induced reconfiguration of the chalcogenide film. Furthermore, our results reveal that a suitable T_{fall} can effectively mitigate the degradation of the memory window at high temperatures. These findings afford valuable insights into the role of material relaxation in SOM devices, potentially aiding the development of high-performance memory devices.

INDEX TERMS Chalcogenide, cross-point array (XPA), ovonic threshold switch (OTS), ReRAM, selector-only memory (SOM).

I. INTRODUCTION

To satisfy the increasing demand for high-performance memory in modern computing systems, a selector-only memory (SOM) operating with a chalcogenide-based ovonic threshold switch (OTS) has been proposed [1], [2], [3]. Owing to its simple structure, the cross-point array (XPA) with SOM can overcome various problems, such as void formation and thermal disturbances, which are found in conventional XPA composed of phase change memory (PCM) and OTS [4]. Moreover, its single-layer structure enables the implementation of a vertical-XPA (V-XPA) architecture for ultra-high-density memory devices [5].

SOM devices operate based on the polarity-induced threshold voltage (V_{th}) shift phenomenon of the OTS [6]. A write pulse with the same polarity as the read pulse results in a low V_{th} (State 1), whereas an opposite polarity induces a high V_{th} (State 2). Although SOM devices offer fast operating speed and excellent cycling endurance compared to traditional PCM-based devices [7], they still face several challenges, such as an insufficient memory window (MW).

Furthermore, material relaxation in chalcogenide-based memory devices is a critical issue that must be overcome to utilize SOM as a non-volatile memory component. This relaxation occurs due to the gradual disappearance of unstable homopolar bonds (e.g., Ge-Ge) present within the chalcogenide materials [8]. The short-range ordering due to this thermodynamic stabilization leads to an increase in film resistance and can result in operation failures during read

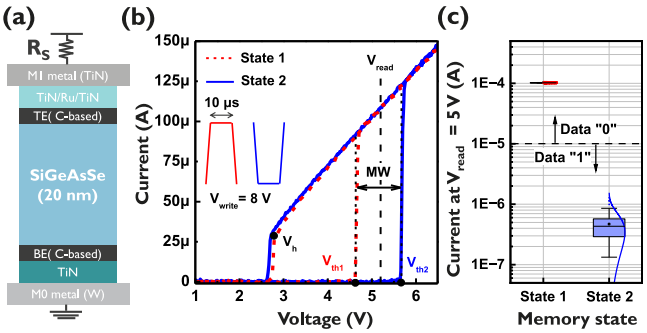

FIGURE 1. **(a) Schematic diagram and (b) typical AC I-V characteristics of a fabricated Se-based SOM device. (c) Current values at V_{read} based on the state of the memory device.**

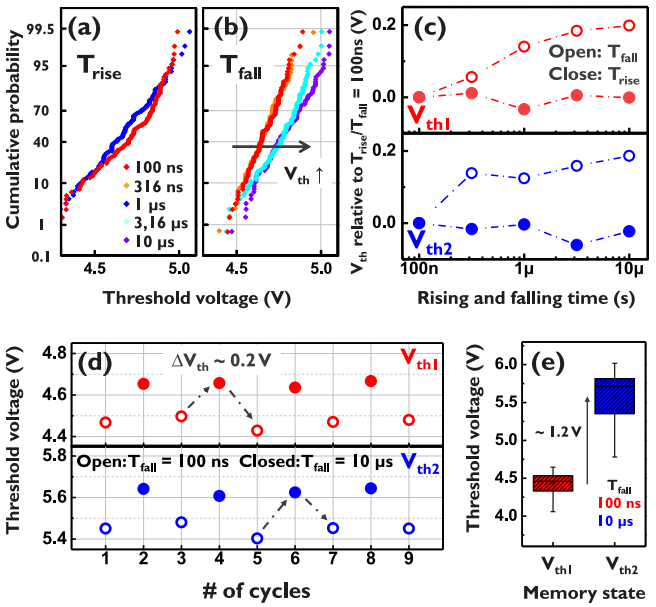

FIGURE 2. **V_{th} as a function of (a) T_{rise} and (b) T_{fall} of writing pulses. (c) Changes of V_{th} with T_{rise} and T_{fall} for two different memory conditions. The presented V_{th} represent the average values extracted from 100 cycling measurements for each pulse condition. V_{th} was unaffected by T_{rise} but strongly depends on T_{fall}. (d) Average value of V_{th1} and V_{th2} with alternate sequences of T_{fall}. The dependency of V_{th} on T_{fall} was reproducible and reversible. (e) MW at optimized T_{fall} for each state, showing excellent characteristics over 1.2 V.**

and write process. Therefore, it is necessary to identify the important factors that cause material relaxation and develop techniques to control them precisely.

To address these challenges and better understand the material relaxation in SOM devices, this study investigated the effect of falling time (T_{fall}) on the memory properties. Our results demonstrate that T_{fall} modulation enables MW optimization by controlling the V_{th}. In addition, by evaluating the V_{th} drift under various T_{fall} conditions, we found that increasing T_{fall} can successfully suppress the drift process. High-temperature (HT) measurements further reveal that the improved electrical performance is attributed to the intentionally accelerated relaxation of the chalcogenide film. Based on our experimental results, we propose a material relaxation model driven by the T_{fall} effect, providing deeper insights into the switching mechanisms. Our study offers practical guidelines for optimizing the applied pulse conditions, which can serve as a key factor in maximizing the memory performance and reliability of SOM devices.

II. EXPERIMENTAL DETAILS

An amorphous SiGeAsSe layer was deposited between a C-based top electrode (TE) and bottom electrode (BE) on a 300 mm wafer by using physical vapor deposition sputtering [2]. The stack was patterned into a pillar, with a critical dimension of 60 nm. An on-chip resistor ($R_s = 2.5$ kΩ), acting as a current limiter, was integrated into the device (**Fig. 1(a)**). Electrical characterization was performed using a Keysight B1530A Waveform Generation-Fast Measurement Unit (WGFMU).

For the write operation of the SOM, we applied square pulse with amplitude of $V_{write} = 8$ V and a width of 10 μs. To evaluate the effects of the rising time (T_{rise}) and T_{fall}, these times varied from 100 ns to 10 μs (denoted as T1 to T5). After the write operation, the V_{th} was extracted using a 10 μs triangular pulse with $V_{applied} = 10$ V. **Fig. 1(b)** shows typical AC current–voltage (I–V) characteristics of the fabricated SOM device. The device exhibited two distinct V_{th} values depending on the polarity of the applied write pulses (V_{th1} for State 1 and V_{th2} for State 2). Upon application of a read voltage (V_{read}) between the two V_{th} values, the current varied according to the memory state (**Fig. 1(c)**).

III. RESULTS AND DISCUSSIONS

A. ELECTRICAL PROPERTIES UNDER VARIOUS PULSE CONDITIONS

Figs. 2(a) and **2(b)** show the distribution of V_{th} across 100 cycles on a representative device, corresponding to varying T_{rise} and T_{fall}, respectively. Evidently, V_{th} was not affected by T_{rise} (**Fig. 2(a)**) but was strongly dependent on T_{fall} (as T_{fall} increased, V_{th} also increased; **Fig. 2(b)**) [9], [10]. These trends were consistent regardless of the memory state (**Fig. 2(c)**). These results indicate that T_{fall} is the determining parameter for V_{th}.

To verify whether V_{th} can be reversibly modulated, write pulses with T_{fall} of 100 ns and 10 μs were alternately applied. As shown in **Fig. 2(d)**, V_{th1} resulting from $T_{fall} = 100$ ns and $T_{fall} = 10$ μs differ by 0.2 V ($\Delta V_{th} \sim 0.2$ V), with the shifts in V_{th} appearing repeatedly. These modulations with T_{fall} can be utilized to maximize the MW of SOM devices. By applying the shortest T_{fall} during the write operation of State 1 and the longest T_{fall} during the write operation of State 2, the V_{th} difference can be increased, improving the MW over 1.2 V (**Fig. 2(e)**).

B. V_{TH} DRIFT CHARACTERISTICS AS A FUNCTION OF T_{FALL}

The drift phenomenon in chalcogenide-based memory and selector devices can be evaluated by measuring the dependency of V_{th} on the delay time (t_{delay}) between write and read operations [11]. In this case, the V_{th} drift follows the

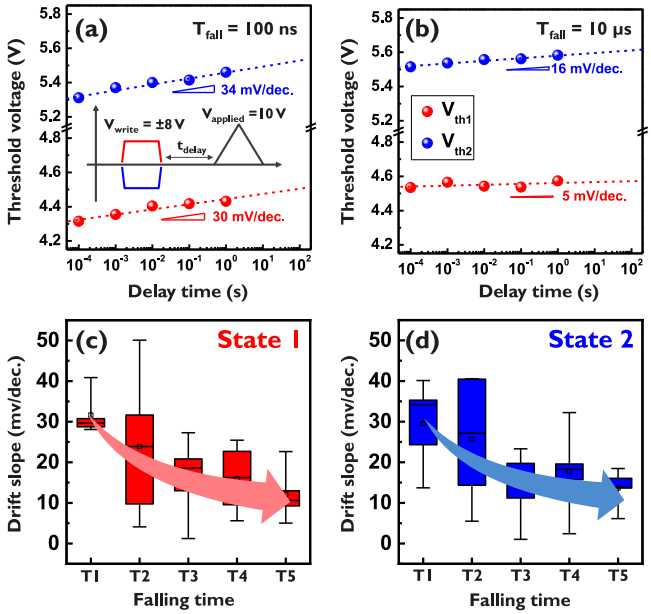

FIGURE 3. V_{th} drift as a function of t_{delay} at (a) T1 (= 100 ns) and (b) T5 (= 10 μs). As T_{fall} of writing pulses increased, the drift characteristic was successfully suppressed. Drift slope with T_{fall} in (c) State 1 and (d) State 2, showing that drift improved as T_{fall} increased regardless of the memory state.

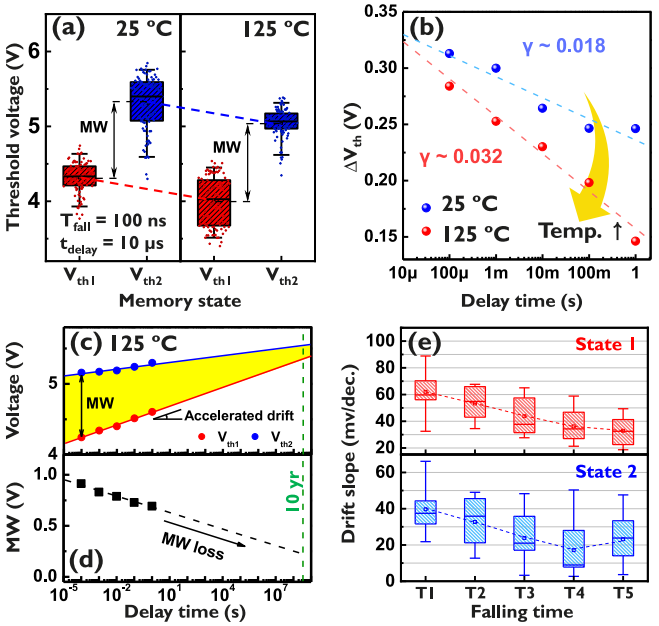

FIGURE 4. (a) 100 cycles of V_{th} and MW at 25 °C and 125 °C. (b) ΔV_{th} as a function of t_{delay}. At 125 °C, ΔVth decreased rapidly as t_{delay} increased. (c) V_{th} drift characteristics and (d) MW as a function of t_{delay} at 125 °C (T_{fall} = 100 ns). MW decreased dramatically as t_{delay} increased. (e) Drift slope at 125 °C with various T_{fall}. V_{th} Drift and MW can be improved at HT from T_{fall} adjustment.

equation below:

$$V_{th} = V_{th0} + \delta * \log\left(\frac{t}{t_0}\right) \quad (1)$$

where V_{th0} and t_0 are material constants, and δ is the characteristic exponent that controls the V_{th} drift [12]. We investigated the effect of T_{fall} on the drift by evaluating the device properties under various T_{fall} conditions. As shown in **Fig. 3(a)**, with a short T_{fall} = 100 ns, the V_{th} drift was approximately 30 mV/dec. for States 1 (red dots) and 2 (blue dots). For longer T_{fall} = 10 μs, the drift characteristics improved dramatically, regardless of the memory state (**Fig. 3(b)**). The SOM devices with optimized pulse condition exhibited an excellent V_{th} drift of less than 10 mV/dec. at a T_{fall} of 10 μs.

Fig. 3(c) and **Fig. 3(d)** show the drift slopes under various T_{fall} conditions for each memory state in 5 different dies. As T_{fall} increased from 100 ns to 10 μs, the drift improved by approximately 66%. Owing to the improvement in the drift characteristics under long T_{fall} operating condition, the SOM device can prevent retention failure.

C. TEMPERATURE DEPENDENCY OF T_{FALL} EFFECT

To understand the effect of T_{fall} on the amorphous chalcogenide films, HT measurement was performed. **Fig. 4(a)** shows the electrical characteristics of the SOM at 25 °C and 125 °C. V_{th} decreased at HT owing to accelerated electron hopping [13], [14]. Under a short t_{delay}, the MW remained stable regardless of the temperature (MW = 1 V). **Fig. 4(b)** illustrates the variation in ΔV_{th} with t_{delay} and temperature, showing that ΔV_{th} decreased as t_{delay} increased. This trend became more dramatic at HT. As mentioned in Section A, ΔV_{th} is defined as "V_{th} at T_{fall} = 10 μs - V_{th} at T_{fall} = 100 ns". This means that ΔV_{th} serves as a parameter representing the effect of T_{fall}. Therefore, the tendency for ΔV_{th} to decrease with the increase in t_{delay} and temperature indicates that, with the increase of these factors, the influence of T_{fall} on the chalcogenide film is reduced, explaining the mechanism behind the improved electrical properties.

Temperature and t_{delay} are key factors in determining the relaxation of the chalcogenide film. As t_{delay} increased, material relaxation occurred in the chalcogenide film, which was further accelerated at HT [15]. Therefore, based on t_{delay} and temperature dependence of ΔV_{th}, it can be confirmed that T_{fall} is another important factor influencing material relaxation.

Fig. 4(c) depicts the V_{th} drift as a function of t_{delay} at 125 °C. The drift characteristics exhibit different t_{delay} dependencies depending on the memory state, along with different temperature acceleration [16]. Notably, V_{th1} exhibited more rapid drift (compared to V_{th2}), leading to a reduction in MW as t_{delay} increased (**Fig. 4(d)**). This accelerated drift significantly deteriorates the retention properties. **Fig. 4(e)** shows the drift slope as a function of T_{fall} at HT, measured across 7 different dies. Drift can be improved by increasing T_{fall} in both memory states. Modulating these drift characteristics can improve device retention.

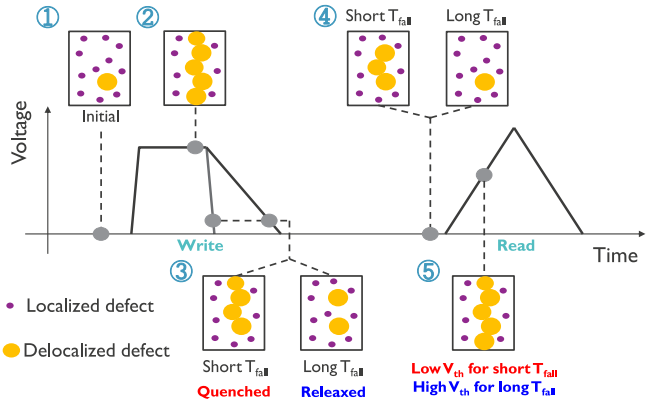

FIGURE 5. Schematic showing the material relaxation mechanism of T_{fall}. By applying a writing pulse having sufficient T_{fall}, the drift characteristics of the SOM devices can be significantly improved.

D. MECHANISM OF MATERIAL RELAXATION DRIVEN BY T_{FALL}

The physical mechanism underlying these phenomena is illustrated in **Fig. 5**, which shows a schematic of T_{fall}-induced material relaxation. After the forming process, a portion of delocalized defects remains within the chalcogenide film, as shown in the initial state in **Fig. 5**. When a write pulse is applied, localized defects transition into delocalized defects under the external electric field, switching the device to a low-resistance state. During the switch-off phase, these delocalized defects lose stability as the external electric field is removed and revert to initial localized defects [17].

For a short T_{fall}, insufficient time for transition causes delocalized defects to remain in a "quenched" state. In contrast, a longer T_{fall} allows adequate time for delocalized defects to revert back to localized defects and promotes the material relaxation via electrical and thermal effects [18]. Consequently, devices with a long T_{fall} exhibit a higher V_{th} in subsequent switching processes due to the reduced number of delocalized defects. Furthermore, even after a short t_{delay}, devices with a long T_{fall} demonstrate improved drift characteristics, as the chalcogenide film undergoes sufficient relaxation during switch-off phase.

IV. CONCLUSION

We demonstrated the impact of T_{fall} on the electrical properties of chalcogenide-based SOM devices. Our findings demonstrate that T_{fall} plays a crucial role in optimizing the performance of SOM devices. By increasing T_{fall}, we achieved a significant increase in V_{th} and a substantial reduction in drift, leading to a more stable and reliable memory operation. From the HT measurement, we revealed that T_{fall} is an essential parameter affecting material relaxation and confirmed that improvement in device performance could be attributed to intentional short-range ordering driven by increased T_{fall}. As a result of these changes, we have successfully improved the device characteristics without imposing additional circuit burdens. This understanding of the role of material relaxation can address the existing challenges in SOM devices for the development of high-performance memory technologies.

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