Electronics Letters

LETTER OPEN ACCESS

Full D-Band Superstrate-Enhanced Transition for Rectangular Waveguide-to-PCB Interfacing

Samuel Rimbaut | Kamil Yavuz Kapusuz | Hendrik Rogier | Sam Lemey

IDLab-Electromagnetics group, Department of Information Technology, Ghent University-imec, Ghent, Belgium

Correspondence: Samuel Rimbaut (samuel.rimbaut@ugent.be)

Received: 10 February 2025 | **Accepted:** 24 February 2025

Funding: This work was supported by the Bijzonder Onderzoeksfonds UGent (Grand number BOF/STA/202109/043).

ABSTRACT

A transition from air-filled rectangular waveguide (RWG) to substrate-integrated waveguide (SIW) is proposed that covers the entire D-band (110–170 GHz). Broadband operation is obtained by leveraging a resonant slot and an aperture-coupled patch antenna-in-waveguide, while co-optimisation with a dielectric-loading superstrate matches both resonances to the RWG and ensures full D-band operation. Special attention is devoted to the stringent design restrictions that originate from its implementation in a standard any-layer high density interconnect printed circuit board manufacturing process at D-band frequencies, omitting inductive via posts, to maximise the robustness of the design against fabrication tolerances. Measurements of the RWG-to-SIW transition demonstrate a fractional bandwidth of 46%, effectively covering the entire D-band, while ensuring a low insertion loss of 0.95 ± 0.15 dB.

1 | Introduction

Large-scale D-band (110–170 GHz) antenna arrays with highly directive adaptive beams are poised to play a pivotal role in next-generation communication and sensing systems [1]. To enable high data rates and low latency by fully exploiting the substantial bandwidths available within the D-band, several highly directive and efficient air-filled antenna arrays have been proposed, implemented through computerised numerical control (CNC) milling [2], 3D printing [3] or silicon micromachining [4]. Compactly integrating these arrays with steering electronics, however, requires a hybrid approach [5, 6], where such electronics are integrated on a printed circuit boards (PCBs) carrier. This, in turn, necessitates efficient, wideband transition structures to interface the on-PCBs steering electronics to rectangular waveguide (RWG) array structures.

Typically, such PCBss consist of several thin substrate layers to route the control and power lines [7] to the active electronics of the aforementioned communication and sensing circuits. To achieve a transition featuring a wide impedance bandwidth with minimum layer count on these PCBs carriers, end-launch transition designs [8–11] can be leveraged, though such substrate-integrate waveguide (SIW)-to-RWG transitions inevitably suffer from a large footprint in the planar dimensions and require a split-block implementation. Alternatively, in surface-mount transition designs [10, 12–23], enhancing the bandwidth is linked to the number of required layers. This leads to compact footprints, but increases insertion loss (IL) and manufacturing costs. Additionally, many of these designs employ inductive posts [12, 24, 25] or depth routing [25] to enhance the bandwidth, further complicating their design and making them more vulnerable to manufacturing tolerances, particularly at frequencies beyond 100 GHz [1, 26]. Finally, minimising the layer number, footprint and loss over a wide impedance bandwidth becomes imperative to enable a high performance, widely deployable transition.

We propose and validate a novel broadband RWG-to-SIW transition operating over the full D-band (110–170 GHz). By incorporating an aperture-coupled resonant patch with a resonant slot

TABLE 1 | Performance of state-of-the-art PCB-based vertical-mount millimetre wave transitions.

ref	f_0[GHz]	Topology	Size[λ_0^2]	# Metal layers	IL[dB]	FBW[%]
[12]	60	Slot + patch + inductive vias	0.99 × 0.84	4	0.58	35
[24]	60	Patch + inductive vias	0.89 × 0.6	2	0.5	**45.5**
[13]	90	Stepped impedance†	0.83 × 0.76	3	0.6	37.8
[25]	80	Patches + inductive vias	0.38 × 0.36	2	0.5	22
[14]	60	Patch + matching network	n/a	7	0.65	27
[15]	50	Probe + patch + Al block	1 × 0.42	3	2.2	42
[28]	**140**	Aperture + back cavity	1.18 × 0.53	2	1.1	10.1
[29]	**140**	RWG irises	n/a	2	2.5	35
T.W.	**140**	Patch + slot + superstrate	0.93 × 0.51	4	0.95	**46**

† indicates depth routing, Al = Aluminum.

and a dielectric-loading superstrate into the design, a −10 dB impedance bandwidth of 108–173 GHz (resulting in a fractional bandwidth (FBW) of 46 %) is achieved. The design also features an IL of only 0.95 ± 0.15 dB, which is the lowest found at D-band. In contrast to reference [24], where a similar fractional bandwidth is obtained at a lower frequency by depending on inductive vias, in this letter, a superstrate layer is applied instead to ensure wide-band operation in the D-band, while maintaining low insertion loss. As such, this transition, which can be reliably fabricated using standard high-density interconnect (HDI) PCBs technology [27], provides robust performance in a compact footprint. To the best of the author's knowledge, this is the first RWG-to-SIW transition that covers the entire D-band, while remaining fully compatible with HDI PCBs technology and additionally omitting critical via positioning to ensure maximum robustness against fabrication tolerances.

A plethora of advanced surface-mount RWG-to-planar waveguide transitions have been presented in the literature (see Table 1). These works show that aperture coupling of the on-PCBs waveguide to a resonant patch, which, in turn, couples to the RWG, is an effective strategy to interface on-PCBs components with RWG structures [12–14, 25]. However, these topologies are generally not sufficiently wideband to cover the entire D-band (FBW ≥ 43 %). Reference [24] makes use of inductive via posts to enhance the matching bandwidth. However, relying on the positioning of a single via makes the transition susceptible to fabrication tolerances at D-band frequencies. In reference [28], a transition relying on an aperture and a back cavity is proposed. Measurements agree well with simulations, suggesting a structure robust against tolerances, but its bandwidth is not yet sufficient for full D-band coverage. Reference [29] presents a microstrip-to-RWG transition that achieves a FBW of 35 % by introducing irises into the RWG. While this technique simplifies the on-PCBs design, tailored RWG sections must be manufactured to exploit this transition. Additionally, the resulting IL is higher.

2 | Transition Design

A full D-band interface between RWG components and PCBs structures, reliably manufacturable in HDI PCBs technology is targeted to achieve wideband interfacing of planar PCBs structures to RWG components in next-generation communication and sensing systems. Therefore, we propose an RWG-to-SIW transition that relies on the previously discussed combination of a resonant slot aperture and resonant patch element, enhanced by the inclusion of a superstrate layer. This additional layer acts as a dielectric load on the patch and slot resonances, which is leveraged to move them into the D-band frequency range, resulting in the desired full D-band coverage.

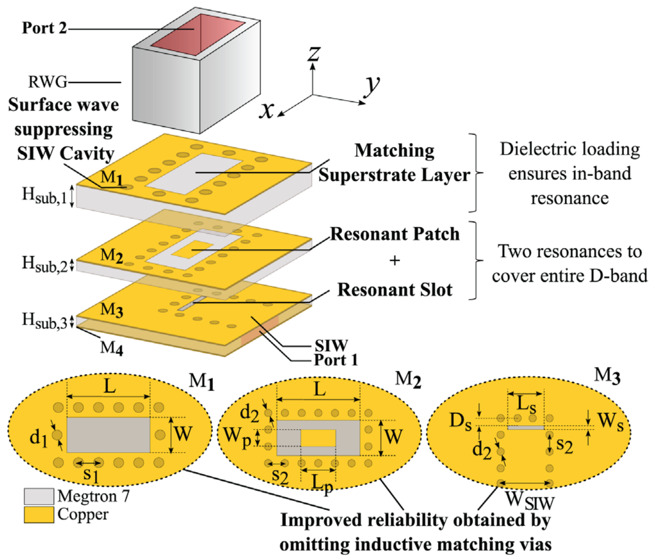

FIGURE 1 | Geometry of the proposed RWG-to-SIW transition employing a resonant patch and slot, co-optimised with a superstrate layer to match both resonances to the RWG and ensure full D-band operation. An SIW cavity is included to suppress surface wave propagation. Final dimensions: $L = 1.65$ mm, $W = 0.7$ mm, $L_p = 0.7$ mm, $W_p = 0.32$ mm, $d_1 = 0.2$ mm, $s_1 = 0.4$ mm, $d_2 = 0.15$ mm, $s_2 = 0.3$ mm, $L_s = 0.725$ mm, $W_s = 0.075$ mm, $W_{SIW} = 1.05$ mm, $D_s = 0.125$ mm, $H_{sub,1} = 136\,\mu$m, $H_{sub,2} = 102\,\mu$m and $H_{sub,3} = 102\,\mu$m. Megtron 7 substrate: $\epsilon_r = \mathbf{3.2}$, $\tan\delta = \mathbf{0.005}$, copper surface roughness: $R_a = 300$ nm.

The proposed RWG-to-SIW transition is shown in Figure 1, where the three crucial elements, being a resonant slot (M_3), a resonant patch (M_2) and a superstrate dielectric (M_1 - M_2), are

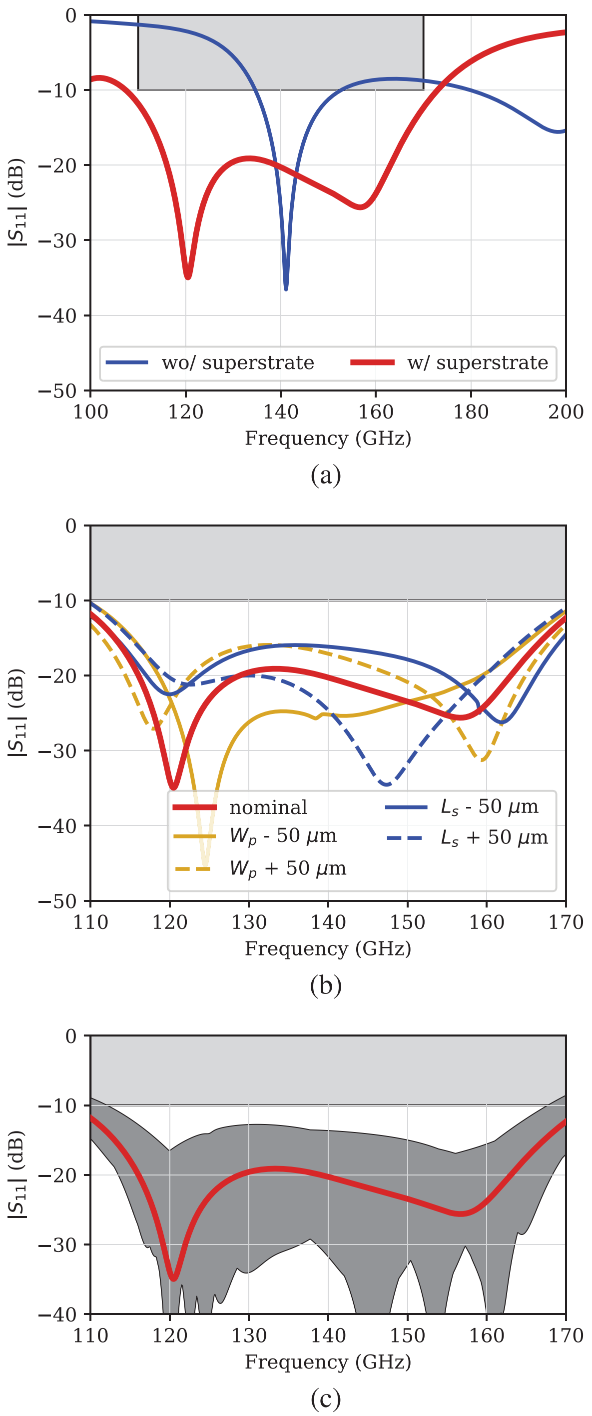

FIGURE 2 | Reflection coefficient $|S_{11}|$ of the RWG-to-SIW transition (a) indicating the nominal behaviour of the proposed transition (red curve) as well as its optimised performance when omitting the superstrate layer (b) effects of variations in the slot and patch dimensions, indicating their role in controlling the resonance frequencies and (c) variation analysis on all relevant transition dimensions, indicating the transition performance under the maximum expected fabrication tolerances.

indicated. The slot couples the TE_{10} mode of the SIW section, dimensioned for a cut-off frequency $f_c = 85$ GHz to ensure in-band linear phase behaviour, to the TM_{100} mode below the patch, which, in turn, interfaces to the RWG's TE_{10} mode. To indicate the necessity of the superstrate, Figure 2a indicates the nominal transition behaviour, as well as the behaviour of an optimised model in case the superstrate, and hence its dielectric loading, are omitted. Note that, for the latter, only the lower resonance peak can be positioned within the D-band, by controlling the patch width (W_p). The resonance resulting from the slot, however, remains out of band as the slot cannot be made long enough within the SIW section to achieve in-band resonance. By including additional dielectric loading, using a $H_{sub,1} = 136\,\mu$m thick superstrate, the slot resonance is shifted into the D-band, vastly improving the achievable bandwidth. A similar dielectric-loading effect may be obtained by increasing $H_{sub,2}$ instead, though this would strongly affect the coupling between the slot and patch structures, while also increasing the minimum manufacturable via diameter in this layer. Simulations of such a design indicate that expected variations in this thick substrate lead to substantial changes in transition behaviour, resulting in significantly reduced robustness.

After including the superstrate into the design, the resonance frequencies, the lower one being controlled by the patch width (W_p) and the upper one by the slot length (L_s), are distributed over the D-band to obtain the desired bandwidth. The optimal positions of the patch and slot resonances are found to be 120 and 157 GHz. This is indicated in Figure 2b, where variations of W_p and L_s are represented by the yellow and blue curves, respectively, to indicate how the two resonances are controlled.

A thorough fabrication tolerance analysis of the structure is performed using the frequency domain solver of CST Microwave Studio, with which we obtain the simulated reflection coefficient $|S_{11}|$ of the single-ended RWG-to-SIW transition shown in Figure 2c. Variations of 50 μm in slot, patch and cavity dimensions are considered, as well as 10 % variations in each substrate height, considering the input from the manufacturer [30]. The analysis demonstrates that the transition design is robust against variations in the nominal design parameters, with a minimum in-band matching of −9 dB only encountered at the band edges. The most sensitive parameter remains the positioning of the vias surrounding the cavity, which confirms the importance of replacing matching via posts by a dielectric-loading approach to ensure full D-band matching. However, since the average position of the via wall dominates matching, the dependence on the positioning of singular vias is still significantly reduced in the proposed design compared to an inductive via-based matching approach.

The nominal IL and the primary loss mechanisms are shown in Figure 3a, for a root-mean-square copper surface roughness profile of $R_a = 300$ nm (hyper very low profile copper foil) [31]. Furthermore, a simulated IL of only 0.65 dB (estimated to be composed of less than 0.35 dB dielectric loss, 0.1 dB conductor loss, 0.15 dB surface roughness loss and 0.05 dB mismatch loss) is achieved at 140 GHz, while remaining below 1.1 dB in the entire band of interest. Notably, of the 0.35 dB dielectric loss, only 0.06 dB is caused by the inclusion of the superstrate. The sensitivity analysis, considering the same variations as mentioned previously, is shown in Figure 3b. The variations result in a maximum in-band increase in IL of 0.5 dB, predominantly occurring at the edges of the operating band, due to a small frequency shift.

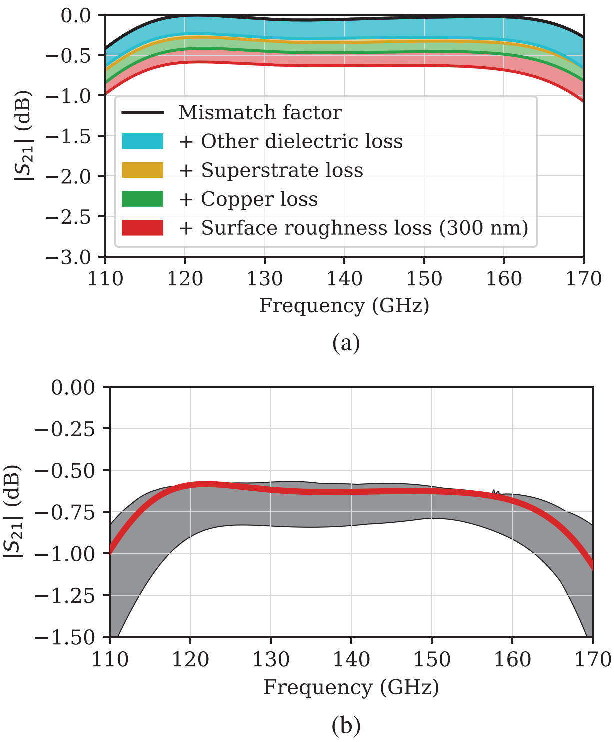

FIGURE 3 | Transmission coefficient $|S_{21}|$ of the transition (a) indicating the impact of every loss mechanism and (b) indicating variations on transmission performance under the maximum expected fabrication tolerances.

3 | Experimental Validation

To validate the performance of the transition, a back-to-back configuration is devised, as shown in Figure 4. Due to the substantial size of the waveguide flanges, the SIW section connecting the two transitions requires a minimum length L_{SIW} of 11 mm. For optimal proximity, the two transitions are positioned on opposite sides of the PCBs within the now eight-layer stack-up. To seamlessly connect both of these transitions with minimal impact on the behaviour of the back-to-back transition, additional slot-coupled SIW layer transitions were introduced in metal layers M_4 and M_5 (Figure 4). Subsequently, IL measurements were performed on SIW sections of lengths $L_{SIW} = 11.35$ and 13.75 mm, allowing the extraction of additional line length losses introduced by the SIW sections from the measurement results [32]. Figure 5a illustrates the prototype of the back-to-back transition, which was manufactured using a standard HDI PCBs fabrication process.

The S-parameters were measured using a Keysight N5242B PNA-X microwave network analyser, coupled with Virginia Diode Incorporated (VDI)'s D-band VNA extenders [33] and WR-6.5 RWGs. Figure 6 shows the measurement setup, including the thru-reflect-line (TRL) calibration reference planes and the associated signal transitions.

Figure 7 depicts the measured S-parameters, showing that the back-to-back reflection coefficient closely matches the simulation across the entire D-band. The average IL of the 11.35 and 13.75 mm lines equal 5.2 and 6 dB, respectively, yielding a measured SIW loss in the Megtron 7 substrate of 0.33 dB/mm,

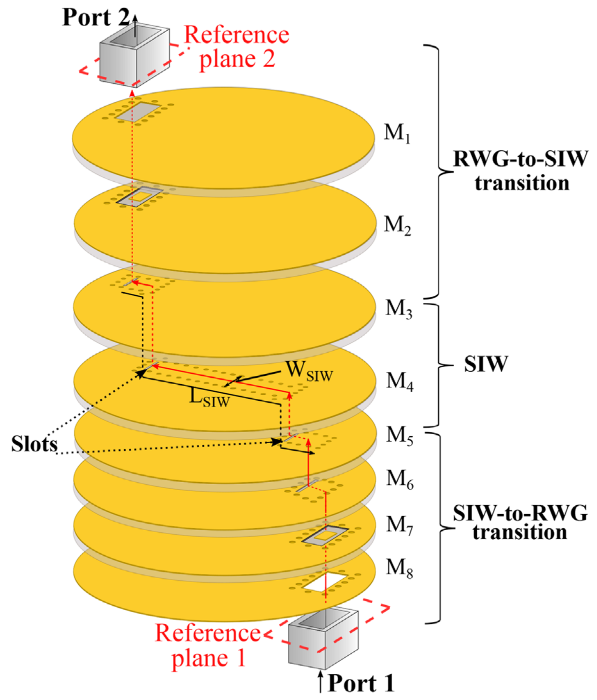

FIGURE 4 | Back-to-back RWG-to-SIW transition connected by an SIW section of length L_{SIW}.

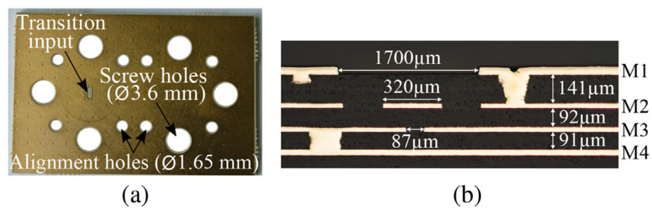

FIGURE 5 | Fabricated back-to-back RWG-to-SIW transition. (a) Top view of the PCBs with waveguide flange alignment and screw holes. (b) scanning electron microscope (SEM) image of the cross-section indicating the average measured patch, slot, cavity and dielectric height dimensions.

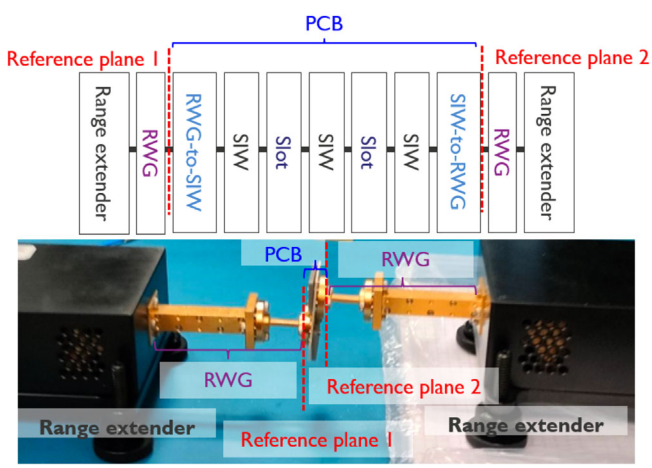

FIGURE 6 | Measurement setup and waveguide transition diagram.

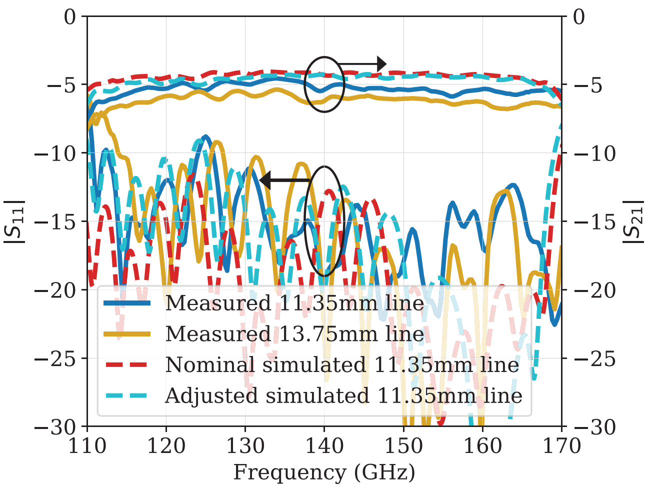

FIGURE 7 | Scattering parameters of the back-to-back transitions in case of a (blue) measured 11.35 mm long line, (yellow) measured 13.75 mm long line, (red) simulated 11.35 mm long line with nominal design values and (cyan) simulated 11.35 mm long line with measured design values, as shown in Figure 5b.

compared to 0.28 dB/mm in simulation. Therefrom, the single-ended transition's average measured IL is calculated to be 0.95 dB, which is slightly higher than the simulated IL of 0.65 dB. This discrepancy is attributed to slightly higher substrate, conductor and surface roughness losses, which also contribute to the increased SIW loss. The average in-band deviation of the IL is found to be 0.15 dB.

Finally, to evaluate the potential extent of fabrication errors, cross-sections of several manufactured test boards were examined under a scanning electron microscope (SEM), as illustrated in Figure 5b.

Measurements revealed that the dielectric layer thickness exhibits a worst-case variation of ±11 μm. The patch length and width vary at most ±12 μm. Moreover, the slot length and width vary by ±25 μm and ±12 μm, respectively, justifying the limits for the corner analysis in simulations. When comparing the measured $|S_{11}|$ (solid blue line) to the nominal simulated results of the final design (dashed red line), with dimensions as depicted in Figure 1, a slight discrepancy is observed. Yet, when manufacturing errors are incorporated into the simulation model (dashed cyan line), the measured −10 dB impedance bandwidth and IL align well with the simulation, covering the 110–170 GHz band. Minor discrepancies between the simulated and measured curves persist, possibly due to variations in the surface roughness profile.

4 | Conclusion

A novel broadband RWG-to-SIW transition with a bandwidth of 46% for $|S_{11}| < -10$ dB was proposed to cover the entire 110–170 GHz band by incorporating an aperture-coupled resonant patch and resonant slot with a dielectric-loading superstrate. Measurements and simulations align well, exhibiting an IL of less than 0.95 ± 0.15 dB. With its compact structure, ease of integration, wide bandwidth, and low IL, this transition is a highly appealing component for interfacing planar PCBs structures to RWG components in next-generation communication and sensing systems.

Author contributions

Samuel Rimbaut: conceptualization, formal analysis, investigation, methodology, supervision, validation, visualization, writing – original draft. **Kamil Yavuz Kapusuz:** conceptualization, supervision, writing – review and editing. **Sam Lemey:** funding acquisition, supervision, writing – review and editing. **Hendrik Rogier:** funding acquisition, supervision, writing – review and editing.

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

1. M. de Kok, A. B. Smolders, and U. Johannsen, "A Review of Design and Integration Technologies for D-Band Antennas," *IEEE Open Journal of Antennas and Propagation* 2 (2021): 746–758.

2. W. Tan, Y. Xiao, C. Li, K. Zhu, H. Luo, and H. Sun, "A Wide-Band High-Efficiency Hybrid-Feed Antenna Array for mm-Wave Wireless Systems," *Electronics* 10, no. 19 (2021), https://www.mdpi.com/2079-9292/10/19/2383.

3. Y. Li, L. Ge, J. Wang, S. Da, et al., "3-D Printed High-Gain Wideband Waveguide Fed Horn Antenna Arrays for Millimeter-Wave Applications," *IEEE Transactions on Antennas and Propagation* 67, no. 5 (2019): 2868–2877.

4. A. Gomez-Torrent, T. Tomura, W. Kuramoto, et al., "A 38 dB Gain, Low-Loss, Flat Array Antenna for 320–400 GHz Enabled by Silicon-on-Insulator Micromachining," *IEEE Transactions on Antennas and Propagation* 68, no. 6 (2020): 4450–4458.

5. A. Vosoogh M. S. Sorkherizi, V. Vassilev, et al., "Compact Integrated Full-Duplex Gap Waveguide-Based Radio Front End for Multi-Gbit/s Point-to-Point Backhaul Links at E-band," *IEEE Transactions on Microwave Theory and Techniques* 67, no. 9 (2019): 3783–3797.

6. M. Peeters, S. Sinha, X. Sun, et al., "(Why do We Need) Wireless Heterogeneous Integration (Anyway?)," in *2022 IEEE Symposium on VLSI Technology and Circuits* (IEEE, 2022), 256–257.

7. A. R. Vilenskiy and Y. Zhang, "A Compact and Wideband MMIC-to-Ridge Gap Waveguide Contactless Transition for Phased Array Antenna Front Ends," *IEEE Antennas and Wireless Propagation Letters* 23, no. 3 (2024): 990–994.

8. Y. Zhang, S. Shi, R. D. Martin, and D. W. Prather, "Broadband SIW-to-Waveguide Transition in Multilayer LCP Substrates at W-Band," *IEEE Microwave and Wireless Components Letters* 27, no. 3 (2017): 224–226.

9. Q. Xu, Z. Jiang, and C. Guo, "A Design of Waveguide-to-Microstrip Transition for V-Band Device Testing," in *2022 ICMMT* (IEEE, 2022), 1–3.

10. A. Hassona, Z. S. He, V. Vassilev, and H. Zirath, "D-Band Waveguide Transition Based on Linearly Tapered Slot Antenna," in *2017 IMAPS NordPac* (IEEE, 2017), 64–67.

11. H. Lee, S. Yun, M. Uhm, and I. Yom, "Full-Band Transition From Substrate Integrated Waveguide to Rectangular Waveguide," *Electronics Letters* 51, no. 14 (2015): 1089–1090.

12. Y. Li and K.-M. Luk, “A Broadband V-Band Rectangular Waveguide to Substrate Integrated Waveguide Transition,” *IEEE Microwave and Wireless Components Letters* 24, no. 9 (2014): 590–592.

13. S. Hansen and N. Pohl, “A W-Band Stepped Impedance Transformer Transition From SIW to RWG for Thin Single Layer Substrates With Thick Metal Cladding,” in *2019 49th EuMC* (IEEE, 2019), 352–355.

14. Y. Chen, K. Ma, and Y. Wang, “A Novel V-Band Substrate Integrated Suspended Line to Rectangular Waveguide Transition,” in *2018 IEEE/MTT-S IMS* (IEEE, 2018), 186–189.

15. Hafeez-Ur-Rehman, H. I. Song, S. Park, and J.-H. Jang, “Broadband Partially Covered Microstrip-to-Waveguide Transition With Enhanced Radiation Suppression for Millimeter-Wave Transmission,” *IEEE Microwave and Wireless Technology Letters* 34, no. 4 (2024): 367–370.

16. C.-Y. Yang, G.-T. Zeng, H. N. Chu, and T.-G. Ma, “A Compact D-Band Transition From Rectangular Waveguide to Substrate Integrated Waveguide,” in *2021 ISAP* (IEEE, 2021), 1–2.

17. S. R. Zahran, S. Moscato, A. Fonte, et al., “Flippable and Hermetic E-Band RWG to GCPW Transition With Substrate Embedded Backshort,” *IEEE Microwave and Wireless Components Letters* 71, no. 6 (2023): 2582–2593.

18. K. Liu, P. Wu, and J. Zhang, “Wideband RWG-SIW Interconnection With Improved Integration for Millimeter-Wave/Terahertz Application,” *IEEE Microwave and Wireless Components Letters* 32, no. 7 (2022): 835–838.

19. S. Lu, Y. Shen, Y. Ding, and S. Hu, “D-Band GCPW-to-Waveguide Transition Using Silicon Micromachined Technology for Planar Integrated MMIC and Aperture Antenna,” *IEEE Antennas and Wireless Propagation Letters* 23, no. 12 (2024): 4842–4846.

20. A. Altaf, M. Elahi, S. M. Abbas, J. Yousaf, and E. Almajali, “A D-Band Waveguide-SIW Transition for 6G Applications,” *Journal of Electromagnetic Engineering and Science* 22, no. 4 (2022): 419–426.

21. T. Li and W. Dou, “Broadband Right-Angle Transition From Substrate-Integrated Waveguide to Rectangular Waveguide,” *Electronics Letters* 50, no. 19 (2014): 1355–1356.

22. W. Abdel-Wahab, A. Ehsandar, H. Al-Saedi, and S. Safavi-Naeini, “E-Plane Metallic RWG-to-SIW Transition for Large-Scale mm-Wave Phased Array Antenna Applications,” *Electronics Letters* 52, no. 17 (2016): 1465–1467.

23. G. Zhang, H. Yi, S. Wang, and M. Han, “Broadband Right-Angle Transition From Substrate Integrated Waveguide to Rectangular Waveguide,” *Electronics Letters* 53, no. 7 (2017): 473–475.

24. I. Mohamed and A. Sebak, “Broadband Transition of Substrate-Integrated Waveguide-to-Air-Filled Rectangular Waveguide,” *IEEE Microwave and Wireless Components Letters* 28, no. 11 (2018): 966–968.

25. K. Zhu, Y. Xiao, W. Tan, H. Luo, and H. Sun, “A Broadband E-Band Single-Layer-SIW-to-Waveguide Transition for Automotive Radar,” *IEEE Microwave and Wireless Components Letters* 32, no. 6 (2022): 523–526.

26. J. Coonrod, “Theory vs. Reality: Using Printed Circuit Board Technology for Grounded Coplanar Waveguide at Millimeter-Wave Frequencies: Understanding PCB Technology for Millimeter-Wave Applications,” *IEEE Microwave Magazine* 25, no. 5 (2024): 24–35.

27. “IPC International, inc. sectional design standard for high density interconnect (HDI) printed boards,” accessed on February 4, 2025, https://www.ipc.org/TOC/IPC-2226A.pdf.

28. Z.-Q. Zhang, X.-L. Huang, L. Zhou, Y.-S. Huang, and C.-R. Zhang, “A D-Band Self-Packaged Low Loss Grounded Coplanar Waveguide to Rectangular Waveguide Transition With Silicon-Based Air Cavity-Backed Structure,” *IEEE Journal of Microwaves* 4, no. 4 (2024): 767–776.

29. M. Schepers and C. Krebs, “Right-Angle D-Band Differential Microstrip to Waveguide Transition With Irises,” in *2024 54th European Microwave Conference (EuMC)* (IEEE, 2024), 7–10.

30. “Aspocomp website,” accessed on February 4, 2025, https://aspocomp.com.

31. A. Lamminen, J. Säily, J. Ala-Laurinaho, J. de Cos, and V. Ermolov, “Patch Antenna and Antenna Array on Multilayer High-Frequency PCB for D-Band,” *IEEE Open Journal of Antennas and Propagation* 1 (2020): 396–403.

32. F. Declercq, H. Rogier, and C. Hertleer, “Permittivity and Loss Tangent Characterization for Garment Antennas Based on a New Matrix-Pencil Two-Line Method,” *IEEE Transactions on Antennas and Propagation* 56, no. 8 (2008): 2548–2554.

33. “Virginia Diode Incorporated Website,” accessed on February 4, 2025, https://www.vadiodes.com/en.