Hybrid and heterogeneous photonic integration

Cite as: APL Photon. 6, 061102 (2021); doi: 10.1063/5.0052700
Submitted: 1 April 2021 • Accepted: 31 May 2021 •
Published Online: 28 June 2021

View Online Export Citation CrossMark

Paramjeet Kaur,[1] Andreas Boes,[1,a)] Guanghui Ren,[1] Thach G. Nguyen,[1] Gunther Roelkens,[2] and Arnan Mitchell[1,b)]

AFFILIATIONS

[1] School of Engineering, Integrated Photonics and Applications Centre, RMIT University, Melbourne, VIC 3001, Australia
[2] Photonics Research Group, Department of Information Technology, Ghent University–imec, Ghent, Belgium

[a)] **Author to whom correspondence should be addressed:** andreas.boes@rmit.edu.au
[b)] **Electronic mail:** arnan.mitchell@rmit.edu.au

ABSTRACT

Increasing demand for every faster information throughput is driving the emergence of integrated photonic technology. The traditional silicon platform used for integrated electronics cannot provide all of the functionality required for fully integrated photonic circuits, and thus, the last decade has seen a strong increase in research and development of hybrid and heterogeneous photonic integrated circuits. These approaches have enabled record breaking experimental demonstrations, harnessing the most favorable properties of multiple material platforms, while the robustness and reliability of these technologies are suggesting entirely new approaches for precise mass manufacture of integrated circuits with unprecedented variety and flexibility. This Tutorial provides an overview of the motivation behind the integration of different photonic and material platforms. It reviews common hybrid and heterogeneous integration methods and discusses the advantages and shortcomings. This Tutorial also provides an overview of common photonic elements that are integrated in photonic circuits. Finally, an outlook is provided about the future directions of the hybrid/heterogeneous photonic integrated circuits and their applications.

© 2021 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/). https://doi.org/10.1063/5.0052700

I. INTRODUCTION

Integrated circuit technology has underpinned the information revolution, enabling our computers, our smart phones, and the information superhighway that connects us. From the very early stages of this technology, there has been a push to have more and more functionalities *monolithically integrated* with ever more complex circuits using the same material and technology platform. However, traditional technology platforms have matured and reached a plateau primarily limited by the bandwidth constraints imposed by electronic input/output interfaces. The need to overcome this electronic bottleneck has led to the advent of integrated photonics with the aim of providing a direct interface to the vast bandwidth that is currently available with fiber optics.

Optical fiber systems are typically composed of discrete elements, such as lasers, modulators, and detectors often packaged in a rack scale module. Photonic integrated circuits (PICs) are particularly attractive as they can shrink down these rack scale photonic modules to a chip the size of a thumb nail—similar to the integrated electronics that they interface. The integration of such systems on a chip comes with additional benefits, such as energy efficiency, robustness, weight reduction, and ultra-fast feedback control. In the laboratory, these properties have enabled unprecedented scientific demonstrations, such as chip-scale optical frequency synthesizers,[1] battery operated optical frequency comb sources,[2] and high-speed optical communication experiments.[3] Industrially, companies, such as Cisco, Juniper, Infinera Corporation, and Huawei,[4] are already offering commercial products using PICs for broadband interfacing of electronics; however, many are exploring the potential of PICs for more sophisticated information processing functionalities as well.

PICs with many different waveguide material technologies have been investigated over the years, such as silicon (Si),[5,6] silicon nitride (Si_3N_4),[7–9] doped silicon dioxide (SiO_2),[10] gallium arsenide (GaAs),[11,12] indium phosphide (InP),[13–15] lithium niobate ($LiNbO_3$),[16] aluminum nitride (AlN),[17–19] and gallium nitride (GaN).[17–19] Arguably, the most prominent waveguide material technology is silicon. The benefit of silicon is the availability of high-quality wafer scale silicon thin-films, which can be patterned with mature fabrication processes, due to the fabrication advances of the complementary metal–oxide–semiconductor (CMOS)

technology driven by the demand of consumer electronics and the potential to monolithically integrate silicon electronics and photonics on the same platform.[20] However, over the years, it also became clear that silicon cannot fulfill the needs for all applications that would benefit from PICs. For example, it is difficult to achieve light sources in silicon due to its indirect bandgap. Silicon also suffers from two photon absorption (TPA) at typical communication wavelengths, which makes it difficult to be used for nonlinear optical applications.[21,22] Other waveguide materials may overcome some of the shortcomings of silicon, but they may have other limitations for the target applications. Current trends in PIC material technologies indicate that there is no waveguide material technology that can address the needs for all the potential applications of PICs. Furthermore, advanced PICs may require the best possible performance of a large number of different photonic elements in a PIC to achieve the desired functionality, which may not be possible with a single waveguide material technology.

A solution to overcome this limitation is to integrate different material technologies into a single PIC or package. This approach has the benefit that each material can be used to provide the photonic element functionality for which it is best suited without compromising the functionalities of the other elements in the system. The integration of the different material technologies can be distinguished by two different integration processes: (i) hybrid integration and (ii) heterogeneous integration.

In this Tutorial, we provide an overview of the hybrid and heterogeneous photonic integration. In Sec. II, we examine different material technologies that are relevant for hybrid/heterogeneous integration. Section III gives a brief introduction into hybrid and heterogeneous integration, and Sec. IV describes diverse ways different material technologies can be interfaced with each other to allow for low loss transitions among them. In Sec. V, we analyze the different integration methods that can be used for the hybrid/heterogeneous integration of photonic circuit elements. Section VI gives an overview of hybrid and heterogeneous integration examples for real world applications, and Sec. VII takes a look into future trends before concluding in Sec. VIII.

II. MATERIAL TECHNOLOGIES

Many different material technologies have been investigated in the decades of research on PICs, motivated by the aim of utilizing the best available material properties for a specific application. Some of the most important material properties for PICs are the refractive index, transparency across various wavelength ranges, the direct/indirect semiconductor bandgap, nonlinear optical properties [$\chi^{(2)}$ and $\chi^{(3)}$], the electro-optic coefficient, the piezoelectric coefficient, the thermo-optic coefficient, acousto-optic properties, and low waveguide propagation losses. It should be noted that this is not a complete list of materials and platform properties that are attractive for PICs but are some of the most important ones and will be further examined in the following.

The refractive index is an important material property for most optical waveguide platforms as it defines the achievable refractive index contrast between waveguide core and surrounding materials. A higher refractive index contrast is beneficial to achieve a tight waveguide bending radius and, therefore, a high integration density as well as the ability to confine the optical waveguide mode tightly.

The width of the waveguide material bandgap is an important parameter for several different applications: (i) it defines the lower edge of the wavelength transmission window of a material and therefore the shortest wavelength ($\lambda_1 > \frac{hc}{E_g}$) that the material can be used for as an optical waveguide without suffering from high optical losses due to the absorption [see Fig. 1(a)]; (ii) for semiconductor photodetectors, it defines the longest wavelength ($\lambda_1 < \frac{hc}{E_g}$) of detectable photons as the absorbed photons create free charge carriers (electron–hole pairs), which generate a current signal when the detector material is biased with a voltage [see Fig. 1(a)]; (iii) for nonlinear optical applications, it defines the shortest wavelength ($\lambda_2 > \frac{2hc}{E_g}$) at which two photon absorption (TPA) can occur [see Fig. 1(d)]; and (iv) for semiconductor light sources and amplifiers, the bandgap defines the emission wavelength ($\lambda_1 = \frac{hc}{E_g}$) when charge carriers recombine [see Fig. 1(b)]. In this fourth category, electrically driven coherent light emission and amplification are generally limited to direct bandgap materials [materials where the maximum of the valence band and the minimum of the conduction band have the same crystal momentum (k) in the Brillouin zone, e.g., GaAs and InP] such that photons can directly stimulate the emission of photons with the same energy and phase [see Fig. 1(b)]. For materials with an indirect bandgap [Fig. 1(c)] [materials where the maximum of the valence band and the minimum of the conduction band have different crystal momentum (k) in the Brillouin zone, e.g., Si and Ge], while it is possible for photons to be absorbed by the generation of electron hole pairs via the generation of a phonon (heat), which makes up the momentum mismatch, it is not possible for a photon to directly stimulate another coherent photon in an indirect bandgap material as this would rely on the presence and absorption of phonons of the appropriate phase and momentum, but as phonons are incoherent and thermal in nature, such transitions are statistically rare.[23,24]

High nonlinear optical coefficients are desirable for generating new wavelengths. The $\chi^{(2)}$ optical nonlinearity enables nonlinear optical processes, such as second harmonic generation (SHG), sum frequency generation (SFG), parametric down-conversion (PDC), and difference frequency generation (DFG)[25] as well as cascaded processes that can emulate $\chi^{(3)}$ nonlinear optical processes.[26,27] Such processes are particularly attractive for optical signal processing in communications[26,27] and the generation of entangled photon pairs for quantum optical applications.[28] $\chi^{(3)}$ nonlinear optical processes, which are caused by the Kerr effect, include self-phase modulation (SPM), cross phase modulation (XPM), and four wave mixing (FWM). Nonlinear refractive index n_2 is used as a parameter for quantifying the Kerr nonlinearity of a medium. One of the most prominent uses of this nonlinearity at present is the generation of optical frequency combs by using micro-resonators.[29,30]

Materials with a high electro-optic coefficient are important for applications that require fast manipulation of the optical wave's phase. Electro-optic materials exhibit the Pockels effect, which changes the refractive index of the material, when an electric field is applied. The refractive index change occurs without a change in the imaginary refractive index (no additional absorption). The instant changes to the refractive index and the ability to phase match the electrical wave with the optical wave to achieve traveling wave

© Author(s) 2021

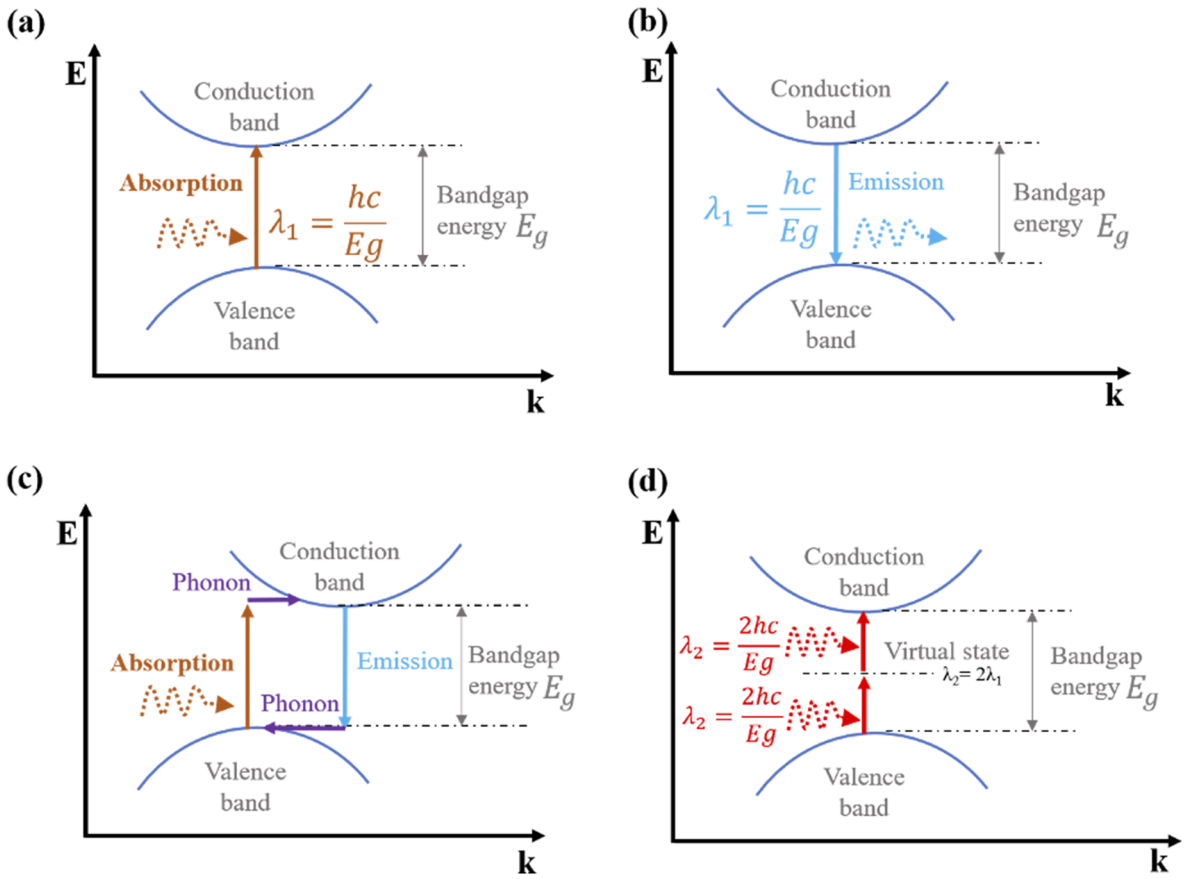

FIG. 1. Illustration of direct bandgap (a) absorption and (b) emission processes. (c) Indirect bandgap absorption and emission processes. (d) Two photon absorption process.

modulators make this process very attractive, and modulation speeds exceeding 100 GHz are feasible.[31,32]

Most materials will also change their refractive index with temperature, and this characteristic is termed the thermo-optic coefficient. A large thermo-optic coefficient can be both an advantage and a disadvantage. For example, a large thermo-optic coefficient is attractive to tune ring resonators[33] or even as low speed optical modulators.[34] One the other hand, a large thermo-optic coefficient can result in significant changes in the behavior of the components on a PIC as the ambient temperature changes. If a PIC material has a relatively high thermo-optic coefficient and the stability of the PIC is very important, then the PIC will typically be packaged with an active temperature controller so that the functionality of the circuit is not impacted. This can introduce additional overhead in terms of size, weight, cost, and power consumption, which can make them less attractive for certain applications.

Some materials will deform mechanically upon application of an electric field, which is characterized by a piezoelectric coefficient. Piezoelectric materials are generally crystals that are non-centrosymmetric, including lead zirconate titanate (PZT), $LiNbO_3$, AlN, and quartz among others. Mechanically deforming optical waveguides are attractive as it can be used to slightly change the length of a waveguide structure (e.g., ring resonator[35]), which can be used for tuning. The piezoelectric effect in waveguide materials can also be used to generate acoustic waves, which enable device functionalities, such as acousto-optical modulators[36] and acousto-optical frequency shifters.[37]

Extremely low optical propagation loss (0.14 dB/km[38]) has been instrumental in the success of optical fibers, but it has only recently become possible to achieve low losses (dB/m) in PICs. Low losses can be important to maintain power budgets on transmission through a PIC; however, recently, losses have become sufficiently low to enable long optical delay lines on a chip with applications, including gyroscopes[39] and microwave photonics.[40] Ultra-low waveguide losses (dB/m) are also required for the integration of high-quality factor ring resonators that can be used for the efficient generation of optical frequency combs.[41]

Table I lists some of the most commonly used optical waveguide materials together with the material properties as discussed above and common material technology parameters, such as mode size and waveguide losses, which enable us to compare different waveguide materials. We have also included two material technologies (GaAs and $LiNbO_3$), which had originally been demonstrated on native substrates (GaAs) or as a diffused waveguide ($LiNbO_3$),

© Author(s) 2021

TABLE I. Overview of various photonic integration technology properties. Lithium niobate ($LiNbO_3$) and aluminum nitride (AlN) are birefringent materials, which possess an ordinary refractive index (n_o) and an extraordinary refractive index (n_e).

Material property/ technology parameter	Silicon (SiO_2 BOX)	Si_3N_4 (SiO_2 BOX)	SiO_2 (doped)	GaAs (native grown)	GaAs (SiO_2 BOX)	InP (native grown)	$LiNbO_3$ (doped)	$LiNbO_3$ (SiO_2 BOX)	AlN (SiO_2 BOX)
Refractive index (at 1.55 μm)	3.47	2.00	1.45	3.67	3.67	3.17	$n_o = 2.21$ $n_e = 2.14$	$n_o = 2.21$ $n_e = 2.14$	$n_o = 2.12$ $n_e = 2.16$
Refractive index contrast (at 1.55 μm)	2.2	0.53	0.003–0.011[10]	0.233[42]	2.22	0.03–0.77[43]	0.02[44]	~0.7[45]	~0.7
Bandgap	1.14 eV (1.09 μm)	5.0 (0.25 μm)	9.3 eV (0.13 μm)	1.43 eV (0.86 μm)	1.43 eV (0.86 μm)	1.34 eV (0.93 μm)	3.7 eV (0.34 μm)	3.7 eV (0.34 μm)	6.0 eV (0.21 μm)
Bandgap	Indirect	Indirect	Indirect	Direct	Direct	Direct	Indirect	Indirect	Direct (wurtzite)
Two photon absorption (at 1.55 μm) (cm/GW)	1.5[22]	0[46]	...	27[47]	27[47]	24–33[48]	...	...	...
Second order nonlinearity d [1/2 $\chi^{(2)}$] (pm V^{-1})	...	...	...	119[49]	119[49]	...	$d_{22} = 2.1$[50]	$d_{22} = 2.1$[50]	1[51]
Nonlinear refractive index (Kerr coefficient) n_2 (m^2 W^{-1})	5×10^{-18}[52]	2.4×10^{-15}[48]	1.15×10^{-19}[53]	1.59×10^{-17}[54]	1.59×10^{-17}[54]	...	1.8×10^{-19}[55]	1.8×10^{-19}[55]	2.3×10^{-19}[55]
Electro-optical coefficient* pm/V	...[56]	...[56]	...[56]	$r_{41} = 1.5$[45]	$r_{41} = 1.5$[45]	...	$r_{33} = 33$[17]	$r_{33} = 33$[17]	$r_{13} = 1.0$[17]
Thermo-optic coefficient (K^{-1})	1.8×10^{-4}[57]	2.4×10^{-5}[55]	0.8×10^{-5}[55]	2.67×10^{-4}[58]	2.67×10^{-4}[58]	1.94×10^{-4}[58]	3.34×10^{-5}[57]	3.34×10^{-5}[57]	2.32×10^{-5}[17]
Piezoelectric coefficient (pc/N)	...[56]	...[56]	...[56]	$d_{14} = 2.6$[50]	$d_{14} = 2.6$[50]	...	$d_{15} = 74$[56]	$d_{15} = 74$[56]	$d_{33} = 5$[50]
Mode size (μm^2)	10–0.1	<1[59]	30–80[10]	1–1.5	0.5[59]	1–1.5	2[59]	2[59]	1[59]
Waveguide propagation loss at 1.55 μm (dB/cm)	0.1–0.5[60]	4[48]	<0.1[10]	1.6[53]	4[47]	<0.5[43]	0.086[47]	0.4[61]	0.6[17]

© Author(s) 2021

but have recently been transferred as thin-films on SiO_2 (buried oxide, BOX), enabling the fabrication of optical waveguides with a much greater refractive index contrast and, therefore, smaller mode field diameters. For comparison, we included both the traditional waveguide structure and the thin film waveguide structure with buried oxide.

From Table I, one can see that the waveguide materials have different strengths and weaknesses. For example, silicon is attractive for its very high refractive index and mature fabrication processes, but the small bandgap means that it can suffer from two photon absorption at moderate powers, which limits the power handling of the platform. Si_3N_4, on the other hand, offers ultra-low optical waveguide losses, which enable efficient optical frequency comb generation, but active components such as light sources, high-speed modulators, detectors, and amplifiers are not possible in Si_3N_4. Similar examples can be found for each of the materials. The conclusion is that no single material can address all the needs of complex PICs that require the integration of many different optical components with different functionalities, such as passive, active, and nonlinear on a single chip. Hence, there is a strong motivation to integrate different materials in PICs to increase the functionalities and use each material for what it is best for. The integration of different materials can be achieved by hybrid and heterogeneous integration, which will be discussed in more detail in Sec. III.

III. HYBRID AND HETEROGENEOUS INTEGRATION

The terms "hybrid integration" and "heterogeneous integration" are not always clearly distinguished in the literature, and sometimes, they are even used interchangeably. In this section, we aim to define these two distinct technologies and provide a brief introduction of the hybrid and heterogeneous integration processes. We also outline the differences between the two concepts and their advantages and disadvantages.

A. Hybrid integration

Hybrid integration is an integration process that connects two or more PIC or photonic device chips usually from different material technologies into one single package (see Fig. 2). This process is, in general, performed at the packaging stage after the fabrication of the PIC and photonic device chips. For example, hybrid integration has been used to integrate fully processed III–V devices, such as laser chips,[62–64] gain chips,[65,66] or even photodiodes,[67] onto silicon[68] and silicon nitride[69] PICs. The processed chips can be mounted either directly on the top of the PIC[62–67] or next to it.[70] The advantages of this integration technique are that one can test and characterize the device that needs to be integrated before the integration process. This enables to pick the best performing devices and discard non-functional components, which increases the yield and allows for tightening the performance control.[68] Moreover, due to the high flexibility of the integration process, it offers a path toward highly accessible automated production.[70] Hybrid integration is also very attractive for small scale production and bespoke circuits as the photonic elements that need to be integrated in the photonic circuit can be selected on a case by case basis. The disadvantage of hybrid integration is that the assembly for the hybrid integration method is usually larger, when compared to the heterogeneous

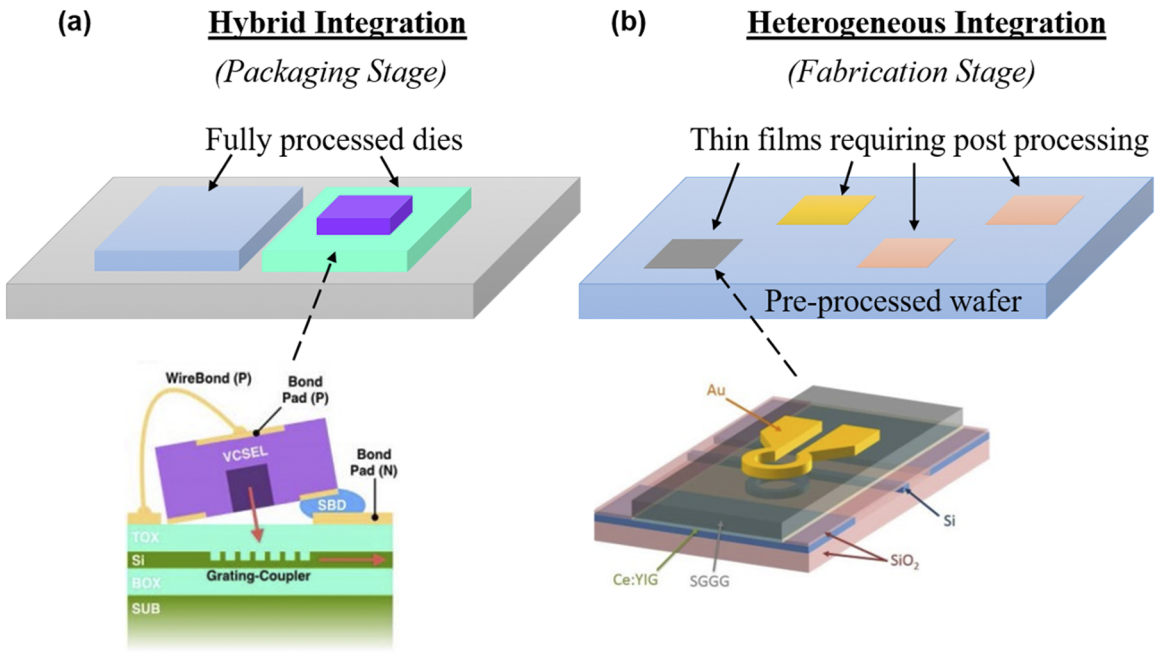

FIG. 2. Schematic illustration of (a) hybrid and (b) heterogeneous integration, with examples shown as insets. (a) Schematic and SEM image of a VCSEL on a SOI PIC, reprinted with permission from Lu *et al.*, Opt. Express **24**, 16258 (2016). Copyright 2016 The Optical Society. (b) Schematic of a heterogeneously integrated optical isolator, reprinted with permission from Huang *et al.*, Optica **4**, 23 (2017). Copyright 2017 The Optical Society.

© Author(s) 2021

integration method. Furthermore, the photonic device alignment and integration process is a serial process (one device or one bar of devices at a time), which can be time consuming and can have limited throughput. This makes this process less attractive for PIC chips with extremely large quantities (such as might be required for low-cost mass market consumer electronics).

B. Heterogeneous integration

Heterogeneous integration is an integration process that combines two or more material technologies into a single PIC chip (see Fig. 2). This process is generally performed at the early- to mid-stages of fabrication of the PIC chip, for example, unpatterned III–V thin-films integrated onto pre-processed silicon photonic wafers. Heterogeneous integration[38] has been a field of intense research in recent years, particularly for the heterogeneous integration of III–V material into silicon[71–76] and silicon nitride[77] PICs. The key benefit of heterogeneous integration is that it can provide functionalities similar to monolithic integration, resulting in high alignment accuracy and low losses when transitioning between different waveguide material technologies. Other benefits are reliable performance of the integrated photonic elements and the low cost due to economy of scale. Therefore, it is suited for high-volume applications.[78] A minor disadvantage of heterogeneous integration is that it has stringent requirement of ultra-clean and smooth surfaces, which can be challenging in university research facilities. However, in semiconductor foundries, this is not an issue due to the dedicated and automated infrastructure and highly trained personnel. Another minor disadvantage of heterogeneous integration processes such as die-to-wafer bonding is that it does not allow for component-by-component modular testing before integration into more complex PICs. Thus, it is somewhat "all or nothing" with tight requirements on process control to improve the yield. Nevertheless, die bonding has been used for the majority of integrated photonic demonstrations.

IV. MATERIAL INTERFACING METHODS

The integration of different materials for hybrid and heterogeneous integration requires interfaces to transition from one material to another, as the refractive index and, therefore, the light guiding properties are different in each material. Generally, desired properties of these interfaces are that they have low loss, are tolerant to variations in the fabrication process, and should often operate over a certain wavelength range (e.g., the complete C-band). In the following, we will describe material interfacing methods that are commonly used for the hybrid and heterogeneous integration of different waveguide materials. In particular, we will describe grating coupling, mirror coupling, butt coupling, and adiabatic taper coupling.

A. Grating coupling

Grating coupling uses a periodic structure that is often etched into the waveguide material, creating a periodic grating of high and low refractive index regions, and can be used to couple light into or out of the PIC. The periodic refractive index structure creates a second-order Bragg grating, which, under normal conditions, couples the light vertically in and out. However, vertical coupling causes unwanted second-order reflection[79–81] and reduces coupling efficiency, which is why the period of the grating is adjusted in such a way that the coupling angle is tilted slightly off vertical,[80,82] as shown in Fig. 3 for a shallow etched grating coupler in the SOI technology. The Bragg condition for a diffraction grating coupler is

$$n_{wg} - n_c \sin\theta = m\frac{\lambda}{\Lambda},$$

where "n_{wg}" denotes the effective index of the waveguide, "n_c" denotes the cladding refractive index, "λ" denotes the wavelength, "Λ" denotes the period of the grating, and "m" denotes the diffraction order.[83]

One should note that the perturbation from the grating affects the diffraction of light going to the top and the bottom, usually causing coupling losses that are larger than 3 dB as most of the light scattered to the bottom (approximately half) is lost.[83] However, the coupling efficiency can be increased by using specially designed grating couplers, such as slanted grating couplers,[80] chirped grating couplers,[84,85] grating couplers with an extra reflector,[86,87] and dual-layer grating couplers,[88–91] which enables coupling losses below 2 dB.[81,92–95]

The ability to couple light in and out of a PIC surface is usually used to interface optical fibers or fiber arrays with the PIC, enabling wafer-scale testing. It also provides the flexibility of placing the optical interface anywhere on the chip surface.[95] Moreover, it can also be used to interface the PIC waveguide material with materials that enable a different PIC functionality (see Fig. 4). For example, over a decade ago, the integration of InP/InGaAsP photodetectors was demonstrated on a SOI PIC by mounting the detectors (operation wavelength: 1.55 μm) on top of grating couplers and using a thick polymer (BCB) bonding layer.[97] In addition, light sources can be integrated by using grating couplers as demonstrated by Huihui Lu *et al.*, showing the integration of a tilted-VCSEL above a grating coupler.[63]

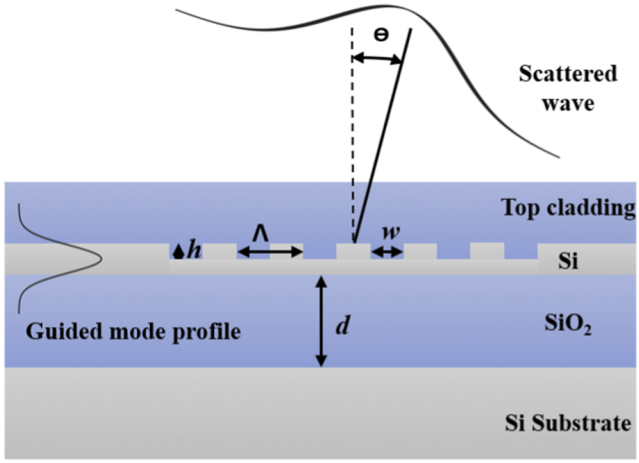

FIG. 3. Illustration of a grating coupler in the SOI technology.[96] "Λ" denotes the period of the grating, "w/Λ" denotes the duty cycle of the grating coupler, "Θ" denotes the scattered angle of the grating coupler, "h" denotes the depth of grating teeth or etch depth, and "d" denotes the thickness of the BOX layer (SiO_2).

© Author(s) 2021

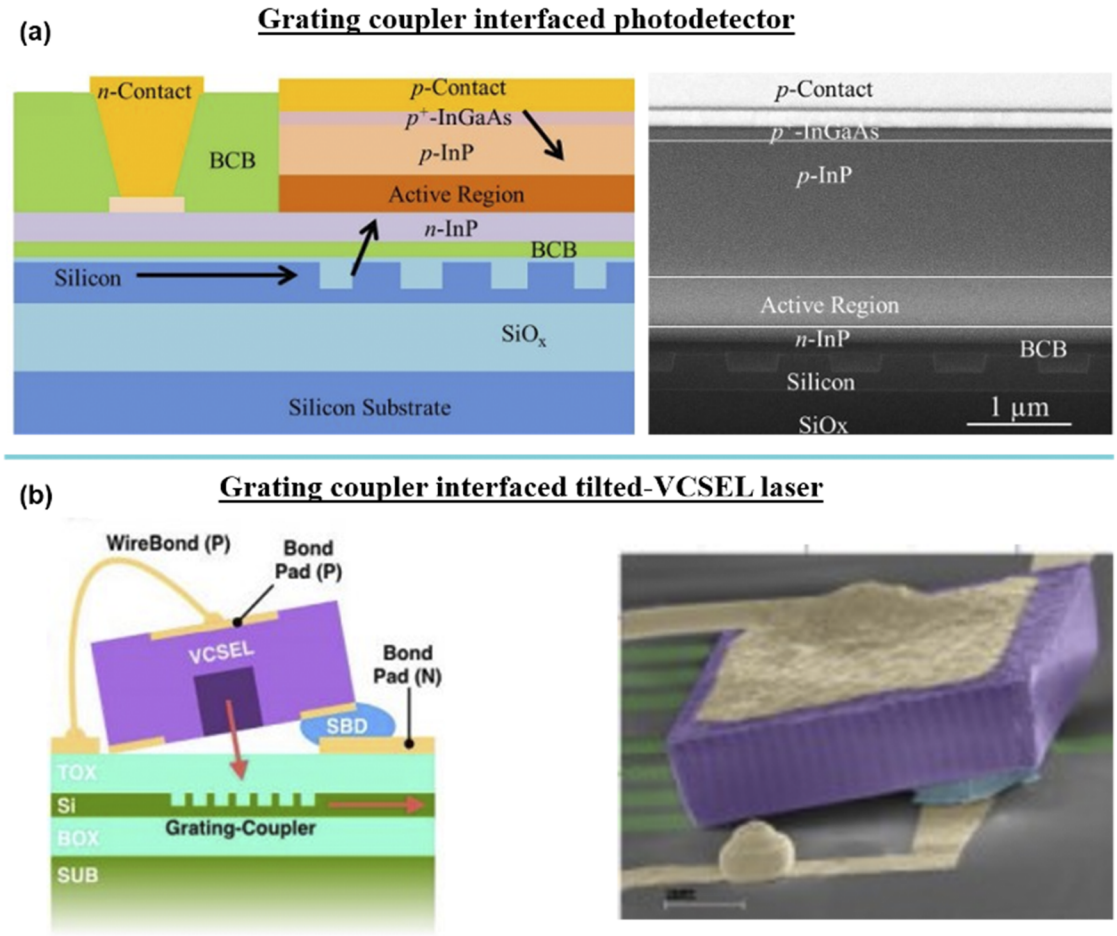

FIG. 4. (a) Schematic and SEM image of the cross section of a photodetector on a SOI PIC, reprinted with permission from Wang *et al.*, Opt. Express **24**, 8480 (2016). Copyright 2016 The Optical Society. (b) Schematic and SEM image of a VCSEL on a SOI PIC, reprinted with permission from Lu *et al.*, Opt. Express **24**, 16258 (2016). Copyright 2016 The Optical Society.

An advantage of this integration method is that the required positioning accuracy of the detector/laser is lower when compared to other interfacing methods[98] as the beam diameter is usually in the order of ~10 μm but can be controlled as required by adjusting the grating coupler design. Some of the limitations of this interfacing method are that it is challenging to achieve coupling efficiencies that are better than ~2 dB (due to the grating coupler), the optical bandwidth of the grating couplers can be too narrow (~58 nm for 3 dB FWHM),[99] and the coupling is polarization-dependent.[100]

B. Mirror coupling

Another way to achieve a vertical coupling interface between two different material technologies is to use mirror coupling. The mirror couplers reflect light in/out of the waveguide by using an angled, highly reflective material interface that is fabricated in the waveguide plane. The angled material interface can be achieved by different means, such as mechanically polishing,[101,102] dicing blades,[101,102] and etching,[103,104] and the high reflectivity can be achieved by using metal coatings[105] or total internal reflection.[65,106] Figure 5 shows two examples of such mirror coupling schemes, which have so far mainly been employed to couple to optical fibers; however—similar to grating couplers—these mirrors can also be used to vertically couple two material technologies with each other, as explained by Noriki[102] *et al.* and Song[65,107] *et al.* They used a chemically assisted ion beam etched mirror interface to redirect the propagating light from a semiconductor optical amplifier waveguide into a SOI PIC with the help of a grating coupler in the silicon layer.[65,107]

Mirror coupling as an interfacing method has some advantages, when compared to grating coupling as a vertical interfacing method. For example, mirror coupling does not suffer from the limited wavelength bandwidth of grating couplers and can, in principle, achieve higher coupling efficiencies as they do not suffer from the diffraction of light into the substrate. However, the mirror interfaces are usually more difficult to fabricate as they require additional

© Author(s) 2021

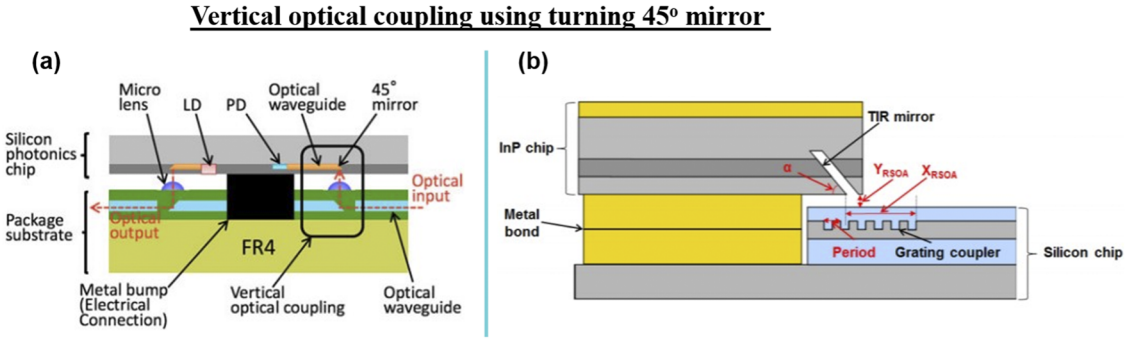

FIG. 5. Two scenarios of mirror coupling: (a) Schematic of the cross-sectional image of vertical optical coupling using the turning mirror of the flip-chip bonded silicon photonic chip. Reprinted with permission from Noriki *et al.*, J. Lightwave Technol. **34**, 3012 (2016). Copyright 2016 IEEE. (b) Side view schematic of vertical coupling using the turning mirror and grating coupler of a 3D integrated hybrid laser, reprinted with permission from Song *et al.*, Opt. Express **24**, 10435 (2016). Copyright 2016 The Optical Society.

fabrication steps, and depending on the fabrication method, they may only be achievable at the chip end facets.

C. Butt coupling

Butt coupling is commonly used to interface fibers with PIC chips, but it is also an attractive method to interface two different PIC material technologies. Butt coupling has its name from the coupling process, which requires the butting of the two devices to be interfaced in a way that enables the coupling of the mode field of the transmitter to the receiver device.[108] The coupling efficiency depends on several factors:[108] (1) the quality of the end facets, (2) the angle at which light is reflected back from the end facet, (3) the spatial misalignment of the modes, and (4) the matching of the modes in the two material technology interfaces. (3) and (4) are usually calculated together by using the overlap integral.[108]

Butt coupling was demonstrated by Urino *et al.*[109] and Mack *et al.*,[110] who co-packaged a III–V laser diode interfacing with a silicon photonic PIC,[110] as shown in Fig. 6. They did hybrid integration of the laser with a Si PIC comprising modulators and PDs

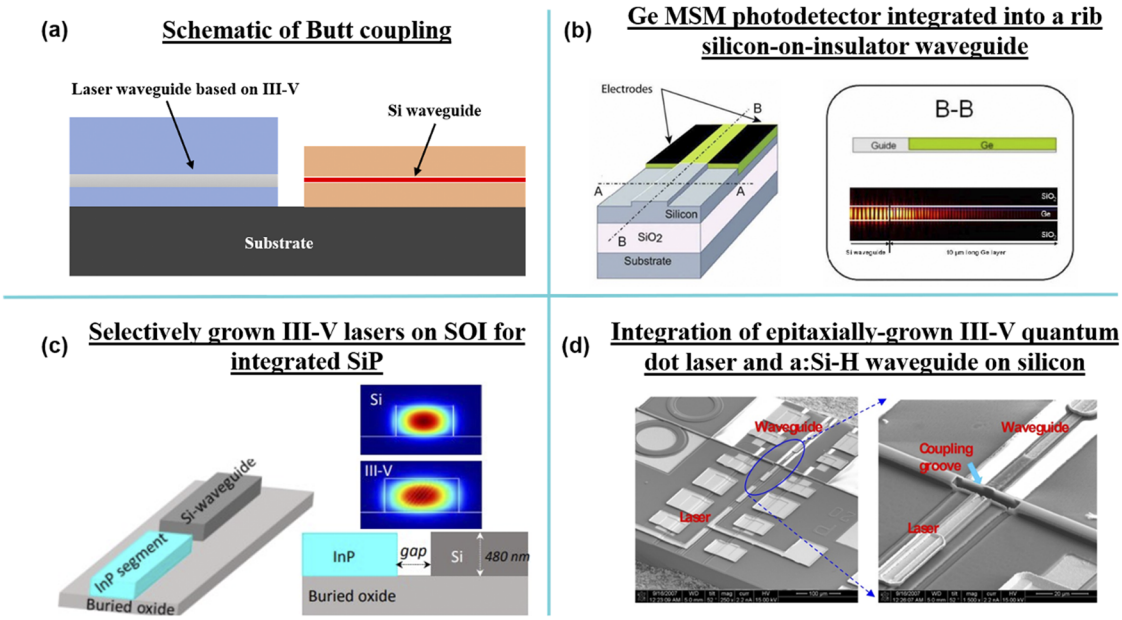

FIG. 6. (a) Schematic of hybrid integration of III–V and silicon photonic PIC through butt coupling.[110] (b) Schematic diagram and electric field amplitude in a longitudinal cross section of the integrated Ge MSM photodetector in SOI Rib waveguides, reprinted with permission from Vivien *et al.*, Opt. Express **15**, 9843 (2007). Copyright 2007 The Optical Society. (c) Heterogeneous integration of III–V laser and Si waveguide through butt coupling by using the "lateral ART" method. Reprinted with permission from Han *et al.*, J. Lightwave Technol. **39**, 940 (2020). Copyright 2020 IEEE. (d) SEM image of an integrated InGaAs/GaAs quantum dot laser and hydrogenated amorphous silicon waveguide on silicon,[120] reprinted with permission from J. Yang and P. Bhattacharya, Opt. Express **16**, 5136 (2008). Copyright 2008 The Optical Society.

© Author(s) 2021

by flip-chip bonding.[109,111] This interfacing method is also compatible with heterogeneous integration as demonstrated by Han *et al.*[112] They presented the butt coupling of InP lasers with an SOI PIC by in-plane InP epitaxy selective growth[113–118] on a SOI wafer.

Butt coupling is attractive as it is not very sensitive to different polarizations and operates over a very broad range of wavelengths. Furthermore, very high coupling efficiencies can be achieved by this coupling method as the mode sizes at the interfaces can be matched very well and scattering and reflection channels can be reduced by appropriate designs.[121] However, it also has some drawbacks, such as it is very sensitive to misalignment as the mode size is usually quite small; therefore, small misplacements can cause a significant reduction in the coupling efficiency. It also possesses stringent requirements for the coupling facet[122] (smooth interface), and the interfaces may cause undesired strong back reflections.

D. Adiabatic tapers

Adiabatic tapers are optical waveguide structures that slowly vary their dimensions (most commonly, the waveguide width) to adiabatically transition the guided waveguide mode from one material technology to the other. Changing the width of the waveguide influences the effective refractive index of the waveguide mode, which is used in adiabatic taper transitions to achieve a smooth transition of light between the two materials.

Such adiabatic tapers have successfully been used to transition between many different waveguide material technologies (see Fig. 7). Examples include adiabatic tapers between Si_3N_4 and $LiNbO_3$ waveguides with transition losses as low as 0.9 dB,[123] between Si_3N_4 and GaAs with transition losses below 1 dB,[27] and between Si and Si_3N_4 with transition losses as low as 0.5 dB.[124] Such transitions can also be used to interface with lasers and detectors. For example, Lamponi *et al.* explored and used inverted adiabatic tapers for heterogeneously integrated InP/silicon-on-insulator (SOI) laser sources (evanescently coupled hybrid lasers), achieving a 90% coupling efficiency for a taper length of 100 μm.[125] Similarly, Wang *et al.*[98] used adiabatic tapers for a heterogeneously integrated InP/silicon photodetector and achieved 1.6 A/W responsivity at 2.35 μm.

The advantages of adiabatic tapers are that they offer a way to achieve extremely low loss, broadband, and fabrication tolerant transitions between different waveguide technologies. For example, the alignment tolerances of adiabatic couplers can be in the order

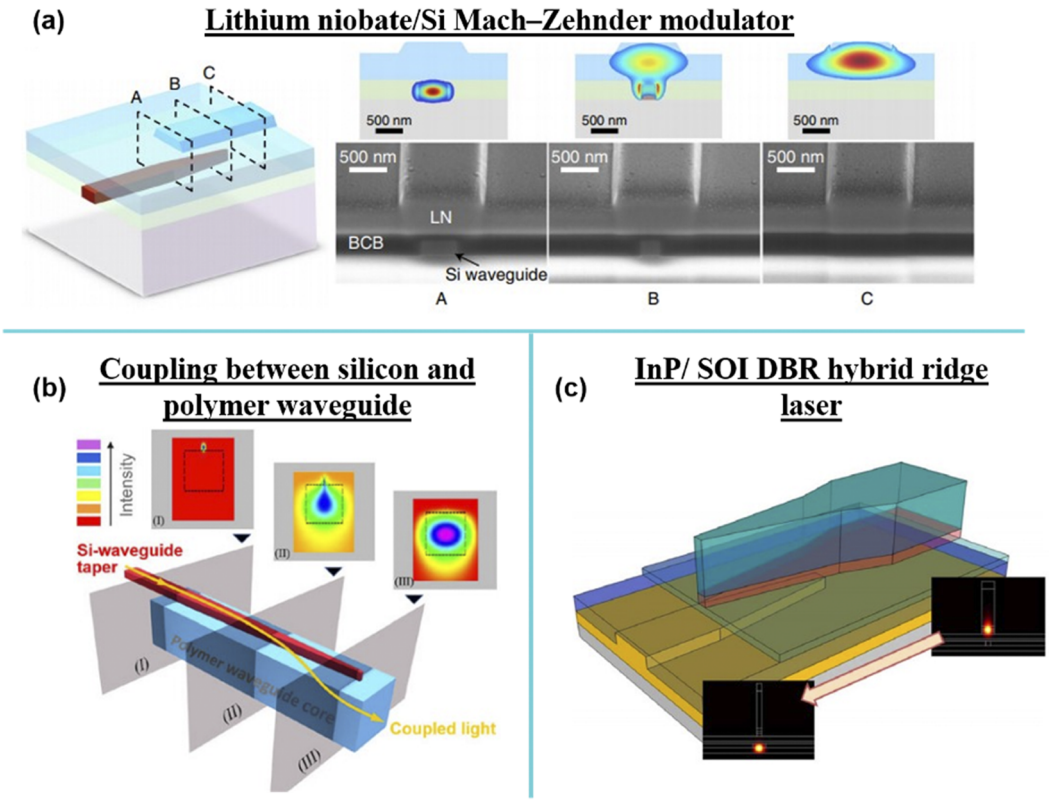

FIG. 7. (a) Schematic and SEM image of the cross section of lithium niobate on a silicon waveguide,[126] reprinted with permission from He *et al.*, Nat. Photonics **13**, 359 (2019). Copyright 2019 Nature Publishing Group. (b) Optical super-mode evolution in the adiabatic coupling system from a Si material waveguide to polymer material waveguide.[127] Reprinted with permission from Dangel *et al.*, IEEE J. Sel. Top. Quantum Electron. **24**, 1 (2018). Copyright 2018 IEEE. (c) Three-dimensional view of the adiabatic taper coupler structure of the hybrid InP/SOI laser with the view of mode profiles in two cross sections. Reprinted with permission from Lamponi *et al.*, IEEE Photonics Technol. Lett. **24**, 76 (2011). Copyright 2011 IEEE.

© Author(s) 2021

of 1 μm,[128] which makes this interfacing method very robust. A systematic study investigated grating coupling, butt coupling, and adiabatic coupling when transitioning between GeSbS and Si single-mode waveguides and found that out of the three interfacing methods, adiabatic coupling offers the lowest coupling losses (0.7 dB) and negligible back-reflections.[129]

A downside of adiabatic tapers can be that they require a larger footprint (100s of micrometers) when compared to grating coupling and butt coupling. The larger footprint is required as the adiabatic change in waveguide width means that the taper needs to have a certain length in order to change the width sufficiently slowly to transition the waveguide modes efficiently. Another issue of taper couplers can be that the tip width of the taper is limited due to fabrication limitations, which may cause undesirable reflections and that it can be difficult to transition between waveguide materials that have a large difference in their respective refractive indices.

V. INTEGRATION METHODS

Having considered how optical components can be interfaced between different material platforms, we must now consider how these different material platforms can be co-integrated and how the devices can be aligned. In this section, we provide an overview of different integrations methods that are commonly used for hybrid and heterogeneous integration for PICs. In particular, we describe flip-chip, die and wafer bonding, transfer printing, and the direct growth and deposition integration methods (which is rather a monolithic integration approach). Several of these integration methods can also be combined to achieve PICs that require the integration of several material technologies.

A. Flip-chip integration

The flip-chip integration technique (also known as controlled collapse chip connection) is a method to integrate and interconnect manufactured chip dies to a carrier wafer or package substrate using bumps of electrically conducting material for the adhesion and electrical connection and was first developed by IBM 60 years ago.[130,131] In the integration process, the chip surface with the electrodes is flipped or put face down on the carrier substrate.[132] This integration method was developed for the integration of electronic circuits and matured over the course of the electronic circuit revolution. However, in recent years, this integration method has also attracted attention for the integration of optical components in photonic integrated circuits.[130,131] In the following, we will provide a brief overview of this integration method and how it has been used for hybrid integration in PICs.

The flip-chip technique requires metal electrode pads on the surfaces of the chip die and the wafer/larger chip that will be bonded together. The pattern of the pads on the die and wafer surface matches each other's or is mirrored when viewed from the top [see Fig. 8(a)]. These electrodes are then interfaced to each other using "bumps" of solder or other metals, which are liquefied and wet between the electrodes on the two surfaces [see Fig. 8(b)].

The fabrication process for creating the mirrored electrode pads (also referred to as "under-bump metallization") often uses metal deposition methods, such as sputtering, plating, or evaporation. The under-bump metallization is important as it provides a strong adhesion interface between the die bond pad and the bump metal, provides a low electrical resistance contact between the chip and the bump metal, and prevents the diffusion of the bump material into the chip, which can be undesired.[131,134] After the under-bump metallization is completed, the bump is deposited on the bonding pads of the chip. The bump material is commonly a low melting point solder such as lead/tin, tin/copper/silver, or gold/tin, and it can be deposited by plating, stencil printing, laser dispense, or mold transfer.[131] In cases where very high frequency operation is required, the bumps can also be pure gold deposited using a ball-bonder from gold wire.[135]

The last step of the flip-chip integration technique is to bring the top chip in contact with the substrate and melt the solder bumps by using thermocompression, thermosonic, or adhesive (isotropic, anisotropic, and nonconductive) flip-chip joining methods.[130] The surface tension and the gravitational force of the molten solder can create a force on the chip that centers the bonding pads, which is also called a self-alignment phenomenon [as illustrated in Fig. 8(b)].[131,133]

Common advantages of the flip-chip integration method are that it is a very mature process (has been developed for decades), it allows for good thermal management of the integrated dies,[132,136] the footprint of the contacts is small,[131] it increases the integration density,[137] it is a low-cost process, dies can be tested/characterized before assembly, and it increases the yield.[138] Furthermore, the

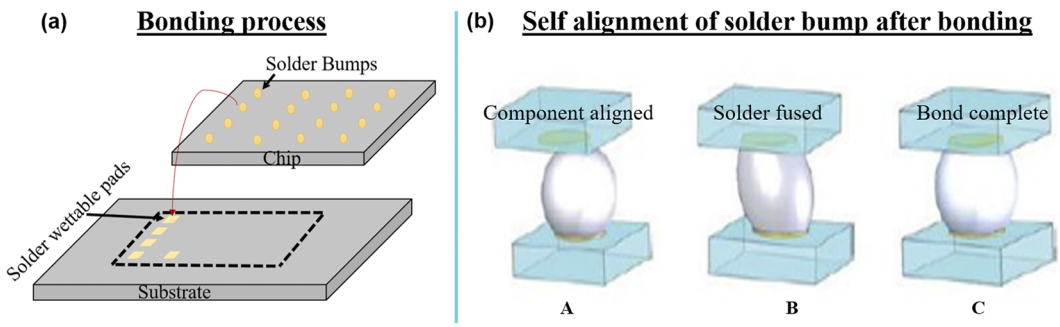

FIG. 8. (a) Bonding process of the flip-chip method[131] and (b) self-alignment phenomenon of solder bumps, reprinted with permission from Bernabé *et al.*, Opt. Express **20**, 7886 (2012). Copyright 2012 The Optical Society.

© Author(s) 2021

electrical contacts have a low parasitic inductance and short interconnect length, making them suitable for high-frequency signal transmission, i.e., tens of GHz.[139]

The mature flip-chip integration process also makes this method attractive for the integration of optical components in PICs. An example is the cost-effective hybrid integration of a laser-source on a silicon photonic integrated circuit, as demonstrated by Lu *et al.*[63] in 2016. They bonded a VCSEL diode on top of a grating coupler and optimized the tilt angle to achieve low coupling losses [see Figs. 4(a) and 4(b)], resulting in an insertion loss of 11.8 dB.[63] Flip-chip integration can also be used for achieving waveguide-to-waveguide interfaces via butt coupling. The precision alignment for this integration is achieved by using solder aligned photonic flip-chip assembly [see Fig. 9(a)], as demonstrated by Barwicz *et al.*,[140] including vertical and lateral mechanical stops, which resulted in a minimum transmission loss of 1.1 dB over a 100 nm spectrum. Flip-chip integration is best suited to interfacing relatively large chips together. In cases where much smaller chips or more intimate contact is required, other techniques should be considered.

B. Transfer printing

Micro-Transfer Printing (μTP) is a versatile micro-assembly technology, which provides deterministically fast and precise assembly of microscale components from their native substrates onto non-native substrates with the help of an elastomer stamp.[142–144] This integration method was invented in 2003–2006 by Rogers *et al.*[145,146] and commercialized in 2006 by Semprius[142] and X-Celeprint. This assembly method has been used to transfer a range of materials and devices, such as inorganic semiconducting materials, organic materials, functional polymers, metals, piezoelectric materials, photodetectors, sensors, filters for CMOS cameras, and MEMS.[142–144,147] In the following, we will focus on the use of this assembly method for integrating photonic components on PICs. An extensive overview of this integration method can be found in Ref. 148.

The basic principle of the micro-transfer printing procedure is shown in Figs. 10(a) and 10(b). The transfer process requires a pickup and printing step and uses a viscoelastic material [polydimethylsiloxane (PDMS)] as a stamp. In the first step, prefabricated functional devices on their native substrate are picked up

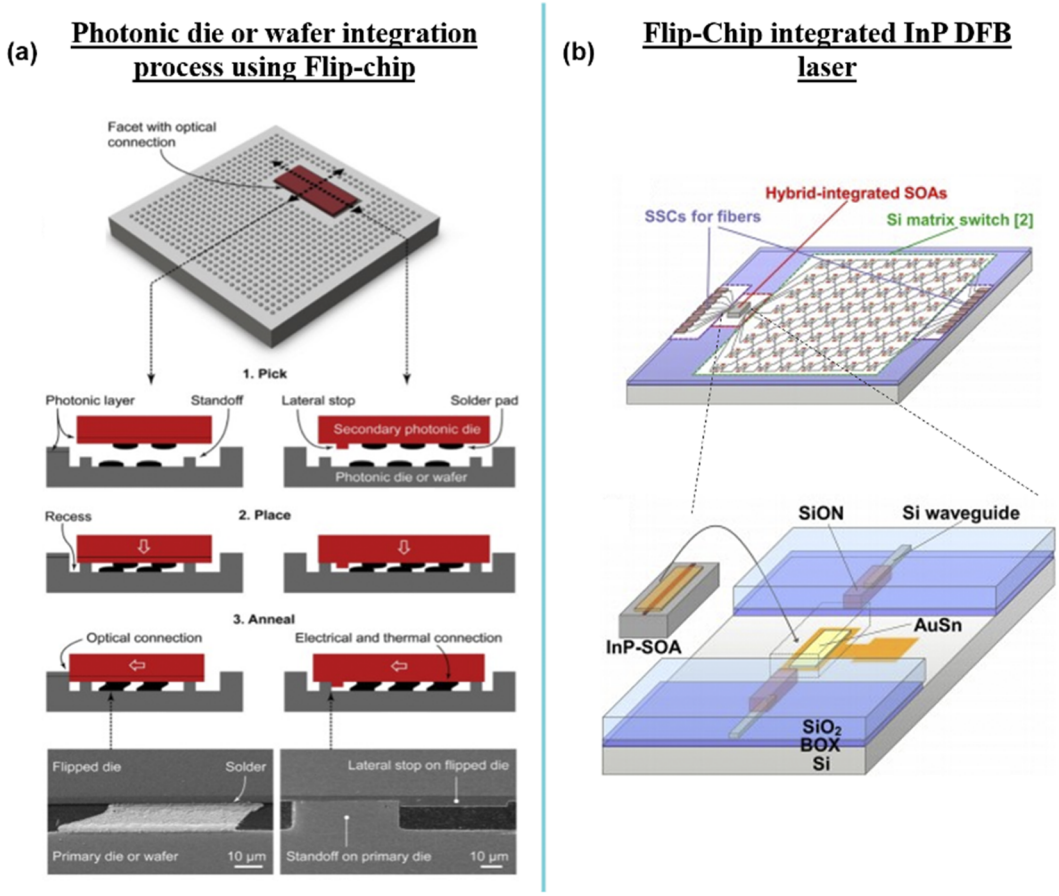

FIG. 9. (a) The schematic of the solder-aligned flip-chip assembly of photonic dies, reprinted with permission from Lichoulas *et al.*, Opt. Fiber Technol. **44**, 24 (2018). Copyright 2018 Elsevier. (b) Schematic of the silicon matrix switch, which uses the hybrid integrated SOA via flip-chip bonding.[141] Reprinted with permission from Matsumoto *et al.*, J. Lightwave Technol. **37**, 307 (2019). Copyright 2019 IEEE.

© Author(s) 2021

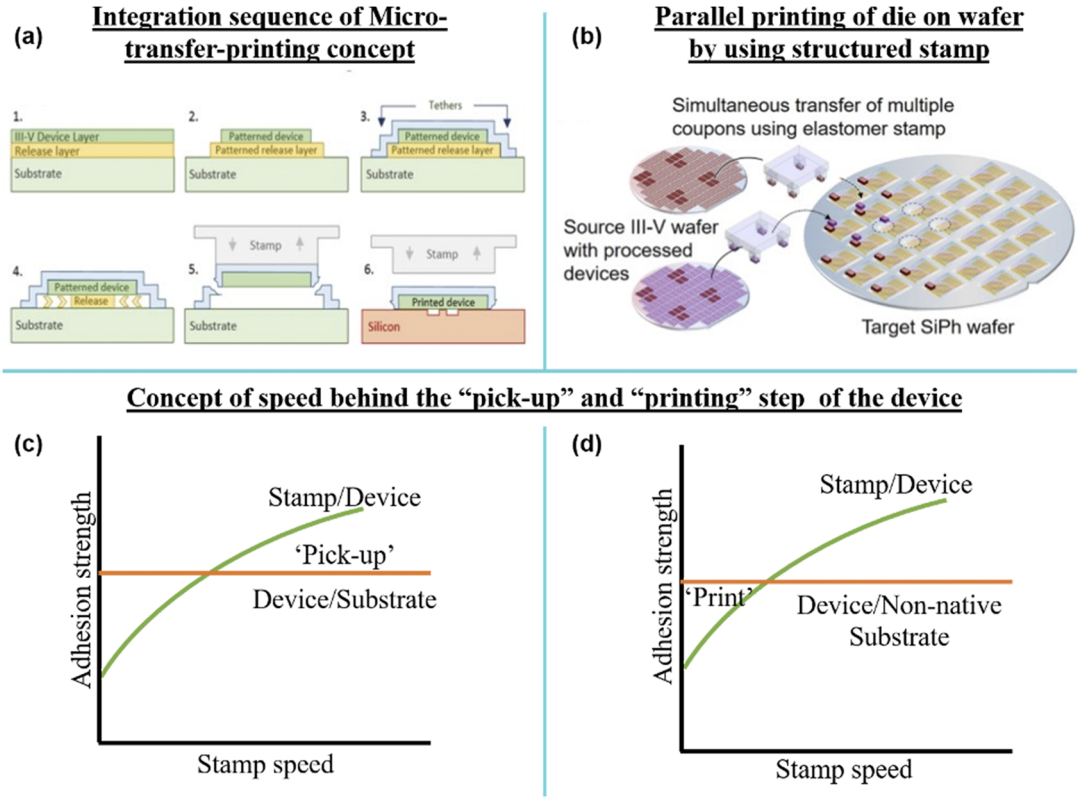

FIG. 10. Concept of μTP. [(a) and (b)] Prefabrication of III–V devices on their native substrate and the μTP integration sequence release, picking, and printing of the devices on the target substrate.[148] The schematic of μTP-based integration of multiple devices on 200 or 300 mm Si photonic wafers in a parallel or serial manner using an elastomer stamp, reprinted with permission from Zhang *et al.*, APL Photonics **4**, 110803 (2019). Copyright 2019 Author(s), licensed under a Creative Commons Attribution 4.0 License. [(c) and (d)] Schematic diagram of critical energy release rates.[142]

by adhering to the stamp upon contact.[142–144] The pickup step requires that the energy release rate of the device–stamp interface is larger than that of the device–substrate interface, which can be achieved by using high speed stamp movements.[142,147] The fast stamp movements result in the adhesion of the device to the stamp, which can then be used to transfer the device to a non-native substrate for integration. In the printing step, the stamp is brought in contact with the non-native substrate and the stamp is moved out of contact slowly,[143,147] completing the printing process. The slow movement speed results in a smaller energy release rate of the device–stamp interface, when compared to the device–substrate interface.[142,147]

Micro-transfer printing has successfully been used to integrate a range of active optical components on passive optical device layers. One of the first demonstrations in 2012 was the membrane reflector (MR) surface-emitting laser on silicon that is based on a multilayer semiconductor nanomembrane,[149] which was quickly followed by the transfer printing of diodes[150] and the integration of single-mode waveguide-coupled III–V-on-silicon broadband light emitters.[73] [To interface the transfer printed optical devices with the waveguides, grating couplers,[153] adiabatic tapers,[154] and butt coupling[153] have been explored, where adiabatic tapers are particularly attractive for lasers and amplifiers due to the low interface loses, grating couplers are attractive for detectors as the PICs can be characterized beforehand with the same grating couplers, and butt coupling because of the good thermal contact with the silicon substrate (Fig. 11).] Since then, the integration method has enabled the integration of high-quality DFB lasers,[151] semiconductor optical amplifiers,[73,152] modulators, and detectors[153] onto SOI.

Micro-transfer printing has matured significantly over the years. It can transfer multiple active and passive components onto non-native substrates with high precision ±1.5 μm (3 sigma), high speed (30–40 s),[155] and high transfer yields that exceed 99%.[147,156] Furthermore, the stamps used for the transfer have a long lifetime of more than 300 000 printing cycles.[155] Similar to the flip-chip technique, micro-transfer printing allows—in some cases—for pretesting of the fabricated devices prior to integration on the target wafer.[155] However, in contrast to flip-chip bonding, micro-transfer printing is best suited to transferring very small elements—even at the scale of individual devices onto a large substrate. Furthermore, the transferred "chiplets" are generally between 0.2 and 3 μm thick, and hence, it is possible to conduct transfer printing midway through fabrication of the PICs, planarize the surface after the chiplet has been transferred, and proceed with additional

© Author(s) 2021

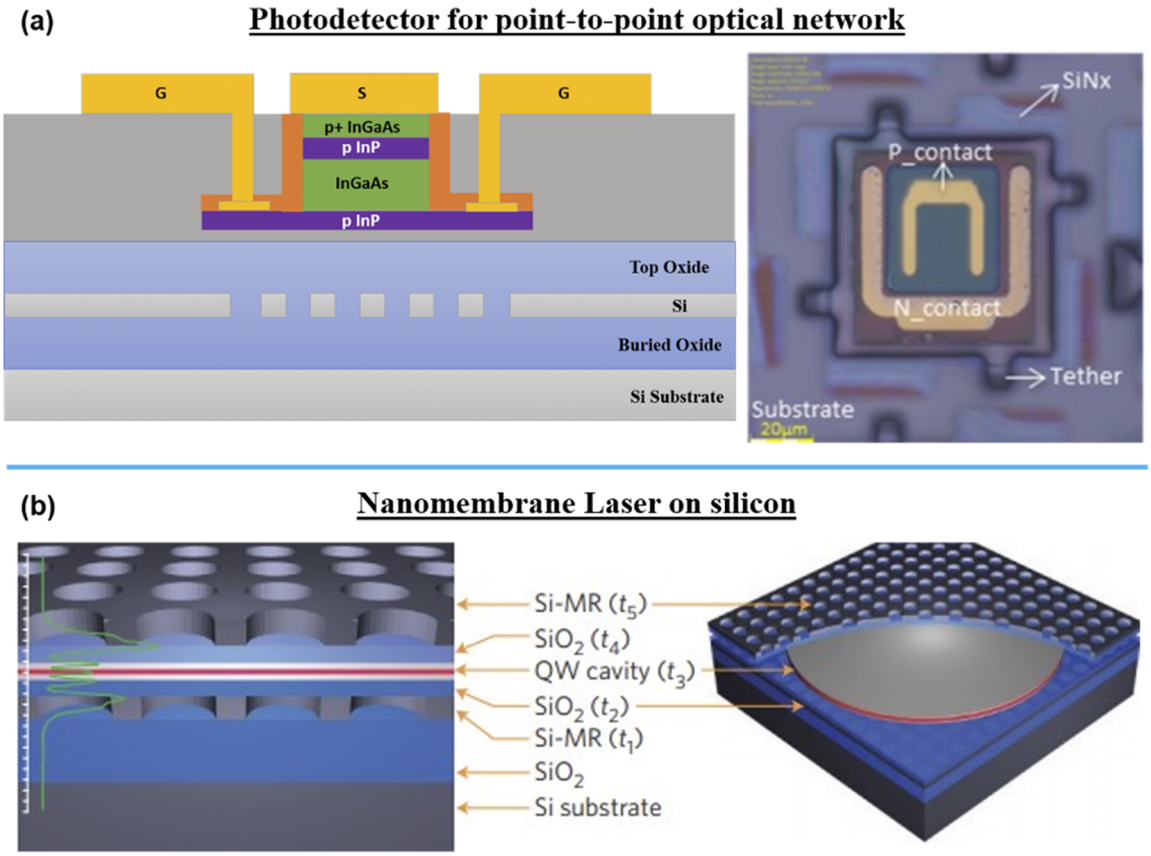

FIG. 11. (a) Cross section and microscopic view of the III–V photodetector,[157] reprinted with permission from Zhang *et al.*, Opt. Express **25**, 14290 (2017). Copyright 2017 The Optical Society. (b) Schematic layout and cut-out view of the silicon membrane reflector (MR) VCSEL, reprinted with permission from Yang *et al.*, Nat. Photonics **6**, 615 (2012). Copyright 2012 Nature Publishing Group.

lithography steps. In this way, micro-transfer printing can offer some of the beneficial features of both hybrid integration and heterogeneous integration simultaneously.

Micro-transfer printing has enabled a number of experimental demonstrations, for example, the work of Zhang *et al.*,[153] who demonstrated a III–V photodetector array for O band (1260–1360 nm), enabling Point-to-Point (P2P) fiber-to-the-home (FTTH) optical networks. Yang *et al.*[149] used the micro-transfer printing to demonstrate a nanomembrane laser on silicon, where the quantum-well heterostructure of III–V InGaAsP is sandwiched between two silicon membranes, where the III–V membrane and top silicon membrane are integrated by micro-transfer printing.[149]

C. Die and wafer bonding

Die and wafer bonding is a process of joining a die/wafer to a wafer to form a permanently bonded stack. This process is particularly attractive when large area films are required with excellent material properties (e.g., crystalline materials that are difficult to grow on non-native materials). The bonding process has been developed for the electronic integrated circuits and MEMS industries, and bonding tools (commonly called wafer bonders) are commercially available from most micro- /nano-fabrication equipment suppliers.[158] Wafer bonders consist of wafer-handling stack and a pair of chucks for applying heat, voltage, and force to the wafer stack. The whole setup is usually placed in a chamber to control the atmosphere during the bonding process (typically, vacuum to avoid trapping of air), as illustrated in Fig. 12(a).[158] Different wafer bonding methods have been developed over the years, and they can be categorized depending on the bonding mechanism, namely, without intermediate layer bonding and intermediate layer bonding, as illustrated in Fig. 13(b).[159,160]

Bonding without an intermediate layer describes the method to join two surfaces together without using an adhesion layer in between, and the most commonly used bonding method for PICs[162] in this category is the direct bonding [see Fig. 13(a)]. Direct bonding has been used since 1960 for many substrates and structures.[163–165] A breakthrough for the direct bonding technique was the demonstration by Lehmann *et al.* in 1989 and bonding III–V semiconductor layers, such as GaAs and InP, on the bare silicon bubble free.[166] The bonding strength of this method can be very high, enabling the further processing of the wafers and even mechanically grinding and

© Author(s) 2021

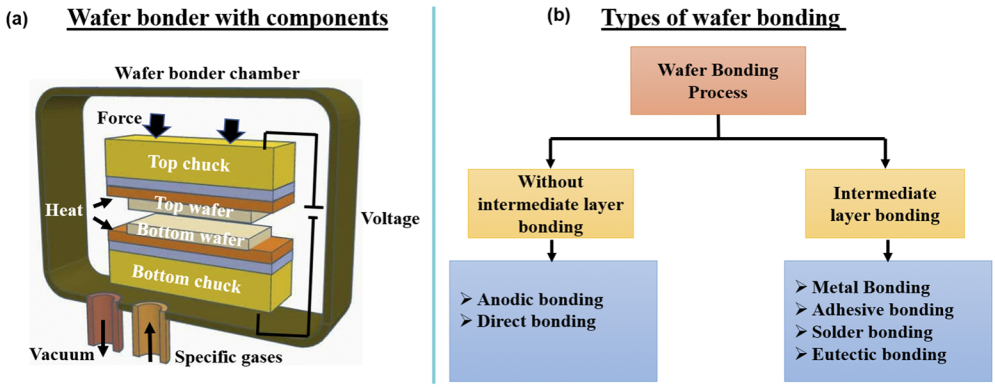

FIG. 12. (a) Schematic of the key components of a wafer bonder.[158] (b) Types of wafer bonding processes currently used in semiconductor technology.[161]

polishing the bonded dies/wafer. Furthermore, direct bonding provides an excellent thermal conductivity between the bonded film and the target wafer,[161] which is very attractive for the thermal management of the integrated devices. The yield of integrated devices can be very high when using the direct bonding integration method; however, it has stringent requirements on the surfaces, which need to be extremely clean and ultra-flat.[159,167,168] If the surfaces are not carefully prepared, the bond may suffer from issues such as outgassing, trapped particles, and a weak bond.[168,169] When using direct bonding at high-temperature (e.g., annealing at 600 °C[170]), one also needs to consider the thermal expansion coefficients of the materials that will be interfaced as the thermal mismatch can create stress,

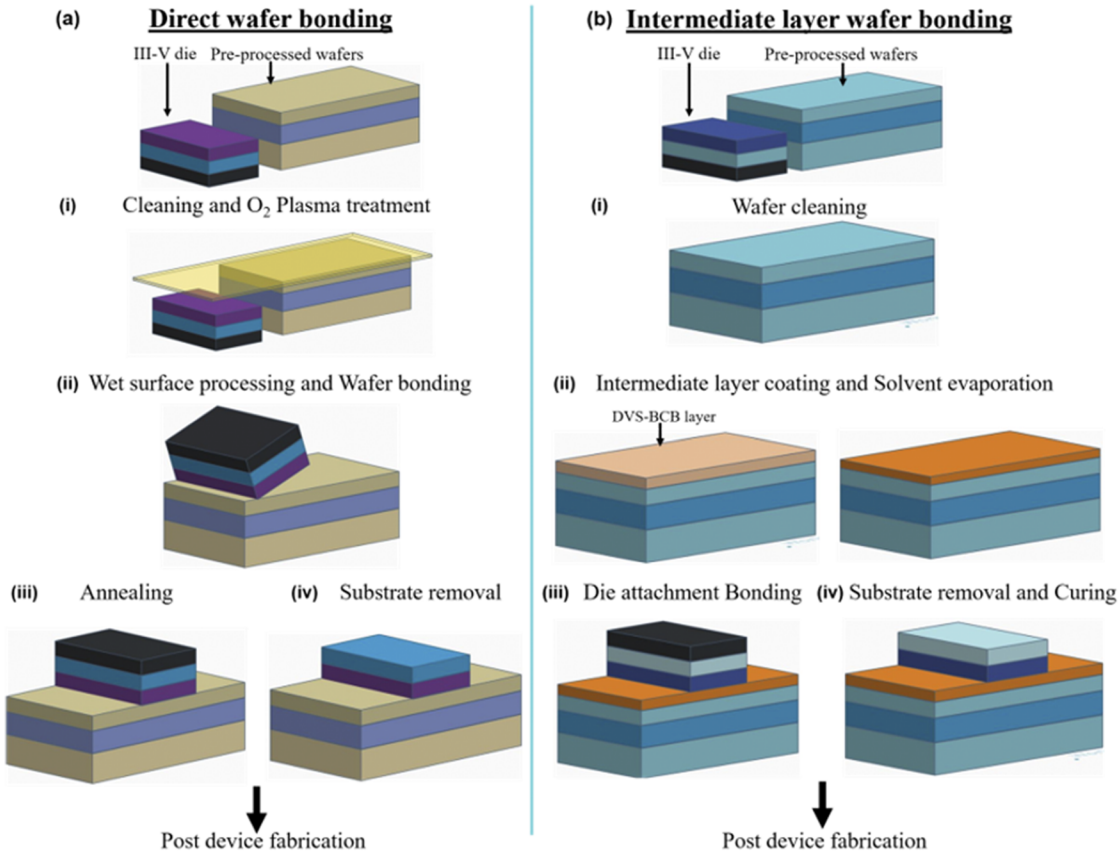

FIG. 13. Schematic process flow for (a) direct (O_2 plasma-assisted/SiO_2 covalent) wafer bonding[173] and (b) intermediate layer wafer bonding (DVS-BCB).[173]

© Author(s) 2021

which may be detrimental to the bond and, therefore, for the integrated devices.[161] However, the O_2 plasma assisted (SiO_2 covalent bonding) method can achieve a high bonding strength even for a low-temperature annealing process (<400 °C).[171,172]

The most commonly used intermediate layer bonding method for PICs is adhesive bonding by using polymers such as BCB and SU-8 as an adhesion material.[160] For the bonding process, the polymer layer is spin coated on the target wafer followed by a soft bake to remove any solvents (as they can create bubbles) and then brought into contact with the dies/wafers that will be integrated on the target wafer and finally perform a thermal annealing step [see Fig. 13(b)].[173] When compared to the direct bonding method, the intermediate layer bonding imposes far fewer restrictions on the roughness and cleanliness of the surface;[158,160] in fact, the spin-coating of the polymer can be used to fill gaps and provide a flat surface. Furthermore, intermediate layer bonding offers a high bonding strength at moderate temperatures (~250 °C), low bonding induced strain, and good uniformity and scalability.[173] However, one potential disadvantage of the intermediate layer bonding when using polymers is that the thermal conductivity of the layer is quite low, which can make the thermal management of devices difficult. However, typically, in a PIC context, the thermal resistance of the integrated devices is determined by the buried oxide layer and not the adhesive bonding layer.

Both bonding methods (direct bonding and intermediate layer bonding) have enabled the integration of several optical components on PICs[174] (see Fig. 14). A large effort of this work was the integration of III–V materials on silicon waveguides, enabling the integration of lasers,[175] modulators,[176] amplifiers,[177] and detectors.[178] However, wafer bonding is also a very attractive method for integrating high quality material films on waveguides, such as magneto-optic materials[179] and nonlinear optical materials,[25] enabling PICs with a wide variety of useful functions, properties, and high performance.[180] For example, wafer bonding can be used to produce vertically integrated circuits using a crystalline Si layer on the top of an ultra-low loss silicon nitride (SiN) waveguide layer;[181] the integration of crystalline magneto-optical materials [yttrium iron garnet (Ce:YIG)] for nonreciprocal devices, such as optical isolators and circulators;[180,182] and nonlinear and electro-optical materials, such as $LiNbO_3$.[123] Furthermore, in 2019, Hu *et al.* demonstrated a novel photonic integration method of integrating III/V (MQW lasers) materials into the SOI substrate by regrowth on a bonding template. This unique process combines the advantages of both monolithic growth and wafer bonding approaches.[183] A similar approach is followed by NTT, resulting in high-performance III–V membrane devices integrated on silicon waveguide circuits.[184]

D. Layer deposition

Layer deposition is a monolithic integration process, where thin films of materials are deposited on the target wafer. In general, one can differentiate between two categories of deposition processes:

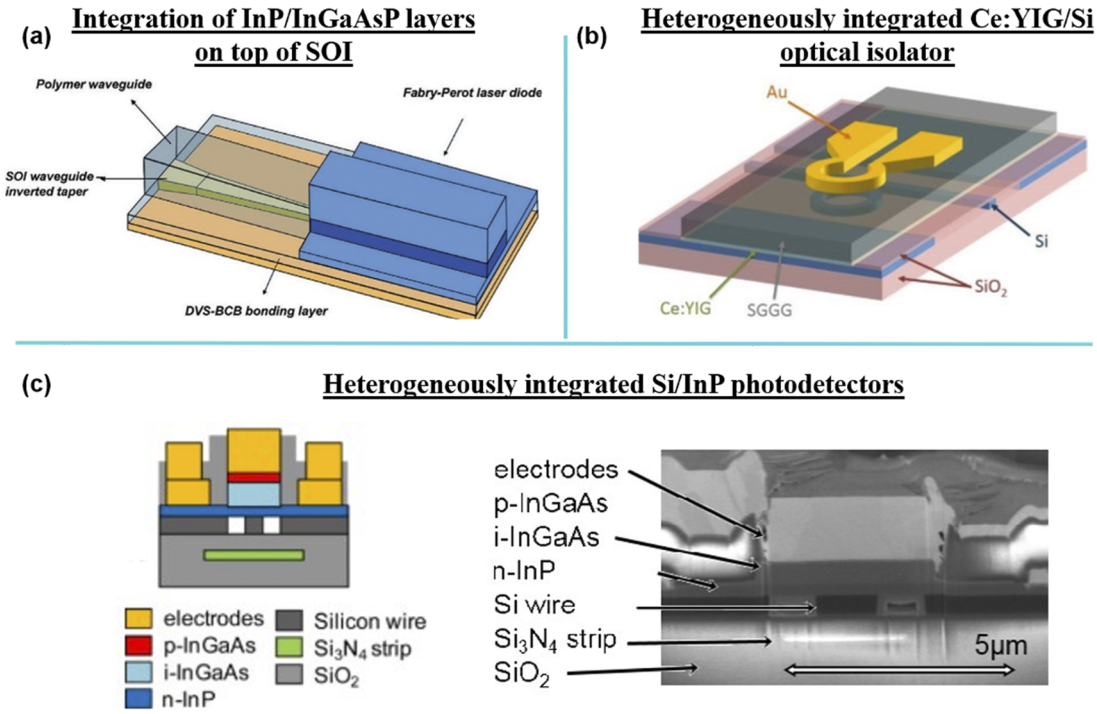

FIG. 14. (a) Schematic layout of the Fabry–Perot laser diode and an underlying SOI waveguide,[175] reprinted with permission from Roelkens *et al.*, Opt. Express **14**, 8154 (2006). Copyright 2006 The Optical Society. (b) Schematic of a heterogeneously integrated optical isolator, reprinted with permission from Huang *et al.*, Optica **4**, 23 (2017). Copyright 2017 The Optical Society. (c) Schematic layout and SEM image of the cross section of a heterogeneously integrated photodiode. Reprinted with permission from Piels *et al.*, J. Lightwave Technol. **32**, 817 (2014). Copyright 2014 IEEE.

© Author(s) 2021

(i) physical vapor deposition (PVD) and (ii) chemical vapor deposition (CVD). A list of different deposition methods for the two categories is given in Fig. 15. Physical vapor deposition is a vacuum deposition process in which the co-deposited material undergoes a transition from the solid state at a source to a gaseous state that is directed to the target, and at the target surface, it condenses to form a solid state, resulting in a thin film. Chemical vapor deposition describes processes that expose target wafers to volatile precursor gases, which react and/or decompose on the target to form a high-quality thin film of the desired material. In general, each of the different deposition methods has its advantages and disadvantages and is suitable for the deposition of a range of materials. In practice, the material that is desired for integration defines the deposition method to enable the deposition of high-quality thin films on target wafers. One of the main restrictions when such deposition methods are used to integrate materials on PICs is that the processing temperature in most cases should not be too high. Depending on the PIC material technology, it is required that the processing temperature stays below the dopant activation temperature for Si modulators (1030 °C) or the thermal budget used for dislocation control of Ge-on-Si photodiodes (825 °C). When applied in the back-end, it is important that the processing temperatures stay below ~450 °C. Another important property of the deposition process is the conformality of the deposited layer. The conformality is, generally speaking, lower in PVD processes, when compared to CVD processes, as the directionality of to-deposited material is very high (particularly, in the case of evaporation). A detailed description of the different deposition methods would be too long for this tutorial; hence, we recommend Ref. 185 for further information and focus in the following on examples of materials that can be deposited using some of the deposition methods that are attractive to integrate additional functionalities into PICs.

Highly efficient nonlinear acousto-optic waveguides can be integrated on silicon waveguides by depositing chalcogenide glasses using e-beam evaporation.[186] Chalcogenide glasses, such as As_2S_3, GeSbTe, and AgInSbTe, are attractive for acousto-optical applications (e.g., stimulated Brillouin scattering) as they can confine acoustic modes even when a SiO_2 buffer layer is used.[187] Furthermore, chalcogenide glasses have a broadband infrared transparency (0.8–20 μm)[188] and high third order nonlinearity,[189] which make chalcogenide waveguides attractive for mid-IR applications,[187,190,191] optical frequency comb generation,[192] supercontinuum generation,[193] and wavelength conversion.[194]

Si_3N_4 is an attractive material for integration on PICs as it enables optical waveguides with low optical losses, which are attractive for routing optical signals over longer distances on chip and for high Q-factor nonlinear optical microresonators.[195,196] Different deposition methods have been explored for the deposition of high-quality Si_3N_4 films, where low pressure chemical vapor deposition allows ultra-low loss waveguides[195] if processing temperatures of >700 °C can be tolerated by the PIC; for lower temperatures (inductively coupled), plasma enhanced chemical vapor deposition[197] and sputtering[198] are attractive achieving waveguide losses below 0.5 dB/cm.

E. Direct growth

Direct growth is another monolithic integration process. The difference in the deposition processes outlined above is that direct growth is an epitaxial process in which crystalline layers are grown, which is a very attractive way to integrate semiconductor materials in a scalable manner. Crystalline growth is particularly important for electro-optic active devices, such as lasers, amplifiers and detectors, as defects and dislocations can be detrimental to the device performance and lifetime. A challenge in reducing such defects is to overcome crystal lattice mismatch between different materials. For example, the lattice mismatch between GaAs and Si is around 4.1%.[201] This can cause structural defects during the growth, which can occur in different sizes and ranges from 0D point defects (such as vacancies or interstitials), over 1D line defects (such as misfit dislocations), and 2D planar defects (such as stacking faults, twin defects, misfit dislocations, and grain boundaries) to 3D defects (such as voids and precipitates). Another challenge can be the significant differences in the coefficient of thermal expansion[202] between different

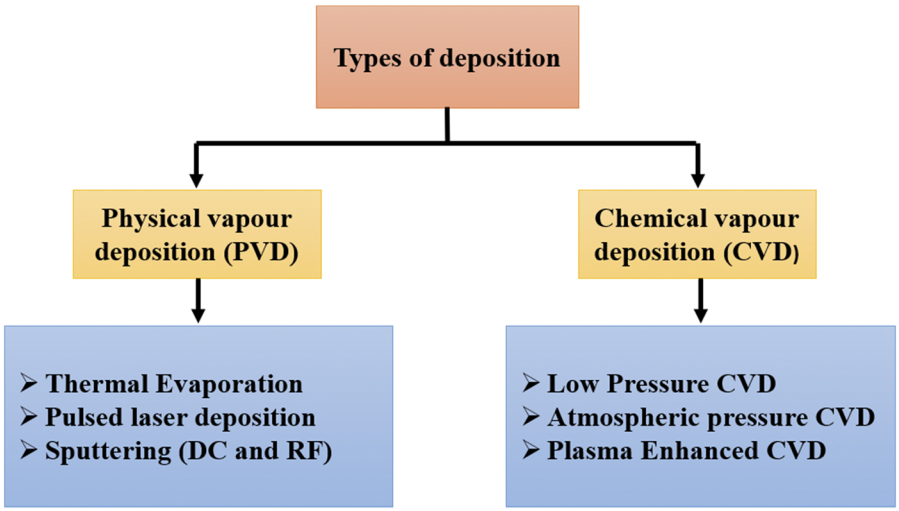

FIG. 15. Overview of deposition methods that are often used for photonic material technologies.

© Author(s) 2021

materials and the fact that a polar semiconductor (III–V) is grown on a non-polar semiconductor (Si). A detailed overview of direct growth and the different defects is given in Refs. 199 and 200. In the following, we provide two examples of materials grown on PICs.

Germanium is a very attractive material for photodetectors on silicon photonic integrated circuits. Germanium photodetectors can be epitaxially and selectively grown by Reduced Pressure Chemical Vapor Deposition (RP-CVD) in a silicon recess.[119,203] This process is also available in current silicon photonic foundry processes. The germanium film is grown at 730 °C on a germanium buffer layer, which reduces the misfit dislocations and keeps the surface of the grown germanium layer smooth.[119] Experimental demonstrations include photodetectors with a responsivity of 1 A/W at a wavelength of 1.55 μm[119,203] and a bandwidth of >67 GHz at 1 V reverse bias.[204]

The growth of III–V materials on silicon is also very attractive as it enables the integration of lasers, amplifiers, modulators, and detectors on material technologies, such as SOI (see Fig. 16). In recent years, there has been a considerable progress in this field, demonstrating the direct epitaxial growth of bufferless 1.5 μm III–V lasers by metal organic chemical vapor deposition (MOCVD) onto one of the standard SOI wafers with a silicon film thickness of 220 nm.[205] When growing pure InP, lasing can be achieved at the room temperature, emitting a wavelength of 900 nm. When embedding InGaAs quantum structures inside InP, the lasing wavelength can be shifted to the desired communication wavelength of around 1500 nm.[205] In addition, GaAs-based ridge lasers operating at an ~1000 nm wavelength have been demonstrated.[184] Photodetectors can also be directly grown on SOI without the need of a buffer layer, enabling the demonstration of a photoresponsivity of 1.06 A/W at 1.55 μm with an operating range from 1.45 to 1.65 μm.[206]

VI. HYBRID AND HETEROGENEOUS INTEGRATION EXAMPLES FOR REAL WORLD APPLICATIONS

In this section, we provide an overview of three examples that highlight and show the power of hybrid and heterogeneous integration approaches to achieve PICs with outstanding properties that would not have been possible in a single PIC material technology.

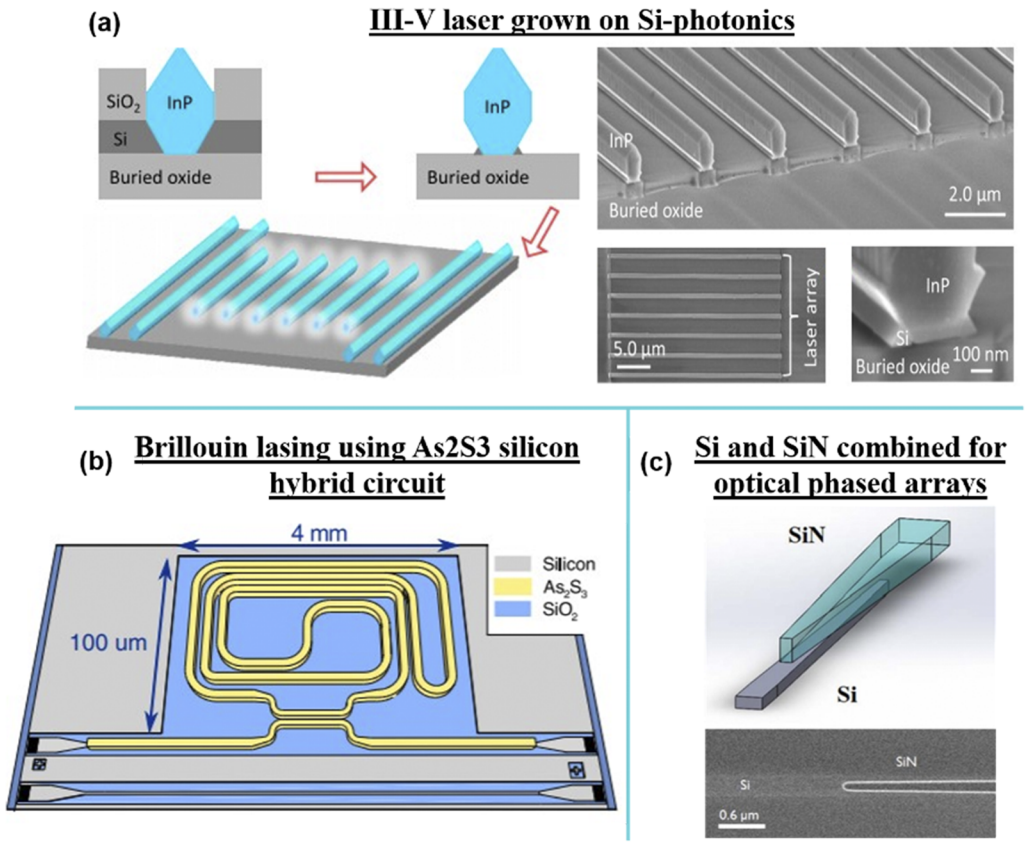

FIG. 16. (a) Schematic of the fabrication process of bufferless III–V lasers on SOI[205] and tilted and top view of the SEM image of the fabricated laser array, reprinted with permission from Han *et al.*, Optica **7**, 148 (2020), Copyright 2020 The Optical Society. (b) Schematic of the integration of an As_2S_3 ring resonator structure on SOI for a Brillouin laser, reprinted with permission from Morrison *et al.*, Optica **4**, 847 (2017). Copyright 2017 The Optical Society. (c) Schematic 3D view and the SEM top view image of a Si–SiN vertical coupler,[207] reprinted with permission from Marinins *et al.*, Jpn. J. Appl. Phys., Part 1 **59**, SGGE02 (2020). Copyright 2020 The Japan Society of Applied Physics.

© Author(s) 2021

A. Transceivers

The transceiver market for data centers is driven by the rapid growth of the Internet. Ideally, transceivers should have a high data capacity, while they should be pluggable (small size) with low power requirements. Furthermore, the price of transceivers should be as low as possible, which requires a scalable technology with production volumes in the multimillion per annum.[208] Arguably, the most attractive material technology for scalability and with potential for low prices is silicon photonic technology. However, the lack of light sources requires hybrid/heterogeneous integration approaches to achieve the required functionalities on silicon.

Transfer-printing-based integrated photodetectors have been used for transceivers, such as the experimental demonstrations of a silicon photonic transceiver array (four channels) by Zhang *et al.*[153] [Fig. 17(a)]. They showed that transfer printing integration technology is suitable to integrate O-band III–V photodiodes, and by choosing a cutoff wavelength of 1.37 μm, it was possible to realize a duplexing of the upstream (1310 nm O-band) and downstream (1550 nm C-band) signals. An example of a recent demonstration using die-to-wafer bonding is the III–V/Si transceivers with integrated DFB lasers, Mach–Zehnder modulators, and wavelength multiplexer for the transmitter, which has been demonstrated and commercialized by Intel. The III–V heterogeneous integration can be done on 300 mm wafers, and the technology is enabling fiber communication up to 10-km reach with data rates of 100 Gb/s [Fig. 17(b)].[209]

B. Integrated optical gyroscopes

Precision positioning and navigation are forecasted to be a rapidly growing market, which is driven by autonomously driving cars and drone applications, among others. For such applications, the efficient use of space, weight, and power is very important. Technological devices that promise to address such navigational needs are integrated optical gyroscopes. The anticipated production value for such integrated optical gyroscopes systems is estimated to be \$20 $\times$ 10^6 per annum by 2025.[210] Similar to transceivers, such high production numbers make it attractive to utilize heterogeneously integrated III–V materials on silicon photonic circuits as a material technology. In the following, advances toward such systems are provided.

For instance, John Bowers' group in 2017 demonstrated a heterogeneously integrated optical engine for interferometric optical gyroscopes (see Fig. 18). In this engine, all the active and passive components (a Fabry–Perot multi-mode laser, photodiodes, phase modulators, and adiabatic 3-dB splitters) except the sensing coil were fabricated on a chip within a 0.5 $\times$ 9 mm^2 area. Using a 180-m-long polarization maintaining fiber (PMF) with 200 mm diameter as a sensing coil, a minimum measurable rotation rate of ~0.53°/s (1908°/h) was achieved.[211,212] To replace the bulky fiber coil, they also investigated the integration of a waveguide coil by utilizing ultra-low loss (<0.78 dB/m) SiN waveguides, which resulted in a theoretical bias instability of 58.7°/h.[213] Although this result is much higher than fiber optic gyroscopes, which can reach bias

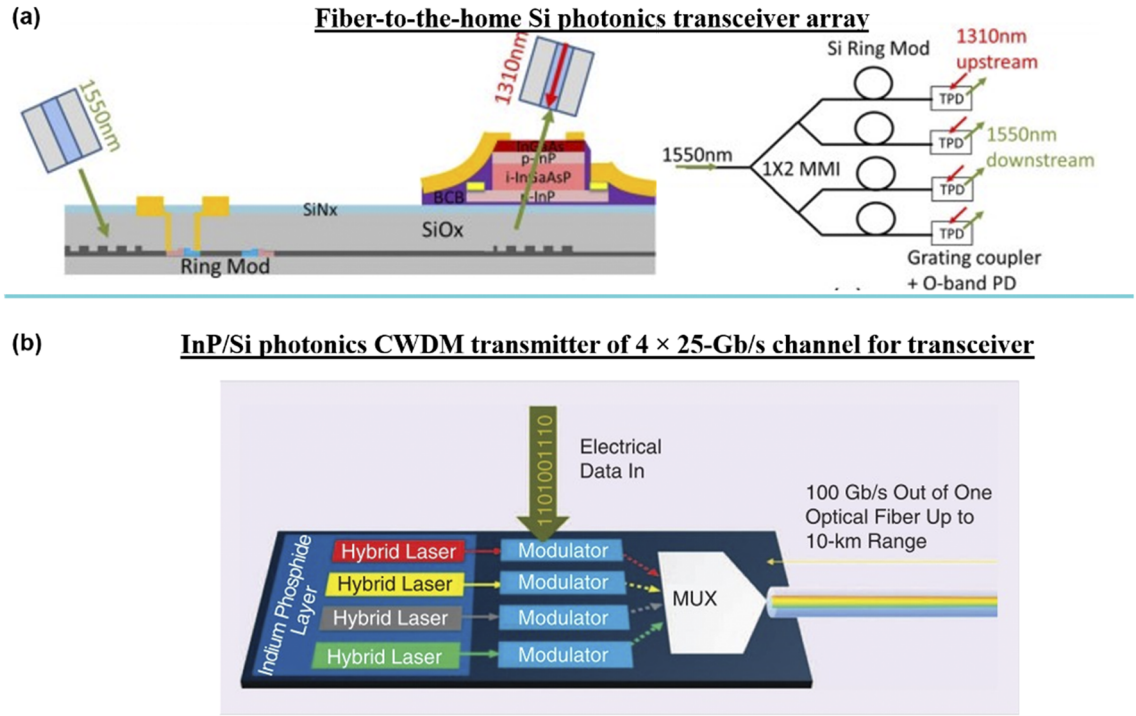

FIG. 17. (a) Schematic layout of the III–V-on-silicon four-channel FTTH transceiver array and cross section of the O-band PD and silicon photonic integrated circuit, reprinted with permission from Zhang *et al.*, Opt. Express **25**, 14290 (2017). Copyright 2017 The Optical Society. (b) Schematic layout of the integrated InP/Si photonic four-channel CWDM transmitter. Reprinted with permission from Jones *et al.*, IEEE Nanotechnol. Mag. **13**, 17 (2019). Copyright 2019 IEEE.

© Author(s) 2021

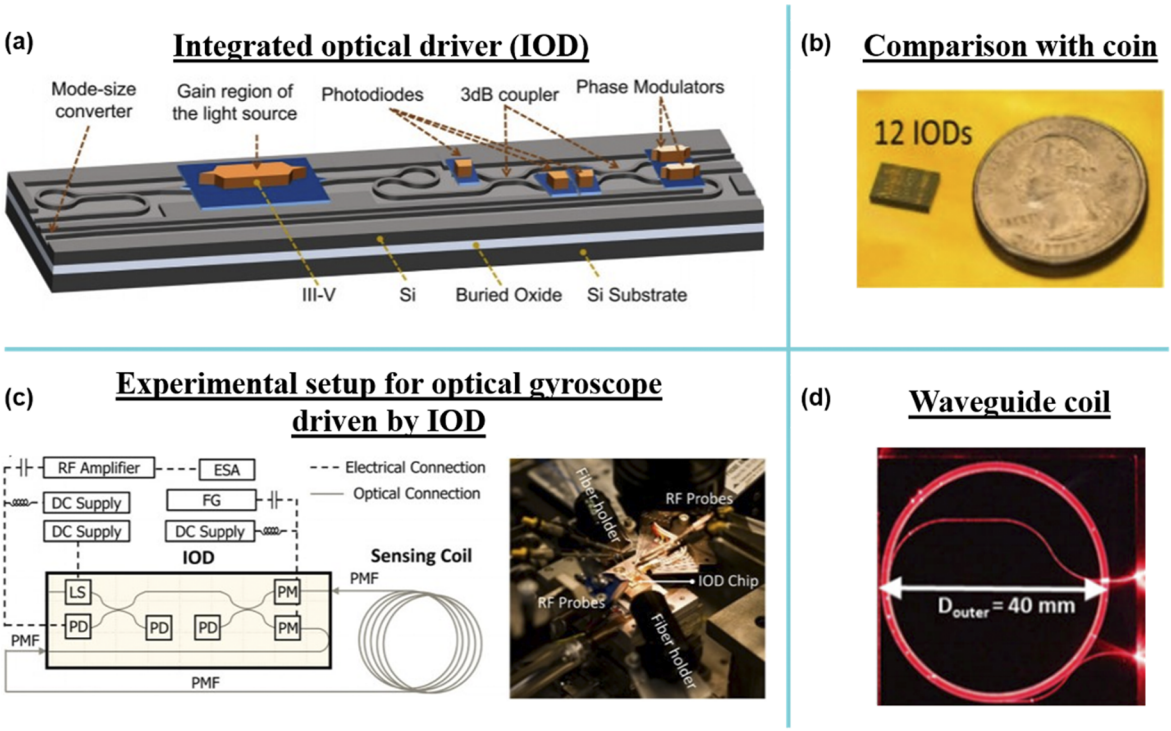

FIG. 18. (a) 3D illustration of the optical engine of the gyroscope, reprinted with permission from Tran *et al.*, Opt. Express **25**, 3826 (2017). Copyright 2017 The Optical Society. (b) A set of 12 individual engines next to a US quarter dollar coin for size comparison, reprinted with permission from Tran *et al.*, Opt. Express **17**, 6252 (2009). Copyright 2009 The Optical Society. (c) Schematic and setup image of the interferometric optical gyroscope driven by the engine, reprinted with permission from Tran *et al.*, Opt. Express **25**, 3826 (2017). Copyright 2017 The Optical Society. (d) Top view of a fabricated 3-m large-area coil waveguide made in SiN, coil illuminated using a red laser, reprinted with permission from Xie *et al.*, Opt. Express **27**, 3642 (2019). Copyright 2019 The Optical Society.

instabilities of 0.0001°/h and below,[214] there is a huge potential to further improve the integrated gyroscopes, making them competitive for the market segment that is currently dominated by using MEMS sensors. Furthermore, replacing the sensing fiber coil with an on-chip waveguide coil (or resonator) will not only shrink down the size but also make it less sensitive to vibration and shock,[211–213] which MEMS sensors are sensitive to.

C. Optical frequency synthesizer

Another excellent example of the power of hybrid and heterogeneous integration is the recent demonstration of an optical frequency synthesizer by using integrated photonics (see Fig. 19).[1] This demonstration required the integration of several optical material technologies in order to utilize each material's strengths: (i) Heterogeneously integrated III–V lasers on silicon photonic waveguides to achieve tunable narrow linewidth lasers; (ii) ultra-high quality factor silica toroid for the generation of a narrow spaced optical frequency comb (22 GHz); (iii) high-quality factor silicon nitride microresonators for the generation of an octave spanning frequency comb with a wide spacing (~1 THz); (iv) GaAs (or $LiNbO_3$) for frequency doubling the ~2 μm comb line, generating ~1 μm wavelength, which is beating with a 1 μm wavelength comb line; and the beat frequency is detected by using (v) high speed III–V photodetectors. Using a combination of hybrid and heterogeneous integration technologies to combine these elements together enabled the demonstration of an optical frequency synthesizer that can be programmed by a microwave clock across 4 THz with 1 Hz resolution and is exceptionally stable across this region with a synthesis error of below 7.7×10^{-15}.[1] Achieving such an outstanding performance in a small package has potential to disrupt research fields such as ultrafast science and metrology,[1] data transmission,[215] physical sensors,[216] and quantum photonics.[217]

VII. FUTURE DIRECTIONS

Hybrid integration and heterogeneous integration enable the integration of an increasing variety of active and passive optical components on photonic integrated circuits. By their nature, active integrated photonics require electrical contacts for the generation, manipulation, and detection of the optical signals, and indeed, the primary motivation for the industrialization of integrated photonics is to relieve the electronic input/output bottleneck; hence, the co-integration with electronic chips within a single package is already being pursued with appropriate interposers.[20] We believe that as the hybrid approaches for mass manufactured transceivers mature, there will be a new wave of densely integrated hybrid photonic chips deployed across a wider variety of applications.

© Author(s) 2021

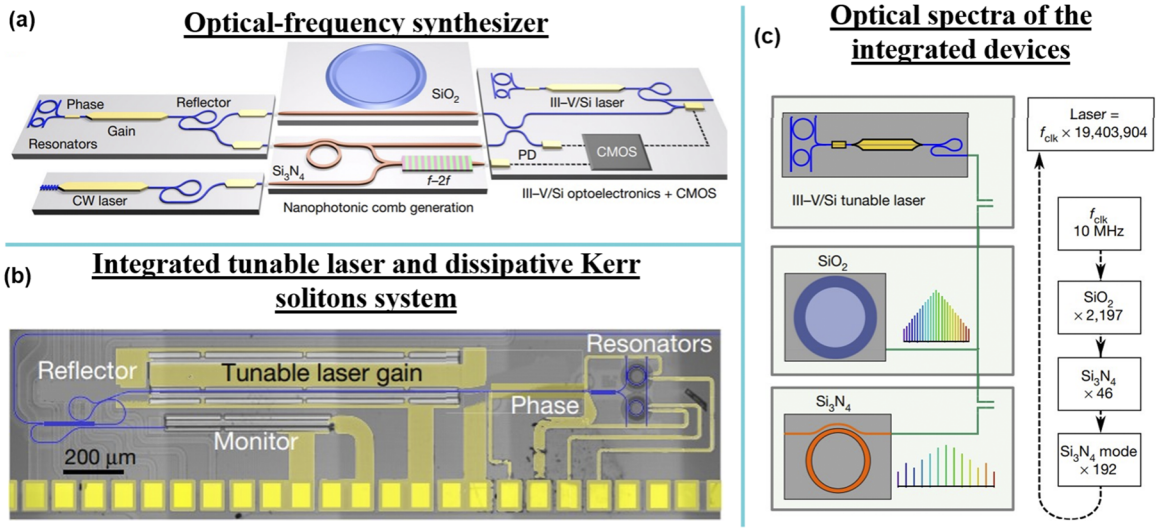

FIG. 19. (a) Illustration of the integrated optical synthesizer by using hybrid and heterogeneous integration methods.[1] (b) Scanning electron microscope (SEM) image of the heterogeneous III–V/Si integrated components of the synthesizer on the chip.[1] (c) Schematic diagram of spectral combination, integrated devices, and with the frequency chain. (a)–(c) are reprinted with permission from Spencer *et al.*, Nature **557**, 81 (2018). Copyright 2018 Nature Publishing Group.

One of the main developments that we foresee is the integration of more exotic materials on photonic integrated circuits. For example, 2D materials have very attractive materials properties that enable the generation, manipulation, and detection of light.[218] Hence, 2D materials will become more attractive over the next few years as the fabrication maturity and control of the material properties increase rapidly. We also believe that there will be a strong push for interfacing photonic integrated circuits with free space optics. Such technology is currently pursued for LIDAR applications, but in the future, one can also image that a similar technology can be used to probe atomic transitions in on-chip vapor cells[219,220] or manipulate ions in complex ion traps.[221,222]

Furthermore, with the emergence of scalable techniques such as micro-transfer printing, in combination with ever improving direct-write maskless approaches, it is conceivable that quite complex hybrid circuits could be "printed" digitally and on demand. This would enable low-cost prototyping and even low volume manufacture of photonic chip products tailored to the specific needs of even quite niche customers. This would lead to an explosion of new applications and opportunities.

VIII. CONCLUSION

The maturity of hybrid and heterogeneous photonic integration technologies is accelerating rapidly, enabling photonic integrated circuit devices with unprecedented functionalities and a reduction in device size, weight, power consumption, and cost. Furthermore, hybrid integration onto a single substrate also provides the additional benefit of increased robustness and potentially more scalable automated manufacture than comparable systems assembled from discrete components. The motivation behind the hybrid and heterogeneous integration for photonic integrated circuits is to use each material according to its strengths featured by the material properties. As an introduction into this field, we provided an overview of some of the most common photonic integrated materials, hybrid and heterogeneous integration concepts, photonic interfaces to transition between the different materials, different integration methods, hybrid and heterogeneous integration examples for real world applications, and an outlook into the future of these technologies in this Tutorial.

We strongly believe that the future of photonic integrated photonics requires photonic circuits that use different material technologies, as the complexity and the requirements for photonic integrated circuits grow with the applications that it enable. Hence, we foresee a bright future of hybrid and heterogeneous photonic integrated circuits with mass production applications, such as high-speed communications and eventually computing. We also anticipate that as this technology matures, it will enable economically viable manufacture of hybrid chips for lower volume niche applications, such as microwave photonics, quantum photonics, precision sensing, metrology, and spectroscopy among many others.

ACKNOWLEDGMENTS

This research was supported by the Australian Research Council, Grant Nos. DP190102773 and DP190101576, and the Australian Department of Industry, Innovation and Science Automotive Engineering Graduate Program (No. AEGP000007).

DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

REFERENCES

[1] D. T. Spencer, T. Drake, T. C. Briles, J. Stone, L. C. Sinclair, C. Fredrick *et al.*, Nature **557**, 81 (2018).
[2] B. Stern, X. Ji, Y. Okawachi, A. L. Gaeta, and M. Lipson, Nature **562**, 401 (2018).

© Author(s) 2021

[3]B. Corcoran, M. Tan, X. Xu, A. Boes, J. Wu, T. G. Nguyen, S. T. Chu, B. E. Little, R. Morandotti, A. Mitchell, and D. J. Moss, Nat. Commun. **11**, 2568 (2020).
[4]Research and markets, https://www.researchandmarkets.com/research/x39z98/photonic?w=5, 2017, p. 93.
[5]M. Bruel, Electron. Lett. **31**, 1201 (1995).
[6]L. Wosinski, Z. Wang, and Y. Tang, in *2010 12th International Conference on Transparent Optical Networks* (IEEE, 2010), p. 16.
[7]F. L. Riley, J. Am. Ceram. Soc. **83**, 245 (2000).
[8]A. E. Kaloyeros, Y. Pan, J. Goff, and B. Arkles, ECS J. Solid State Sci. Technol. **9**, 063006 (2020).
[9]A. E. Kaloyeros, F. A. Jové, J. Goff, and B. Arkles, ECS J. Solid State Sci. Technol. **6**, P691 (2017).
[10]M. Kawachi, Opt. Quantum Electron. **22**, 391 (1990).
[11]J. Wang, A. Santamato, P. Jiang, D. Bonneau, E. Engin, J. W. Silverstone, M. Lermer, J. Beetz, M. Kamp, S. Höfling, M. G. Tanner, C. M. Natarajan, R. H. Hadfield, S. N. Dorenbos, V. Zwiller, J. L. O'Brien, and M. G. Thompson, Opt. Commun. **327**, 49 (2014).
[12]S. F. Fang, K. Adomi, S. Iyer, H. Morkoç, H. Zabel, C. Choi, and N. Otsuka, J. Appl. Phys. **68**, R31 (1990).
[13]J. van der Tol, J. Pello, S. Bhat, Y. Jiao, D. Heiss, G. Roelkens, H. Ambrosius, and M. Smit, Proc. SPIE **8988**, 89880M (2014).
[14]J. Klamkin, H. Zhao, B. Song, Y. Liu, B. Isaac, S. Pinna, F. Sang, and L. Coldren, in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)* (IEEE, 2018), ISBN: 978-1-5386-6503-9.
[15]J. J. G. M. Van Der Tol, Y. Jiao, L. Shen, A. Millan-Mejia, V. Pogoretskii, J. P. Van Engelen, and M. K. Smit, IEEE J. Sel. Top. Quantum Electron. **24**, 6100809 (2018).
[16]S. Fathpour, IEEE J. Quantum Electron. **54**, 6300716 (2018).
[17]C. Xiong, W. H. P. Pernice, and H. X. Tang, Nano Lett. **12**(7), 3562–3568 (2012).
[18]C. Xiong, W. Pernice, C. Schuck, and H. X. Tang, Int. J. High Speed Electron. Syst. **23**, 1450001 (2014).
[19]N. Tansu, H. Zhao, G. Liu, X.-H. Li, J. Zhang, H. Tong, and Y.-K. Ee, IEEE Photonics J. **2**, 241 (2010).
[20]A. H. Atabaki, S. Moazeni, F. Pavanello, H. Gevorgyan, J. Notaros, L. Alloatti, M. T. Wade, C. Sun, S. A. Kruger, H. Meng, K. Al Qubaisi, I. Wang, B. Zhang, A. Khilo, C. V. Baiocco, M. A. Popović, V. M. Stojanović, and R. J. Ram, Nature **556**, 349 (2018).
[21]T. K. Liang, H. K. Tsang, I. E. Day, J. Drake, A. P. Knights, and M. Asghari, Appl. Phys. Lett. **81**, 1323 (2002).
[22]A. D. Bristow, N. Rotenberg, and H. M. van Driel, Appl. Phys. Lett. **90**, 191104 (2007).
[23]L. Gu, V. Srot, W. Sigle, C. Koch, P. van Aken, F. Scholz, S. B. Thapa, C. Kirchner, M. Jetter, and M. Rühle, Phys. Rev. B **75**, 195214 (2007).
[24]D. K. Seo and R. Hoffmann, Theor. Chem. Acc. **102**, 23 (1999).
[25]R. W. Boyd, *Nonlinear Optics*, 3rd ed. (Academic Press, Burlington, VT, 2008).
[26]C. Langrock, S. Kumar, J. E. McGeehan, A. E. Willner, and M. M. Fejer, J. Lightwave Technol. **24**, 2579 (2006).
[27]L. Chang, A. Boes, H. Shu, W. Xie, H. Huang, J. Qin, B. Shen, X. Wang, A. Mitchell, and J. E. Bowers, "Second order nonlinear photonic integrated platforms for optical signal processing," IEEE J. Sel. Top. Quantum Electron. **27**(2), 5100111 (2020).
[28]H. Shimizu, K. Kumada, S. Uchiyama, and A. Kasukawa, Electron. Lett. **37**, 28 (2001).
[29]P. Del'Haye, A. Schliesser, O. Arcizet, T. Wilken, R. Holzwarth, and T. J. Kippenberg, Nature **450**, 1214 (2007).
[30]T. J. Kippenberg, R. Holzwarth, and S. A. Diddams, Science **332**, 555 (2011).
[31]A. J. Mercante, S. Shi, P. Yao, L. Xie, R. M. Weikle, and D. W. Prather, Opt. Express **26**, 14810 (2018).
[32]P. O. Weigel, J. Zhao, K. Fang, H. Al-Rubaye, D. Trotter, D. Hood, J. Mudrick, C. Dallo, A. T. Pomerene, A. L. Starbuck, C. T. DeRose, A. L. Lentine, G. Rebeiz, and S. Mookherjea, Opt. Express **26**, 23728 (2018).
[33]F. Gan, T. Barwicz, M. A. Popović, M. S. Dahlem, C. W. Holzwarth, P. T. Rakich, H. I. Smith, E. P. Ippen, and F. X. Kärtner, in 2007 Photonics in Switching (IEEE, 2007), p. 67.
[34]R. L. Espinola, M. C. Tsai, J. T. Yardley, and R. M. Osgood, IEEE Photonics Technol. Lett. **15**, 1366 (2003).
[35]W. Jin, R. G. Polcawich, P. A. Morton, and J. E. Bowers, Opt. Express **26**, 3174 (2018).
[36]L. Cai, A. Mahmoud, M. Khan, M. Mahmoud, T. Mukherjee, J. Bain, and G. Piazza, Photonics Res. **7**, 1003 (2019).
[37]L. Shao, N. Sinclair, J. Leatham, Y. Hu, M. Yu, T. Turpin, D. Crowe, and M. Lončar, "Integrated microwave acousto-optic frequency shifter on thin-film lithium niobate," Opt. Express **28**(16), 23728–23738 (2020).
[38]T. Komljenovic, M. Davenport, J. Hulme, A. Y. Liu, C. T. Santis, A. Spott, S. Srinivasan, E. J. Stanton, C. Zhang, and J. E. Bowers, J. Lightwave Technol. **34**, 20 (2016).
[39]T. Huffman, M. Davenport, M. Belt, J. E. Bowers, and D. J. Blumenthal, IEEE Photonics Technol. Lett. **29**, 185 (2017).
[40]L. Zhuang, D. Marpaung, M. Burla, W. Beeker, A. Leinse, and C. Roeloffzen, Opt. Express **19**, 23162 (2011).
[41]X. Ji, F. A. S. Barbosa, S. P. Roberts, A. Dutt, J. Cardenas, Y. Okawachi, A. Bryant, A. L. Gaeta, and M. Lipson, Optica **4**, 619 (2016).
[42]L. Scaccabarozzi, M. M. Fejer, Y. Huo, S. Fan, X. Yu, and J. S. Harris, Opt. Lett. **31**, 3626 (2006).
[43]M. Takenaka and Y. Nakano, Opt. Express **15**, 8422 (2007).
[44]C. Wang, M. Zhang, X. Chen, M. Bertrand, A. Shams-Ansari, S. Chandrasekhar, P. Winzer, and M. Lončar, Nature **562**, 101 (2018).
[45]D. Sun, Y. Zhang, D. Wang, W. Song, X. Liu, J. Pang, D. Geng, Y. Sang, and H. Liu, Light: Sci. Appl. **9**, 197 (2020).
[46]H. Yildirim, Opt. Commun. **284**, 2031 (2011).
[47]T. H. Stievater, R. Mahon, D. Park, W. S. Rabinovich, M. W. Pruessner, J. B. Khurgin, and C. J. K. Richardson, Opt. Lett. **39**, 945 (2014).
[48]K. Ikeda, R. E. Saperstein, N. Alic, and Y. Fainman, Opt. Express **16**, 12987 (2008).
[49]I. Shoji, T. Kondo, A. Kitamoto, M. Shirane, and R. Ito, J. Opt. Soc. Am. B **14**, 2268 (1997).
[50]D. Zhu, L. Shao, M. Yu, R. Cheng, B. Desiatov, C. J. Xin, Y. Hu, J. Holzgrafe, S. Ghosh, A. Shams-Ansari, E. Puma, N. Sinclair, C. Reimer, M. Zhang, and M. Lončar, "Integrated photonics on thin-film lithium niobate," Adv. Opt. Photon. **13**(2), 242–352 (2021).
[51]X. Guo, C.-L. Zou, and H. X. Tang, Optica **3**, 1126 (2016).
[52]S. C. Samudrala, "Silicon nitride devices for nonlinear and quantum optics applications," Ph.D. thesis (The University of Texas at Arlington, 2016), available at http://hdl.handle.net/10106/25900.
[53]M. Ferrera, L. Razzari, D. Duchesne, R. Morandotti, Z. Yang, M. Liscidini, J. E. Sipe, S. Chu, B. E. Little, and D. J. Moss, Nat. Photonics **2**, 737 (2008).
[54]M. Dinu, F. Quochi, and H. Garcia, Appl. Phys. Lett. **82**, 2954 (2003).
[55]L. Chang, W. Xie, H. Shu, Q. F. Yang, B. Shen, A. Boes, J. D. Peters, W. Jin, C. Xiang, S. Liu, G. Moille, S. P. Yu, X. Wang, K. Srinivasan, S. B. Papp, K. Vahala, and J. E. Bowers, Nat. Commun. **11**, 1331 (2020).
[56]H. Liang and Q. Lin, "High-Q lithium niobate micro/nano resonators," Ph.D. (University of Rochester, 2019).
[57]X. Liu, P. Ying, X. Zhong, J. Xu, Y. Han, S. Yu, and X. Cai, Opt. Lett. **45**, 6723 (2020).
[58]F. G. Della Corte, G. Cocorullo, M. Iodice, and I. Rendina, Appl. Phys. Lett. **77**, 1614 (2000).
[59]L. Chang, A. Boes, X. Guo, D. T. Spencer, M. J. Kennedy, J. D. Peters, N. Volet, J. Chiles, A. Kowligy, N. Nader, D. D. Hickstein, E. J. Stanton, S. A. Diddams, S. B. Papp, and J. E. Bowers, Laser Photonics Rev. **12**, 1800149 (2018).
[60]G. Li, J. Yao, H. Thacker, A. Mekis, X. Zheng, I. Shubin, Y. Luo, J.-h. Lee, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, Opt. Express **20**(11), 12035–12039 (2012).
[61]J. D. Witmer, J. A. Valery, P. Arrangoiz-Arriola, C. J. Sarabalis, J. T. Hill, and A. H. Safavi-Naeini, Sci. Rep. **7**, 46313 (2017).
[62]B. Snyder, B. Corbett, and P. O'Brien, J. Lightwave Technol. **31**, 3934 (2013).
[63]H. Lu, J. S. Lee, Y. Zhao, C. Scarcella, P. Cardile, A. Daly, M. Ortsiefer, L. Carroll, and P. O'Brien, Opt. Express **24**, 16258 (2016).

© Author(s) 2021

[64]S. Lin, X. Zheng, J. Yao, S. S. Djordjevic, J. E. Cunningham, J.-H. Lee, I. Shubin, Y. Luo, J. Bovington, D. Y. Lee, H. D. Thacker, K. Raj, and A. V. Krishnamoorthy, Opt. Express **24**(19), 21454 (2016).
[65]B. Song, C. Stagarescu, S. Ristic, A. Behfar, and J. Klamkin, Opt. Express **24**, 10435 (2016).
[66]G. de Valicourt, C.-M. Chang, M. S. Eggleston, A. Melikyan, C. Bolle, N. Kaneda, M. P. Earnshaw, Y.-K. Chen, A. Maho, R. Brenot, and P. Dong, J. Lightwave Technol. **35**, 1376 (2017).
[67]A. Moscoso-Mártir, J. Müller, J. Hauck, N. Chimot, R. Setter, A. Badihi, D. E. Rasmussen, A. Garreau, M. Nielsen, E. Islamova, S. Romero-García, B. Shen, A. Sandomirsky, S. Rockman, C. Li, S. Sharif Azadeh, G. Q. Lo, E. Mentovich, F. Merget, F. Lelarge, and J. Witzens, Sci. Rep. **7**, 13857 (2017).
[68]L. Carroll, J. S. Lee, C. Scarcella, K. Gradkowski, M. Duperron, H. Lu, Y. Zhao, C. Eason, P. Morrissey, M. Rensing, S. Collins, H. Y. Hwang, and P. O'Brien, Appl. Sci. **6**, 426 (2016).
[69]Y. Zhu, S. Zeng, and L. Zhu, Photonics Res. **8**, 375 (2020).
[70]M. Rodlin Billah, M. Blaicher, T. Hoose, P.-I. Dietrich, P. Marin-Palomo, N. Lindenmann, A. Nesic, A. Hofmann, U. Troppenz, M. Moehrle, S. Randel, W. Freude, and C. Koos, Optica **5**(7), 876–883 (2018).
[71]J. Justice, C. Bower, M. Meitl, M. B. Mooney, M. A. Gubbins, and B. Corbett, Nat. Photonics **6**, 610 (2012).
[72]X. Luo, Y. Cao, J. Song, X. Hu, Y. Cheng, C. Li, C. Liu, T. Y. Liow, M. Yu, H. Wang, Q. J. Wang, and P. G. Q. Lo, Front. Mater. **2**, 28 (2015).
[73]A. De Groote, P. Cardile, A. Z. Subramanian, A. M. Fecioru, C. Bower, D. Delbeke, R. Baets, and G. Roelkens, Opt. Express **24**, 13754 (2016).
[74]G. H. Duan, X. Pommarede, G. Levaufre, A. Shen, D. Carrara, N. Girard, A. Gallet, D. Make, G. Glastre, J. Decobert, F. Lelarge, R. Brenot, S. Olivier, C. Jany, S. Malhouitre, and B. Charbonnier, in *2016 IEEE 13th International Conference on Group IV Photonics, November* (IEEE, 2016), p. 50.
[75]M. Buffolo, M. Meneghini, C. De Santi, M. L. Davenport, J. E. Bowers, G. Meneghesso, and E. Zanoni, IEEE J. Quantum Electron. **53**, 8400108 (2017).
[76]H. Integrated, I. Si, and D. F. B. Laser, J. Lightwave Technol. **35**, 1235 (2017).
[77]H. Park, C. Zhang, M. A. Tran, and T. Komljenovic, Optica **7**, 425 (2020).
[78]M. J. R. Heck and J. E. Bowers, IEEE J. Sel. Top. Quantum Electron. **20**, 8201012 (2014).
[79]X. Chen, Z. Cheng, C. K. Y. Fung, and H. K. Tsang, Proc. SPIE **8266**, 82660I (2012).
[80]Z. Zhang, X. Shan, B. Huang, Z. Zhang, C. Cheng, and B. Bai, Materials **13**, 2681 (2020).
[81]G. Roelkens, D. Van Thourhout, and R. Baets, Opt. Express **14**, 11622 (2006).
[82]G. Roelkens, D. Vermeulen, S. Selvaraja, R. Halir, W. Bogaerts, and D. Van Thourhout, IEEE J. Sel. Top. Quantum Electron. **17**, 571 (2011).
[83]D. Taillaert, Ph.D. thesis (Universiteit Gent, 2005), p. 167.
[84]Y. Tong, W. Zhou, and H. K. Tsang, Opt. Lett. **43**, 5709 (2018).
[85]X. Chen, C. Li, and H. K. Tsang, IEEE Photonics Technol. Lett. **20**, 1914 (2008).
[86]G. Roelkens, D. van Thourhout, and R. Baets, Opt. Lett. **32**, 1495 (2007).
[87]D. Taillaert, W. Bogaerts, P. Bienstman, T. F. Krauss, P. Van Daele, I. Moerman, S. Verstuyft, K. De Mesel, and R. Baets, IEEE J. Quantum Electron. **38**, 949 (2002).
[88]M. Dai, L. Ma, Y. Xu, M. Lu, X. Liu, and Y. Chen, Opt. Express **23**, 1691 (2015).
[89]A. Michaels and E. Yablonovitch, Opt. Express **26**(4), 4766–4779 (2018).
[90]D. Benedikovic, C. Alonso-Ramos, D. Pérez-Galacho, S. Guerber, V. Vakarin, G. Marcaud, X. Le Roux, E. Cassan, D. Marris-Morini, P. Cheben, F. Boeuf, C. Baudot, and L. Vivien, Opt. Lett. **42**, 3439 (2017).
[91]T. Watanabe, M. Ayata, U. Koch, Y. Fedoryshyn, and J. Leuthold, J. Lightwave Technol. **35**, 4663 (2017).
[92]L. Vivien, D. Pascal, S. Lardenois, D. Marris-Morini, E. Cassan, F. Grillot, S. Laval, J. M. Fédéli, and L. El Melhaoui, J. Lightwave Technol. **24**, 3810 (2006).
[93]D. Taillaert, P. Bienstman, and R. Baets, Opt. Lett. **29**, 2749 (2004).
[94]D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, P. Absil, D. Van Thourhout, and G. Roelkens, Opt. Express **18**, 18278 (2010).
[95]A. Mekis, S. Gloeckner, G. Masini, A. Narasimha, T. Pinguet, S. Sahni, and P. De Dobbelaere, IEEE J. Sel. Top. Quantum Electron. **17**, 597 (2011).
[96]B. Schmid, A. Petrov, and M. Eich, Opt. Express **17**, 11066 (2009).
[97]G. Roelkens, J. Brouckaert, D. Taillaert, P. Dumon, W. Bogaerts, D. Van Thourhout, R. Baets, R. Nötzel, and M. Smit, Opt. Express **13**, 10102 (2005).
[98]R. Wang, M. Muneeb, S. Sprengel, G. Boehm, A. Malik, R. Baets, M.-C. Amann, and G. Roelkens, Opt. Express **24**, 8480 (2016).
[99]N. Na, H. Frish, I. W. Hsieh, O. Harel, R. George, A. Barkai, and H. Rong, in *IEEE International Conference on Group IV Photonics GFP* (IEEE, 2011), Vol. 36, p. 54.
[100]S. Nambiar, P. Sethi, and S. K. Selvaraja, Appl. Sci. **8**, 1142 (2018).
[101]A. Noriki, T. Amano, D. Shimura, Y. Onawa, H. Sasaki, H. Yaegashi, K. Yamada, H. Nishi, T. Tsuchizawa, M. Mori, and Y. Sakakibara, Jpn. J. Appl. Phys., Part 1 **56**, 090302 (2017).
[102]A. Noriki, T. Amano, D. Shimura, Y. Onawa, H. Sasaki, K. Yamada, H. Nishi, T. Tsuchizawa, S. Ukita, M. Sasaki, and M. Mori, J. Lightwave Technol. **34**, 3012 (2016).
[103]C. Marxer, C. Thio, M.-A. Gretillat, N. F. De Rooij, R.Battig, B. Rainer, O. Anthamatten, B. Valk, and P. Vogel, J. Microelectromech. Syst. **6**, 277 (2007).
[104]R. Santos, D. D. Agostino, F. M. Soares, H. R. Haghighi, M. K. Smit, and X. J. M. Leijtens, Advanced Photonics for Communications© 2014 OSA 8, 2014.
[105]A. Noriki, I. Tamai, Y. Ibusuki, A. Ukita, S. Suda, D. Shimura, Y. Onawa, H. Yaegashi, and T. Amano, J. Lightwave Technol. **38**, 3147 (2020).
[106]D. E. Bossi, R. W. Ade, R. P. Basilica, and J. M. Berak, IEEE Photonics Technol. Lett. **5**, 166 (1993).
[107]B. Song, *3D Hybrid Integration for Silicon Photonics* (University of California, Santa Barbara, CA, 2019).
[108]M. J. Deen and P. K. Basu, *Silicon Photonics: Fundamentals and Devices* (Wiley, 2013), ISBN: 978-0-470-51750-5.
[109]Y. Urino, T. Usuki, J. Fujikata, M. Ishizaka, K. Yamada, T. Horikawa, T. Nakamura, and Y. Arakawa, Photon. Res. **2**(3), A1–A7 (2014).
[110]M. Mack, M. Peterson, S. Gloeckner, A. Narasimha, R. Koumans, and P. De Dobbelaere, U.S. patent 8,440,989 (2013).
[111]B. Song, "3D hybrid integration for silicon photonics," Ph.D. thesis (UC Santa Barbara, 2019), available at https://escholarship.org/uc/item/7xf9b62j.
[112]Y. Han, Y. Xue, Z. Yan, and K. M. Lau, J. Lightwave Technol. **39**(4), 940–948 (2020).
[113]H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia, and H. Riel, Appl. Phys. Lett. **106**, 233101 (2015).
[114]L. Megalini, B. Bonef, B. C. Cabinian, H. Zhao, A. Taylor, J. S. Speck, J. E. Bowers, and J. Klamkin, Appl. Phys. Lett. **111**, 032105 (2017).
[115]M. Paladugu, C. Merckling, R. Loo, O. Richard, H. Bender, J. Dekoster, W. Vandervorst, M. Caymax, and M. Heyns, Cryst. Growth Des. **12**, 4696 (2012).
[116]W. Guo, L. Date, V. Pena, X. Bao, C. Merckling, N. Waldron, N. Collaert, M. Caymax, E. Sanchez, E. Vancoille, K. Barla, A. Thean, P. Eyben, and W. Vandervorst, Appl. Phys. Lett. **105**, 062101 (2014).
[117]S. Li, X. Zhou, M. Li, X. Kong, J. Mi, M. Wang, W. Wang, and J. Pan, Appl. Phys. Lett. **108**, 021902 (2016).
[118]Z. Yan, Y. Han, and K. M. Lau, Nanotechnology **31**, 345707 (2020).
[119]L. Vivien, M. Rouvière, J.-M. Fédéli, D. Marris-Morini, J. F. Damlencourt, J. Mangeney, P. Crozat, L. El Melhaoui, E. Cassan, X. Le Roux, D. Pascal, and S. Laval, Opt. Express **15**, 9843 (2007).
[120]J. Yang and P. Bhattacharya, Opt. Express **16**, 5136 (2008).
[121]R. H. Khandokar, M. Bakaul, M. Asaduzzaman, A. Nirmalathas, and S. Skafidas, IEEE J. Quantum Electron. **52**, 8400106 (2016).
[122]X. Mu, S. Wu, L. Cheng, and H. Y. Fu, Appl. Sci. **10**, 1538 (2020).
[123]L. Chang, M. H. P. Pfeiffer, N. Volet, M. Zervas, J. D. Peters, C. L. Manganelli, E. J. Stanton, Y. Li, T. J. Kippenberg, and J. E. Bowers, Opt. Lett. **42**, 803 (2017).
[124]M. L. Davenport, L. Chang, D. Huang, N. Volet, and J. E. Bowers, ECS Trans. **75**, 179 (2016).
[125]M. Lamponi, S. Keyvaninia, C. Jany, F. Poingt, F. Lelarge, G. De Valicourt, G. Roelkens, D. Van Thourhout, S. Messaoudene, J. Fedeli, and G. H. Duan, IEEE Photonics Technol. Lett. **24**, 76 (2011).
[126]M. He, M. Xu, Y. Ren, J. Jian, Z. Ruan, Y. Xu, S. Gao, S. Sun, X. Wen, L. Zhou, L. Liu, C. Guo, H. Chen, S. Yu, L. Liu, and X. Cai, Nat. Photonics **13**, 359 (2019).

© Author(s) 2021

[127]R. Dangel, A. La Porta, D. Jubin, F. Horst, N. Meier, M. Seifried, and B. J. Offrein, IEEE J. Sel. Top. Quantum Electron. **24**, 8200211 (2018).
[128]B. Haq and G. Roelkens, "Alignment-tolerant taper design for transfer printed III-V-on-Si devices," in *European Conference on Integrated Optics* (2019), paper T.P02, available at http://hdl.handle.net/1854/LU-8626768.
[129]B. Shen, H. Lin, F. Merget, S. S. Azadeh, C. Li, G.-Q. Lo, K. A. Richardson, J. Hu, and J. Witzens, Opt. Express **27**, 13781 (2019).
[130]Z. Zhang and C. P. Wong, IEEE Trans. Adv. Packag. **27**, 515 (2004).
[131]D. J. Pedder, Microelectron. Int. **5**, 4 (1988).
[132]H. M. Tong, Y. S. Lai, and C. P. Wong, *Advanced Flip Chip Packaging* (Springer, 2013).
[133]S. Bernabé, C. Kopp, M. Volpert, J. Harduin, J.-M. Fédéli, and H. Ribot, Opt. Express **20**, 7886 (2012).
[134]H. D. Thacker, Y. Luo, J. Shi, I. Shubin, J. Lexau, X. Zheng, G. Li, J. Yao, J. Costa, T. Pinguet, A. Mekis, P. Dong, S. Liao, D. Feng, M. Asghari, R. Ho, K. Raj, J. G. Mitchell, A. V. Krishnamoorthy, and J. E. Cunningham, in *Proceedings of the Electronic Components and Technology Conference* (IEEE, 2010), p. 240.
[135]Y. S. Visagathilagar, W. S. T. Rowe, A. Mitchell, G. Bennett, and M. Grosser, in *Proceedings of the Electronic Components and Technology Conference* (IEEE, 2004), Vol. 1, p. 212.
[136]M. Theurer, M. Moehrle, A. Sigmund, K.-O. Velthaus, R. M. Oldenbeuving, L. Wevers, F. M. Postma, R. Mateman, F. Schreuder, D. Geskus, K. Wörhoff, R. Dekker, R. G. Heideman, and M. Schell, J. Lightwave Technol. **38**, 2630 (2020).
[137]G. Pascariu, P. Cronin, and D. Crowley, in *IEEE/CPMT/SEMI 28th International Electronics Manufacturing Technology Symposium, 2003. IEMT 2003* (IEEE, 2003), Vol. 12, p. 21, ISBN: 0-7803-7933-0.
[138]M. J. Wale, *40th Conference in Proceedings on Electronic Components and Technology* (IEEE, 1990), Vol. 1, p. 34.
[139]T. Shimura, Y. Kawasaki, Y. Ohashi, K. Shirakawa, T. Hirose, S. Aoki, H. Someta, K. Makiyama, and S. Yokokawa, in *1998 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. Digest of Papers* (IEEE, 1998), Vol. 3, ISBN: 0-7803-4439-1.
[140]T. Barwicz, T. W. Lichoulas, Y. Taira, Y. Martin, S. Takenobu, A. Janta-polczynski, H. Numata, E. L. Kimbrell, J.-W. Nah, B. Peng, D. Childers, R. Leidy, M. Khater, S. Kamlapurkar, E. Cyr, S. Engelmann, P. Fortier, and N. Boyer, Opt. Fiber Technol. **44**, 24 (2018).
[141]T. Matsumoto, T. Kurahashi, R. Konoike, K. Suzuki, K. Tanizawa, A. Uetake, K. Takabayashi, K. Ikeda, H. Kawashima, S. Akiyama, and S. Sekiguchi, J. Lightwave Technol. **37**, 307 (2019).
[142]C. Bower, in IEEE CPMT Orange County Chapter Meeting, 2014.
[143]K. Buehler, G. Lorenz, M. Mittag, U. Krieger, N. Heise, S. Wicht, R. Gerbach, and F. Naumann, in 2019 20th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2019.
[144]D. Gomez, T. Moore, M. A. Meitl, S. Bonafede, A. Pearson, B. Raymond, T. Weeks, K. Oswald, E. Radauscher, D. Kneeburg, J. Roe, A. Fecioru, S. Kelleher, R. F. Gul, A. Ferrell, J. Trindade, and C. A. Bower, "Manufacturing capability of micro-transfer printing," in Smart Systems Integration, 13th International Conference and Exhibition on Integration Issues of Miniaturized Systems (2019), pp. 1–4, ISBN: 978-3-8007-4919-5.
[145]J. Yoon, S.-M. Lee, D. Kang, M. A. Meitl, C. A. Bower, and J. A. Rogers, Adv. Opt. Mater. **3**, 1313 (2015).
[146]E. Menard, K. J. Lee, D. Khang, R. G. Nuzzo, and J. A. Rogers, "A printable form of silicon for high performance thin film transistors on plastic substrates," Appl. Phys. Lett. **84**, 5398 (2004).
[147]H. Zhou, W. Qin, Q. Yu, H. Cheng, X. Yu, and H. Wu, Nanomaterials **9**, 283 (2019).
[148]J. Zhang, G. Muliuk, J. Juvert, S. Kumari, J. Goyvaerts, B. Haq, C. Op De Beeck, B. Kuyken, G. Morthier, D. Van Thourhout, R. Baets, G. Lepage, P. Verheyen, J. Van Campenhout, A. Gocalinska, J. O'Callaghan, E. Pelucchi, K. Thomas, B. Corbett, A. J. Trindade, and G. Roelkens, APL Photonics **4**, 110803 (2019).
[149]H. Yang, D. Zhao, S. Chuwongin, J.-H. Seo, W. Yang, Y. Shuai, J. Berggren, M. Hammar, Z. Ma, and W. Zhou, Nat. Photonics **6**, 615 (2012).
[150]A. J. Trindade, B. Guilhabert, D. Massoubre, D. Zhu, N. Laurand, E. Gu, I. M. Watson, C. J. Humphreys, and M. D. Dawson, Appl. Phys. Lett. **103**, 253302 (2013).
[151]J. Zhang, B. Haq, J. O'Callaghan, A. Gocalinska, E. Pelucchi, A. J. Trindade, B. Corbett, G. Morthier, and G. Roelkens, Opt. Express **26**, 8821 (2018).
[152]C. Op de Beeck, B. Haq, L. Elsinger, A. Gocalinska, E. Pelucchi, B. Corbett, G. Roelkens, and B. Kuyken, Optica **7**, 386 (2020).
[153]J. Zhang, A. De Groote, A. Abbasi, R. Loi, J. O'Callaghan, B. Corbett, A. J. Trindade, C. A. Bower, and G. Roelkens, Opt. Express **25**, 14290 (2017).
[154]B. Haq, J. Rahimi Vaskasi, J. Zhang, A. Gocalinska, E. Pelucchi, B. Corbett, and G. Roelkens, Opt. Express **28**, 32793 (2020).
[155]D. Gomez, K. Ghosal, M. A. Meitl, S. Bonafede, C. Prevatte, T. Moore, B. Raymond, D. Kneeburg, A. Fecioru, A. J. Trindade, and C. A. Bower, "Process capability and elastomer stamp lifetime in micro transfer printing," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)* (IEEE, 2016), pp. 680–687.
[156]N. Ahmed, "Advanced instrumented stamps for micro transfer printing and novel applications areas," Ph.D. thesis (University of Illinois at Urbana-Champaign, 2015), available at http://hdl.handle.net/2142/88948.
[157]G. Muliuk, J. Zhang, J. Goyvaerts, S. Kumari, B. Corbett, D. Van Thourhout, and G. Roelkens, Proc. SPIE **10923**, 1092305 (2019).
[158]X. Wang, "Heterogeneous integration technologies based on wafer bonding and wire bonding for micro and nanosystems," Ph.D. thesis (KTH Royal Institute of Technology, 2019), ISBN: 978-91-7873-280-7.
[159]M. A. Schmidt, Proc. IEEE **86**, 1575 (1998).
[160]P. Ramm, J. J. Lu, and M. M. V. Taklo, *Handbook of Wafer Bonding* (Wiley, 2012), ISBN: 9783527326464.
[161]O. Moutanabbir and G. Ulrich, Annu. Rev. Mater. Sci. **40**, 469 (2010).
[162]T. Komljenovic, D. Huang, P. Pintus, M. A. Tran, M. L. Davenport, and J. E. Bowers, Proc. IEEE **106**, 2246 (2018).
[163]J. B. Lasky, Appl. Phys. Lett. **48**, 78 (1986).
[164]M. Shimbo, K. Furukawa, K. Fukuda, and K. Tanzawa, J. Appl. Phys. **60**, 2987 (1986).
[165]D. Pasquariello, M. Camacho, F. Ericsson, and K. Hjort, Jpn. J. Appl. Phys., Part 1 **40**, 4837 (2001).
[166]V. Lehmann, K. Mitani, R. Stengl, T. Mii, and U. Gösele, Jpn. J. Appl. Phys., Part 2 **28**, L2141 (1989).
[167]U. Gosele and Q. Y. Tong, Annu. Rev. Mater. Sci. **28**, 215 (1998).
[168]C. Ventosa, F. Rieutord, L. Libralesso, C. Morales, F. Fournel, and H. Moriceau, J. Appl. Phys. **104**, 123524 (2008).
[169]R. Beneyton, F. Fournel, F. Rieutord, C. Morales, and H. Moriceau, ECS Trans. **3**, 239 (2019).
[170]G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch, and J. Bowers, Laser Photonics Rev. **4**, 751 (2010).
[171]D. Pasquariello, C. Hedlund, and K. Hjort, J. Electrochem. Soc. **147**, 2699 (2000).
[172]D. Pasquariello, M. Lindeberg, C. Hedlund, and K. Hjort, Sens. Actuators, A **82**, 239 (2000).
[173]D. Liang, G. Roelkens, R. Baets, and J. Bowers, Materials **3**, 1782 (2010).
[174]J. M. Ramirez, H. Elfaiki, T. Verolet, C. Besancon, A. Gallet, D. Néel, K. Hassan, S. Olivier, C. Jany, S. Malhouitre, K. Gradkowski, P. E. Morrissey, P. O'Brien, C. Caillaud, N. Vaissière, J. Decobert, S. Lei, R. Enright, A. Shen, and M. Achouche, IEEE J. Sel. Top. Quantum Electron. **26**, 6100213 (2020).
[175]G. Roelkens, D. Van Thourhout, R. Baets, R. Nötzel, and M. Smit, Opt. Express **14**, 8154 (2006).
[176]Y. Tang, J. D. Peters, and J. E. Bowers, Opt. Express **20**, 11529 (2012).
[177]M. L. Davenport, S. Skendžić, N. Volet, J. C. Hulme, M. J. R. Heck, and J. E. Bowers, IEEE J. Sel. Top. Quantum Electron. **22**, 3100111 (2016).
[178]J. Brouckaert, G. Roelkens, D. Van Thourhout, and R. Baets, IEEE Photonics Technol. Lett. **19**, 1484 (2007).
[179]M. H. Francombe, *Handbook of Thin Film Devices* (Academic Press, 2000).
[180]M. L. Davenport, L. Chang, D. Huang, N. Volet, and J. E. Bowers, Electrochem. Soc. **2**, 179–183 (2016).

© Author(s) 2021

[181]M. Piels, J. F. Bauters, M. L. Davenport, M. J. R. Heck, and J. E. Bowers, J. Lightwave Technol. **32**, 817 (2014).
[182]D. Huang, P. Pintus, C. Zhang, P. Morton, Y. Shoji, T. Mizumoto, and J. E. Bowers, Optica **4**, 23 (2017).
[183]Y. Hu, D. Liang, K. Mukherjee, Y. Li, C. Zhang, G. Kurczveil, X. Huang, and R. G. Beausoleil, Light Sci. Appl. **8**, 93 (2019).
[184]T. Hiraki, T. Aihara, Y. Maeda, T. Fujii, T. Tsuchizawa, K. Takahata, T. Kakitsuka, and S. Matsuo, in *European Conference on Optical Communication* (IEEE, 2020), paper Tu1B.
[185]K. Seshan and D. Schepis, *Handbook of Thin Film Deposition*, 4th ed. (Elsevier, 2018), ISBN: 9780128123119.
[186]B. Morrison, A. Casas-Bedoya, G. Ren, K. Vu, Y. Liu, A. Zarifi, T. G. Nguyen, D. Y. Choi, D. Marpaung, S. Madden, A. Mitchell, and B. J. Eggleton, Optica **4**, 847 (2017).
[187]B. J. Eggleton, B. Luther-Davies, and K. Richardson, Nat. Photonics **5**, 141 (2011).
[188]L. Zhang, W. Zhang, X. Wang, P. Zhang, S. Dai, and Q. Nie, Opt. Mater. Express **3**, 1438 (2013).
[189]R. Pant, D. Marpaung, I. V. Kabakova, B. Morrison, C. G. Poulton, and B. J. Eggleton, Laser Photonics Rev. **8**, 653 (2014).
[190]D. Lezal, J. Pedlikova, and J. Zavadil, "Chalcogenide glasses for optical and photonics applications," J. Optoelectron. Adv. Mater. **6**(1), 133–137 (2004).
[191]J.-L. Adam, L. Calvez, J. Trolès, and V. Nazabal, Int. J. Appl. Glass Sci. **6**, 287 (2015).
[192]W. Shen, P. Zeng, Z. Yang, D. Xia, J. Du, B. Zhang, K. Xu, Z. He, and Z. Li, Photonics Res. **8**, 1484 (2020).
[193]Y. Yu, X. Gai, P. Ma, D.-Y. Choi, Z. Yang, R. Wang, S. Debbarma, S. J. Madden, and B. Luther-Davies, Laser Photonics Rev. **8**, 792 (2014).
[194]M. D. Pelusi, V. G. Ta'eed, L. Fu, E. Mägi, M. R. E. Lamont, S. Madden, D. Duk-Yong Choi, D. A. P. Bulla, B. Luther-Davies, and B. J. Eggleton, IEEE J. Sel. Top. Quantum Electron. **14**, 529 (2008).
[195]X. Ji, F. A. S. Barbosa, S. P. Roberts, A. Dutt, J. Cardenas, Y. Okawachi, A. Bryant, A. L. Gaeta, and M. Lipson, Optica **4**, 619 (2017).
[196]M. J. R. Heck, J. F. Bauters, M. L. Davenport, D. T. Spencer, and J. E. Bowers, Laser Photonics Rev. **8**, 667 (2014).
[197]X. Ji, S. P. Roberts, and M. Lipson, "High quality factor PECVD Si3N4 ring resonators compatible with CMOS process," in *Conference on Lasers and Electro-Optics, OSA Technical Digest* (Optical Society of America, 2019), paper SM2O.6.
[198]A. Frigg, A. Boes, G. Ren, T. G. Nguyen, D. Y. Choi, S. Gees, D. Moss, and A. Mitchell, APL Photonics **5**, 011302 (2020).
[199]D. B. Holt and B. G. Yacobi, *Extended Defects in Semiconductors* (Cambridge University Press, Cambridge, 2007).
[200]P.Y. Yu and M. Cardona, *Fundamentals of Semiconductors*, 4th ed. (Springer US, 2010).
[201]K. H. Lee, A. Jandl, Y. H. Tan, E. A. Fitzgerald, and C. S. Tan, AIP Adv. **3**, 092123 (2013).
[202]X.-Y. Bao, C. Soci, D. Susac, J. Bratvold, D. P. R. Aplin, W. Wei, C.-Y. Chen, S. A. Dayeh, K. L. Kavanagh, and D. Wang, Nano Lett. **8**, 3755 (2008).
[203]L. Vivien, J. Osmond, J.-M. Fédéli, D. Marris-Morini, P. Crozat, J.-F. Damlencourt, E. Cassan, Y. Lecunff, and S. Laval, Opt. Express **17**, 6252 (2009).
[204]H. Chen, P. Verheyen, P. De Heyn, G. Lepage, J. De Coster, S. Balakrishnan, P. Absil, W. Yao, L. Shen, G. Roelkens, and J. Van Campenhout, Opt. Express **24**, 4622 (2016).
[205]Y. Han, Z. Yan, W. K. Ng, Y. Xue, K. S. Wong, and K. M. Lau, Optica **7**, 148 (2020).
[206]Y. Xue, Y. Han, Y. Wang, Z. Zhang, H. Ki Tsang, and K. May Lau, Opt. Lett. **45**, 1754 (2020).
[207]A. Marinins, S. P. Dwivedi, J. Kjellman, S. Kerman, T. David, B. Figeys, R. Jansen, D. S. Tezcan, X. Rottenberg, and P. Soussan, Jpn. J. Appl. Phys., Part 1 **59**, SGGE02 (2020).
[208]J. E. Bowers, L. Chang, D. Huang, A. Malik, A. Netherton, M. Tran, W. Xie, and C. Xiang, in *2020 Optical Fiber Communication Conference and Exhibition OFC* (Institute of Electrical and Electronics Engineers, Inc., 2020), p. W3F.1.
[209]R. Jones, P. Doussiere, J. B. Driscoll, W. Lin, H. Yu, Y. Akulova, T. Komljenovic, and J. E. Bowers, IEEE Nanotechnol. Mag. **13**, 17 (2019).
[210]https://optics.org/news/11/5/12, 2020.
[211]M. A. Tran, T. Komljenovic, J. C. Hulme, M. Kennedy, D. J. Blumenthal, and J. E. Bowers, Opt. Express **25**, 3826 (2017).
[212]W. Xie, T. Komljenovic, J. Huang, M. Tran, M. Davenport, A. Torres, P. Pintus, and J. Bowers, Opt. Express **27**, 3642 (2019).
[213]S. Gundavarapu, M. Belt, T. A. Huffman, M. A. Tran, T. Komljenovic, J. E. Bowers, and D. J. Blumenthal, J. Lightwave Technol. **36**, 1185 (2018).
[214]H. C. Lefèvre, Gyroscopy Navig. **3**, 223 (2012).
[215]S. Rumley, D. Nikolova, R. Hendry, Q. Li, D. Calhoun, and K. Bergman, J. Lightwave Technol. **33**, 547 (2015).
[216]T. P. Purdy, K. E. Grutter, K. Srinivasan, and J. M. Taylor, Science **356**, 1265 (2017).
[217]J. L. O'Brien, A. Furusawa, and J. Vučković, Nat. Photonics **3**, 687–695 (2009).
[218]Q. Ma, G. Ren, A. Mitchell, and J. Z. Ou, Nanophotonics **9**, 2191 (2020).
[219]M. T. Hummon, S. Kang, D. G. Bopp, Q. Li, D. A. Westly, S. Kim, C. Fredrick, S. A. Diddams, K. Srinivasan, V. Aksyuk, and J. E. Kitching, Optica **5**, 443 (2018).
[220]Y. Pétremand, C. Affolderbach, R. Straessle, M. Pellaton, D. Briand, G. Mileti, and N. F. De Rooij, J. Micromech. Microeng. **22**, 025013 (2012).
[221]C. Monroe and J. Kim, Science **339**, 1164 (2013).
[222]D. Yang, F. Gao, Q.-T. Cao, C. Wang, Y. Ji, and Y.-F. Xiao, Photonics Res. **6**, 99 (2018).

© Author(s) 2021