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Can Electro-Mechanical Stress Enable Effective Majority Logic Implementations?

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ABSTRACT Theoretically speaking, Majority logic, originally proposed in the ′70*s*, enables more compact and efficient arithmetic implementations than the conventional Boolean counterpart. Nonetheless, CMOS technology based Majority logic realizations remain challenging, as standard transistor-based approaches are unable to directly exhibit majority behavior. However, recent exploration on beyond CMOS technologies created a resurgence of the interest in majority logic. In this work, we propose and analyze a novel approach towards the 3-input Majority gate (MAJ3) implementation by means of piezoelectric materials. By leveraging their intrinsic electromechanical properties, we convert the digital input signals into mechanical deformations, which are accumulated in a transfer layer. Subsequently, we transform the combined deformation back to the electric domain with a piezoelectronics element properly designed to perform majority functionality. We first present the underlying principles behind our proposal with a short introduction on majority logic, piezoelectronics, and the utilized simulation framework. Afterwards we introduce the proposed piezoelectric 3-input Majority gate (piezo-MAJ3) and strategies for optimizing its behavior and performance. We also detail the material parameters and structural design impact on device performance by utilizing both analytical discussion and physics-based simulations. Finally, we shortly highlight how our proposal can be directly integrated into CMOS circuits and compare the piezo-MAJ3 potential cost and performance with the ones of state of the art implementations. Our results indicate that when compared with its CMOS counterpart, the piezo-MAJ3 gate requires half the area, it is 7x faster, while reducing with 44% the energy consumption.

INDEX TERMS Piezoelectric devices, logic circuits, majority logic, beyond CMOS, numerical simulations, mechanical stress, voltage control.

I. INTRODUCTION

Artificial intelligence has undeniably entered the consumer space, and it's growth pace exhibits no signs of slowing down. From Large Language Models (LLM's) to image, audio, and video generators AI technologies are rapidly being adopted across industries - from customer support and coding to the creation of virtual influencers. However, this widespread adoption comes at a cost, as these models heavily rely on high-end GPU's, which consume significant amounts of power [1]. The transistors powering modern GPUs have evolved significantly since their introduction in the 60's [2]. While Interuniversity Microelectronics Centre (IMEC) has released a roadmap for scaling beyond current generations [3], CMOS technology continues to face substantial challenges. Classical frequency scaling plateaued in the 2000's [4], and as channel lengths have shrunk, issues such as leaky currents and quantum tunneling have become more pronounced [4]. Additionally, cooling consumes a larger portion of the power budget than the chip's own power envelope [5]; among others.

To address these issues, alternatives that seamlessly integrate within the existing technological landscape have gained traction. Technologies such as GFETs [6], carbon

TABLE 1. MAJ3 Gate Truth Table

A	B	C	OUT
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	1
0	1	1	1
1	0	1	1
1	1	1	1

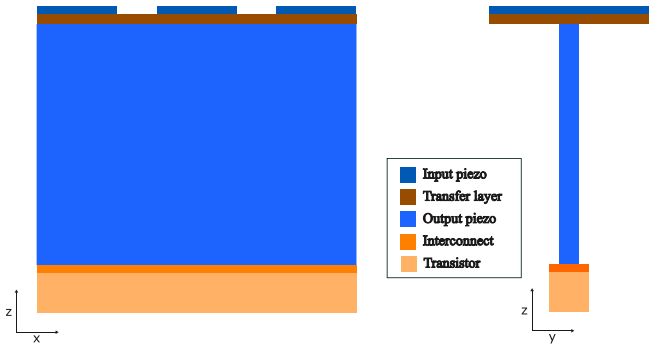

FIGURE 1. Piezo-MAJ3 Gate Structure (all sizing is to proportion).

nanotube [7], and spintronics [8] have emerged as promising candidates to replace traditional silicon transistors. While these emerging technologies demonstrate significant promise, combining them with alternative computing paradigms may offer an even more compelling path forward. Numerous approaches have been proposed, including quantum computing [9], neuromorphic computing [10], majority logic [14], and analog computing [11]. Unlike CMOS, which is poorly suited for implementing these schemes, novel technologies such as spintronics [8] and photonics [12] shine here.

In this paper, we propose a novel method for implementing Majority logic, an alternative logic scheme to the classic Boolean one. By leveraging piezoelectronics, an established technology already utilized in MEMS applications and beyond [23], we demonstrate how a 3-input Majority gate (piezo-MAJ3) can be effectively realized. We present the design and functionality of the piezo-MAJ3 gate, discuss the results of our simulations, illustrate its seamless integration with CMOS logic, and compare its potential cost and performance with the ones of state-of-the-art counterparts.

The rest of the paper is structured as follows. In Section II we briefly discuss Majority logic and piezoelectronics. In Section III we introduce the piezo-MAJ3 gate (structure and utilized materials) and the simulation model. We then analyze and discuss piezo-MAJ3 gate simulations results and potential cost and performance in Section IV. Finally, in Section V we summarize our findings.

II. BACKGROUND

In this section we provide a brief Majority logic and piezoelectronics overview.

A. MAJORITY LOGIC AND GATES

Majority logic, originally a special case derived from Threshold Logic [13], has been studied since the 1970 s. However, it has recently regained prominence due to the growing interest in post-CMOS technologies, and numerous implementations of this logic scheme have been proposed and practically demonstrated [14], [24], [28]. A majority gate is a democratic gate: its output reflects the majority of its inputs, with tie-breaking rules applied in cases of an even number of inputs. In this work, we implement a 3-input majority gate (MAJ3), whose truth table is presented in Table 1. Notably, similarly with NAND/NOR gates, majority gates combined with inverters form a universal gate set, which provides the means for the implementation of any Boolean function. Moreover, recent research indicates that for large-scale circuits, majority gate formulations are often preferred over classical Boolean representations [14], [24], [28]. This preference underscores the potential of beyond CMOS-technologies, e.g., Spintronics [24], that provide natural support for majority logic implementations.

B. PIEZOELECTRONICS

Piezoelectronic materials are widely utilized in power sources [15], sensors [23], actuators [16], frequency modulator [17], motors [16], and more. Their applications span from large-scale systems to micro- and nanoscale devices such as MEMS [17] and transistor gates [18]. Piezoelectricity arises from the ability of certain crystals to accumulate electric charge when subjected to mechanical stress. Conversely, these materials also exhibit the inverse piezoelectric effect, i.e., when an electric field is applied, they generate mechanical strain. This behavior can be mathematically modeled with Equations (1) and (2) in stress-charge form [21]:

$$\sigma = c_E \epsilon - e^T E \tag{1}$$

$$D = e\epsilon + \epsilon_0 \epsilon_{rS} E, \tag{2}$$

where σ is the stress tensor, c_E the elasticity matrix, ϵ the strain tensor, e_T the transposed coupling matrix, E the electric field, D the electrical displacement vector, ϵ_0 the vacuum permittivity, and ϵ_{rS} the relative permittivity tensor.

III. 3-INPUT PIEZO-MAJORITY GATE DESIGN

Fig. 1 depicts front and side views of the 3-input Piezo-Majority device with all dimensions in proportion. The structure consists of:

- Three input electrodes (dark blue) on the top layer,
- A middle transfer layer (brown),
- An output layer (light blue), and

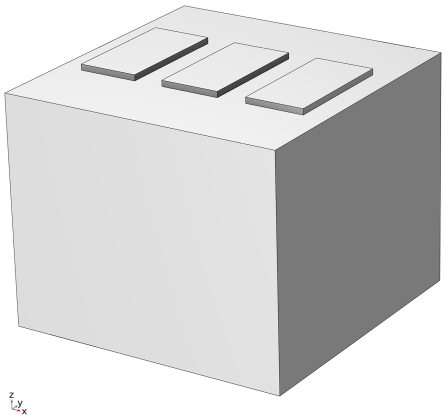

FIGURE 2. Piezo-MAJ3 Gate 3D model. The device is PMMA encased.

- An optional copper interconnect (orange) and a back-gate transistor for thresholding (light orange) at the bottom.

The entire system excluding the top piezoelectric layer, is encased in polymethyl methacrylate (PMMA), as illustrated in the 3D model in Fig. 2.

In a nutshell, the piezo-MAJ3 gate functions as follows: The potentials applied on the 3 inputs generate local stresses, which are captured and accumulated within the transfer layer underneath. Subsequently, the combined stress is passed on to the piezoelectric layer, which transforms it back into a potential. As such, the gate output potential increases in regards to the amount of activated inputs. To properly capture the gate output logic value we augmented our structure with a transistor, but we can also directly connect the structure to an inverter, case which we discuss at the end of Section IV.

A. SIMULATION SETUP

To validate the behavior of the proposed gate we conducted simulations using COMSOL Multiphysics version 6.1 [31]. All materials, except for the amorphous indium-gallium-zinc oxide (a-IGZO), were selected from the COMSOL Multiphyics 6.1 standard material library. The piezoelectric components must maximize strain generation from the input potential or, in the other case the strain induced potential, necessitating materials with high coupling coefficients as one can deduce from Equations (1) and (2). In view of this we made the following material choices:

- Input piezoelectric layer: This layer must generate stress that can be transferred to the transfer layer and consequently the output piezoelectric. We selected PZT-5H for its high elasticity and piezoelectric properties.
- Output piezoelectric layer: A softer material was found to yield better performance, leading us to choose zinc oxide. While alternatives such as polymer composites [19] or lead magnesium niobate (PMN) [20] composites could also be of interests it proved difficult obtaining clear material parameters for these materials.

TABLE 2. a-IGZO Material Parameters [22]

Parameter	Value
Relative permittivity ϵ_r	10
Density ρ	5860 kg/m^3
Band gap Eg_0	3.2 V
Electron affinity χ_0	4.16 V
Valence density of states Nv	$5e24$ $1/m^3$
Conduction density of st Nc	$5e24$ $1/m^3$
Electron mobility μ_n	0.004 $m^2/(V \cdot s)$
Hole mobility μ_p	$1e-5$ $m^2/(V \cdot s)$
Electron lifetime τ_n	10 ns
Hole lifetime τ_p	2 ns
Young's modulus E	$200e6$ Pa
Poisson's ratio ν	0.35

TABLE 3. Piezo-MAJ3 Device Dimensions

Component	x (nm)	y (nm)	z (nm)
Input Piezo	200	400	20
Transfer Layer	800	400	25
Output Piezo	800	50	600
Interconnect	800	100	20
Transistor	800	100	75
Encasing	960	960	770

- Transfer layer: Initially hypothesized to require intermediate hardness, testing revealed that a harder material improves the energy transfer throughout the system. Specifically, in this case a hard material more uniformly applies stress to the output piezoelectric. We therefore utilized Tungsten in our simulations.
- Matrix material: We initially encased the device in SiO_2, but switched to PMMA due to its lower Young's modulus and higher Poisson's ratio, which created a better input/output energy transfer.
- Transistor: The transistor was modeled as a Thin-Film Transistor (TFT) based on simulations in [22]. Material parameters for a-IGZO, listed in Table 2, are also sourced from [22]. a-IGZO was choosen as it has good mobility and has demonstrated excellent on-off ratios. It is also more suited than silicon for more area efficient backend of line transistors as it is not grown by epitaxy.

Device dimensions are detailed in Table 3, with further discussion on sizing being provided in Section IV.

B. SIMULATION PARAMETERS

For our simulations we opted for a default normal sized mesh, with the exception of the transistor where a small swept mesh was applied. All performed studies were stationary and when the semiconductor module was included, a semiconductor initialization step to stabilize the doping was introduced. We utilized the solid mechanics, electrostatics, and piezoelectric effect physics modules and coupled them for our simulations.

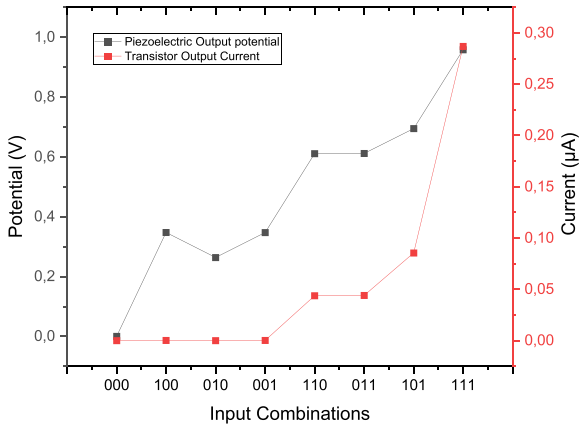

FIGURE 3. Output potential applied to the transistor and subsequent transistor output current.

The bottom of the encasing was fixed to emulate a bottom substrate. For the TFT, we included an analytic doping of 10^{16} cm^{-3}, trap assisted recombination and a thin insulator gate with relative permittivity $\epsilon_0 = 16$, thickness $d_{ins} = 10$ nm, and work function $\Phi = 4.8$ V.

IV. RESULTS

We conducted simulations by utilizing the materials and dimensions detailed in Section III. We assumed that logic $'0'$ is represented by 0 V and logic $'1'$ as -0.5 V. As of note, we apply -0.5 Volt as the use ZnO and PZT-5H strain in opposite directions causing the sign to flip when combining them. This can be through poling the material different during manufacturing. We simulated all possible input values combinations and the results are presented in Fig. 3. In the Figure the left *Oy* axis represents the potential produced by the output piezoelectric and the right *Oy* axis the current flowing through the TFT transistor. From the potential plot, we can clearly distinguish four different output states corresponding to all inputs are $'0'$, one input is $'1'$ and the others are $'0'$, two inputs are $'1'$ and the other $'0'$, and all inputs are $'1'$, respectively. To differentiate between input combinations we employ a transistor for thresholding. The current plot in Fig. 3 demonstrates that, with a correctly biased transistor, current flow can be restricted to cases when more than one input is $'1'$, thus the proposed structure is effectively implementing a majority logic function.

In Fig. 4 we plot the stress components (xx, yy, and zz) for the $'111'$ input combination, with cross sections taken through the middle of the device. We can observe that significant xx and yy stress is generated in the input piezoelectric layer. This stress is then converted to zz stress in the output piezoelectric, which subsequently generates an output potential. In regards to deformation, on the input side you have a expansion of about 1% of the input piezo thickness, which is larger at the corners, which at its turn generates a local expansion of about 1% of the output piezo thickness. Additionally, examining the front view in Fig. 4, we observe that inputs located at the outer edges produce greater stress, resulting in a larger output potential. This effect is evident when comparing the output potentials in Fig. 3 for the input combinations $'100'$, $'010'$, and $'001'$. If necessary, this output disparity can be equalized during the gate deign stage by slightly increasing the thickness or reducing the area of the input piezoelectric, as discusses later in this section.

Given that we demonstrated proper functionality of the piezo-MAJ3 gate it is of interest to analyze the relation between its dimensions and performance in an attempt to optimize its geometry. Note that the open-circuit potential of a piezoelectric element [21], described by Equation (3), provides insight into optimizing device dimensions.

$$V = g * \sigma * t, \tag{3}$$

where, V is the generated potential, g the piezo-electric "g" constant, a material property, and t the thickness of the piezoelectric. For the output piezoelectric, this equation indicates that maximizing the potential requires maximizing both the applied strain (σ) and the thickness (t). Consequently, the output electrode should be sufficiently rigid to maintain its thickness under applied strain. Since strain is defined as $\sigma = F/A$, where F is the applied force and A is the area, the area of the output electrode should be minimized to maximize strain, while the applied force should be maximized. Conversely, the input piezoelectric should be optimized in the opposite manner: maximizing its area and minimizing its thickness to enhance strain generation.

To illustrate the impact of these parameters we simulated various device configurations and the results are graphically presented in Figs. 5 and 6. One can clearly observe in Fig. 6 that reducing the input piezoelectric area and/or increasing its thickness reduces the gate performance. On the other hand, increasing the output piezoelectric area and/or decreasing its thickness is also reducing the gate performance. Therefore for optimal performance we need large, thin inputs and a small, thick output.

To get circuit level sight on the piezo-MAJ3 gate behavior we remove its output transistor and replace it with an inverter, as illustrated in Fig. 7, and perform SPICE simulations. To this end we utilized LTspice [32] with the following transistor models:

- Toshiba SSM3J36FS,LF for the pMOS, and
- Vishay semiconductors SIA517DJ-T1-GE3 for the nMOS.

Fig. 8 depicts the SPICE simulation results for all possible gate input combinations. Note that for the SPICE simulations we utilized the potential outputs provided by COMSOL simulations on which we applied a DC sweep across all gate input combinations. The results demonstrate that the inverter successfully provides inverted MAJ3 output values (an additional inverter is needed if MAJ3 function is required) with clean $'0'/'1'$ logic values.

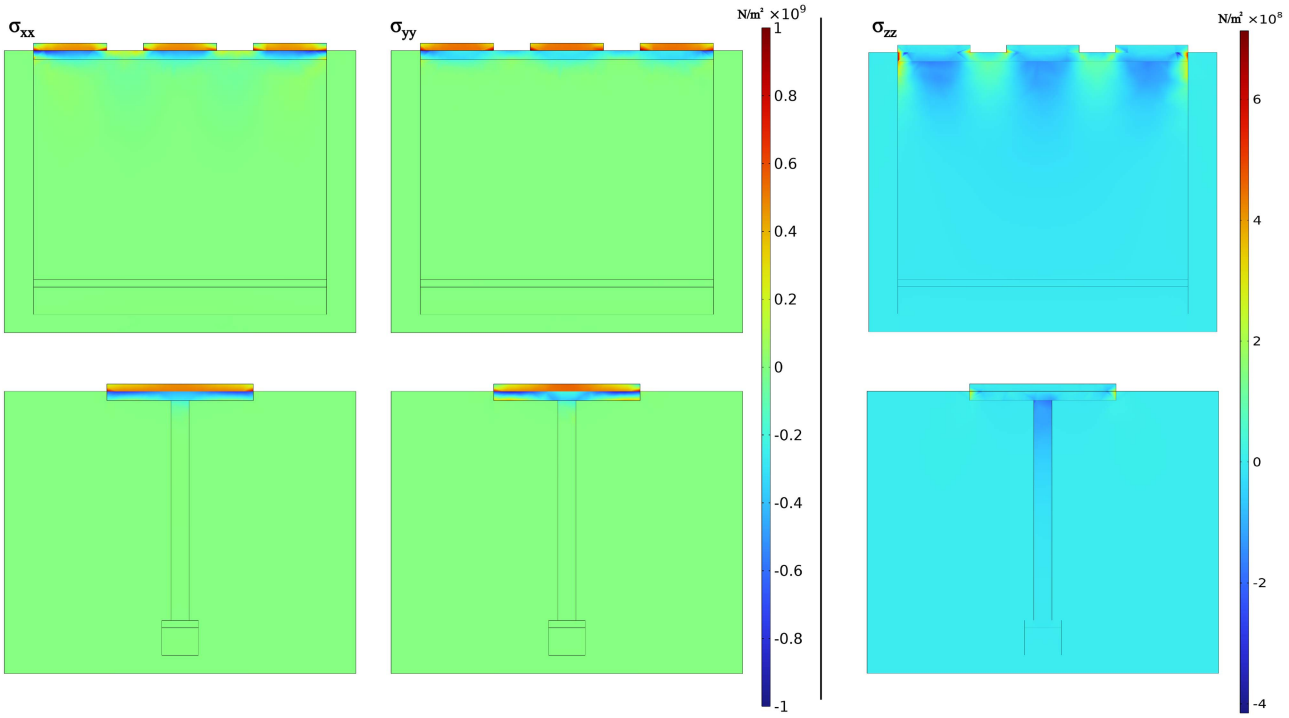

FIGURE 4. Top: Cross-sectional view of the x-z plane at the mid-plane of the device, illustrating the distribution of normal stress components (σ_{xx}, σ_{yy}, and σ_{zz}). Bottom: Cross-sectional view of the y-z plane at the mid-plane of the device, illustrating the distribution of normal stress components (σ_{xx}, σ_{yy}, and σ_{zz}).

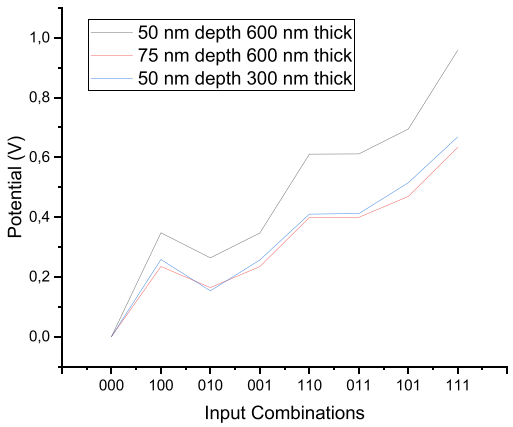

FIGURE 5. Output potential for different output piezoelectric dimensions.

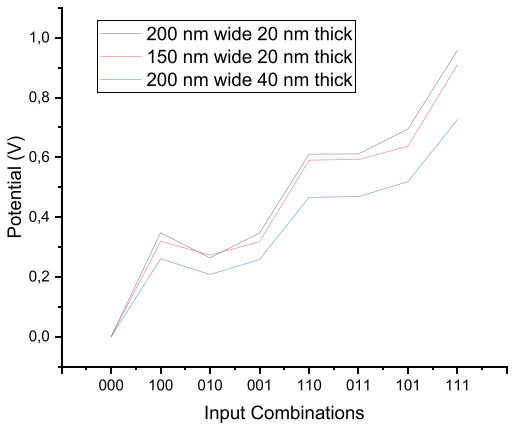

FIGURE 6. Output potential for different input piezoelectric dimensions.

A. PERFORMANCE EVALUATION

Finally, we would like to briefly discuss the cost and performance of our device when compared to other MAJ3 designs, i.e., CMOS implementation (Boolean gate level schematic depicted in Fig. 9) and Spin Waves (SW) interference based implementation [24], [25], [26]. Please note that this is just an attempt to preliminarily compare with other technologies in the field as: (i) our device is by no means optimized and (ii) we could not evaluate it energy consumption, as heating effects were not included in our COMSOL simulations. Moreover, as friction effects we're not included also we can

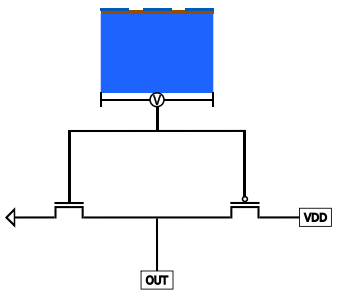

FIGURE 7. piezo-MAJ3 with embedded output inverter; evaluates $\overline{MAJ3}$.

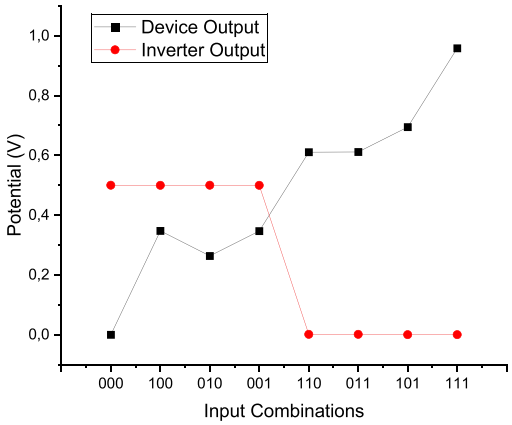

FIGURE 8. piezo-MAJ3 Output for different input combinations.

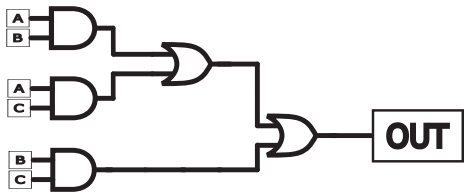

FIGURE 9. 3-input Majority implementation with Boolean gates.

not make any reliability claims. However, we would like to highlight that both PZT and ZnO are materials already in use in MEMS applications and have been found to be reliable in other work [33], [34].

We computed area, delay, and energy consumption estimations for the considered implementations as follows. For the CMOS implementation we assumed a 45 nm technology node for which we utilized a model from [27] and performed SPICE simulations. The implementation of Fig. 9 needs 30 transistors and has a critical path of 9 transistors.

The area, delay, and energy values for the SW majority gate are based on the work in [26]. We note that in [26] the CMOS circuitry necessary for a correct functionality of the SW MAJ3 gate is neglected, thus the actual real-estate value is higher than the one reported inhere. Additionally, in [26] power estimates are assuming Magnetoelectric cell SW transducers, which are still at the concept level and were not practically demonstrated yet.

For the piezo-MAJ3 area calculation we sum-up the area of the COMSOL simulated structure with the one of the inverter assuming a 45 nm technology node [27]. The delay was calculated as the delay of the inverter in addition to the 0.1 ns delay we estimated by means of a COMSOL transient study on the piezo-MAJ3 model. As we could not get inside on the the piezo-MAJ3 energy consumption we built upon data reported in [29], [30], i.e., the energy consumption of a piezoelectric switch can reach as low as 23 aJ. Given that the piezo-MAJ3 gate encompasses three piezo-switches for the inputs, one for the gate output, and an inverter its energy consumption sums up to 0.119 fJ.

TABLE 4. MAJ3 Gate Area, Delay, and Energy Consumption

Technology	Area (μm^2)	Delay (ns)	Energy (fJ)
CMOS	0.61	7.2	0.21
Spin wave	0.085248	0.45	2.743
Piezo	0.32	0.9	0.119

The area, delay, and energy consumption of the considered MAJ3 implementations are summarized in Table 4. One can observe in the Table that, at first glance, the SW implementation is the winner in terms of area and delay, at the expense of higher energy consumption. Note that both figure of merit are neglecting the contribution of the auxiliary CMOS circuitry which could be significant despite the fact that it was neglected in [26]. When focusing on piezo vs CMOS we observe that the piezo-MAJ3 gate requires half the area of the CMOS counterpart, it is 7x faster, and is consuming with 44% less energy.

V. CONCLUSION

In this paper, we introduced a novel piezoelectric-based 3-input majority gate (piezo-MAJ3) and demonstrated its potential to enable effective majority logic implementations. We detailed the working principle of the proposed gate and demonstrated its proper functionality by means of COMSOL and SPICE simulations. We also performed a preliminary evaluation of the piezo-MAJ3 gate area, delay, and energy consumption, which indicated that when compared with its CMOS counterpart, requires half real-estate area, it is 7x faster, while reducing with 44% the energy consumption. Our results clearly indicate the utilization of nonconventional computing technology materials can open unforeseeable avenues towards fast and energy effective computing.

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