

Eight-qubit operation of a 300 mm SiMOS foundry-fabricated device

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Silicon spin qubits are a promising platform for quantum computing due to their high coherence, controllability, and CMOS manufacturability, yet scalable implementations have so far been limited to a few qubits. Here, to take a step towards larger qubit systems, we tune and coherently control an eight-dot linear array of silicon spin qubits fabricated in a 300 mm CMOS-compatible foundry process, establishing operational scalability beyond the two-qubit regime. All eight qubits are successfully tuned and characterized as four double-dot pairs, exhibiting Ramsey dephasing times T_2^* up to 41(2) μ s and Hahn-echo coherence times T_2^{Hahn} up to 1.31(4) ms. Readout of the central four qubits is achieved via a cascaded charge-sensing protocol, enabling high-fidelity measurements of the entire multi-qubit array in a two step process. Additionally, we demonstrate a two-qubit gate operation between adjacent qubits with low phase noise. We show that silicon spin qubit arrays can be scaled to medium-sized arrays of 8 qubits while maintaining system coherence.

Scaling quantum processors from few-qubit demonstrations to viable devices for fault-tolerant quantum computing depends critically on the ability to fabricate, tune, and coherently control larger arrays of qubits with industrially relevant metrics^{1–4}. Among the leading platforms, silicon spin qubits in quantum dots stand out due to their compatibility with CMOS manufacturing^{5–7}, long coherence times in isotopically purified materials, and the possibility of integrating control and readout circuitry in a scalable architecture^{8–10}. Linear spin qubit arrays have been demonstrated in Ge^{11–13} and Si/Ge^{14–18} quantum dots, while CMOS-based implementations have so far been limited to one or two qubits^{19–23}. While fault-tolerant quantum computing will

likely require extending beyond strictly linear arrays to multi-row or two-dimensional architectures^{16,24,25}, linear arrays provide a simple and well-controlled platform for developing and benchmarking qubit control techniques.

Quantum dot spin qubits fabricated in a 300 mm CMOS process can yield low and consistent charge noise across devices²⁶ with single- and two-qubit gate fidelities exceeding 99%^{19,22}. These results demonstrate that the materials, gate stack engineering, and fabrication uniformity required for scaling are already viable. Yet, they remain limited to low qubit counts and do not fully address device variability or coherent operation of qubits across greater linear arrays.

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In this work, we build on the same 300 nm CMOS-compatible fabrication process developed for prior experiments^{19,22} and extend the device and control methodology to an eight-electron spin qubit linear array. We tune all eight dots, characterize single-qubit coherence (T_2^* and T_2^{Hahn}) across the array, and demonstrate the feasibility of two-qubit gate operations among a pair of qubits. We implement a cascaded charge-sensing architecture for the central four qubits to permit simultaneous high-fidelity readout within the extended linear chain^{27,28}. These results demonstrate operational scalability in silicon spin qubits beyond the two-qubit, showing that the fabrication, control, and readout techniques developed in small devices can be translated to larger linear arrays in CMOS-compatible platforms.

Results

Device

The device consists of a linear array of eight quantum dots, with single-electron transistors (SET) integrated at both ends for spin readout (Fig. 1a). The design and fabrication were performed by imec with a 300 nm silicon MOS fabrication workflow on a ^{28}Si wafer, optimized for low noise and defect densities with a residual amount of 400 ppm of ^{29}Si ^{26,29}. The gate geometry and pitch (90 nm) used here were chosen as an evolutionary step in the development of quantum dot fabrication techniques. These parameters can be further optimized for the formation of MOS electron spin qubits by bringing the quantum dots closer together^{22,30}. This improves electrostatic confinement and enables more robust tuning of tunnel coupling and exchange interactions between neighboring qubits³¹.

The device is operated as four unit cells of two qubits per double quantum dot (DQD), which are captured under two neighboring plunger gates (P) each. This technique breaks down the complex task of forming an 8-qubit system into forming mostly independent, well-understood two-qubit systems. Oddly numbered barrier gates (J) control the intra-DQD tunneling while evenly indexed barrier gates

determine the inter-DQD tunnel coupling. A schematic of the gate geometry can be seen in Fig. 1a.

Gate electrodes are made from poly-crystalline silicon to minimize lattice strain compared to historically used aluminum gates^{20,32} and are electrically insulated from each other by an oxide layer. The electrons are simultaneously loaded from the two-dimensional electron gas (2DEG) formed by the lateral SETs, either directly to the adjacent DQDs (P1–P2 or P7–P8) or through them for the two central DQDs P3–P4 and P5–P6. We form a continuous 2DEG from the SET island to the desired dot pair and subsequently raise the dot potential until the desired electron number is acquired. The charge occupations shown in Fig. 1c are chosen to achieve the best possible qubit operating regime. A complete schematic of the electron loading routine, providing independent access to all charge occupations (see Supplementary Fig. 2), is shown in the Supplementary Fig. 1. We expect this technique to be applicable to longer 1D arrays but suggest loading only the edge dots with electrons and shuttling to inner dots for more complex devices to avoid a full reset of charge occupancies. The electrons in each dot form an effective spin-half system that is individually controlled via electron spin resonance (ESR) using a TiN stripline microwave antenna located above the mentioned gate electrodes, applying an oscillating magnetic field B_1 . This field is engineered to be homogeneous across the entire array and oscillates out-of-plane as shown in the schematic in Fig. 1a. Dot pairs from P1–P2 to P7–P8 have respective electron configurations of (9–3), (3–3), (3–7) and (3–1). Larger quantum dots exhibit lower excited-state energies, increasing the influence of surface roughness at the silicon-oxide interface towards dot formation. The electron wavefunction can be modified either by adjusting the electrostatic confinement potential or by changing the electron occupation number. This sensitivity to tuning parameters leads to the observed variation in usable charge occupancies, which may appear arbitrary. Additional charge configurations explored in this work are summarized in Supplementary Table 1. All

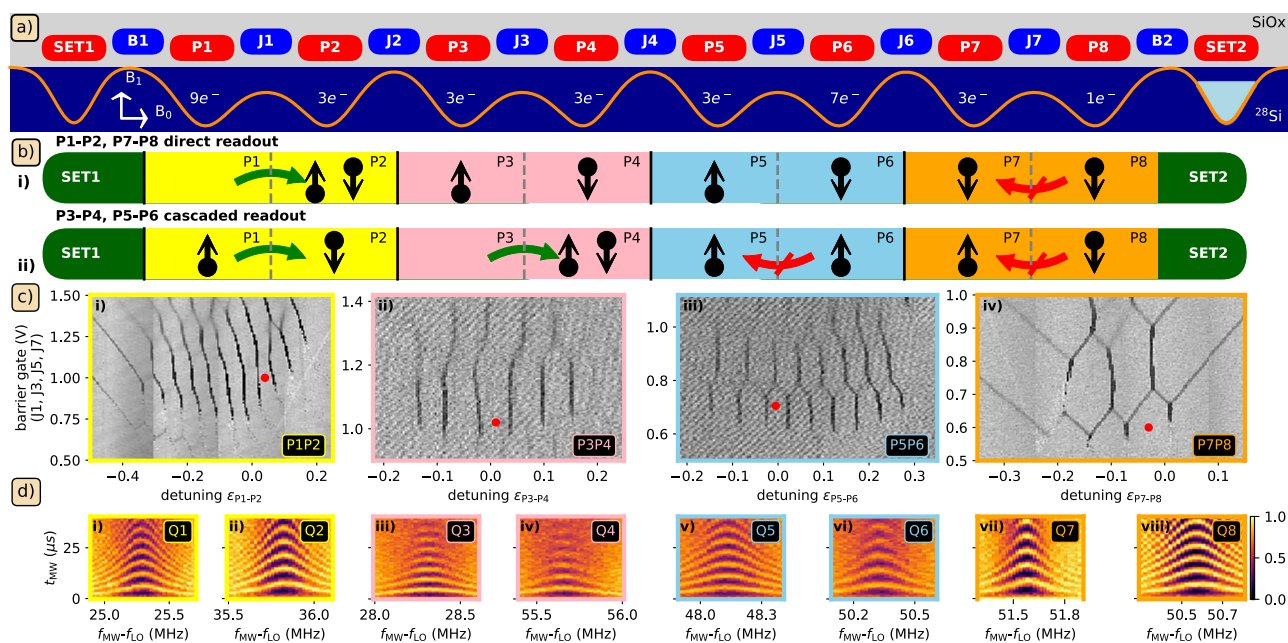


Fig. 1 | Overview of the operation and calibration of an 8-dot device.

a Schematic of cross-section of the device depicting silicon (^{28}Si) substrate, oxide layers (shades of gray), and plunger electrodes (P_i and SET_i) and barrier (J_i and B_i) gates. The electric potential is visualized within the Si substrate with the used electron occupancy. A SEM scan of a similar device is shown in Supplementary Fig. 7. **b** Spin-to-charge conversion readout techniques of the lateral DQDs: (i) P1–P2 and P7–P8 via direct SET readout and the central

DQDs; (ii) P3–P4 and P5–P6 via cascaded readout facilitated by electrons in lateral dots. The left side exemplifies charge movement for odd spin states (green arrows), while the right side exemplifies Pauli spin blockade for even spin states (red arrows). **c** Charge stability maps in isolated mode for (i) P1–P2, (ii) P3–P4, (iii) P5–P6, and (iv) P7–P8. Red circles mark the charge configuration used for the measured qubits. **d** Rabi-chevron measurements for qubits 1–8, shown in (i)–(viii), respectively.

Table 1 | Double quantum dot electron occupations during control, initialization and readout

e ⁻ occupation:	P1-P2	P3-P4	P5-P6	P7-P8
Qubit control	(9-3)	(3-3)	(3-7)	(3-1)
Initialization & readout	(10-2)	(4-2)	(4-6)	(4-0)

measurements are performed in a $^3\text{He}/^4\text{He}$ dilution refrigerator operated at a base temperature of ~ 20 mK with a vector magnet.

Operation

We initialize pairwise spin parity states by detuning the plunger gate voltages to an even-even charge distribution (e.g. from 9-3 to 10-2 in P1-P2) and waiting for 100 μs to allow the spin pair to decay to its ground state $|\uparrow\downarrow\rangle/|\downarrow\uparrow\rangle$. By ramping back to the operational (e.g., 9-3 in P1-P2) odd-odd charge configuration diabatically, one can initialize the mixture of odd states $|\downarrow\uparrow\rangle$ and $|\uparrow\downarrow\rangle$, respectively. Pure spin states are initialized by ramping to a T_1 decay-hotspot within the qubits odd-odd electron configuration and confirming success by collapsing the wavefunction to the $|\downarrow\downarrow\rangle$ state by measurement via a heralding protocol^{20,23}. We utilize Pauli spin blockade (PSB) to read the qubit pairs' spin parity state^{33,34}. Polarized triplet states prevent charge movement from dot 1 to dot 2 when ramping to the PSB region, whereas unpolarized parity states are free to tunnel. Those charge movements are captured by the SET³⁴. All electron occupations during the described operating regimes are given in Table 1.

The central four dots P3-P6 are measured via electron cascading where PSB readout is performed, but the lateral sub-systems are tuned to be close to their electron anti-crossing while being in an unblockaded spin state. A charge movement in P3-P4 or P5-P6 triggers an electron cascade in P1-P2 or P7-P8, respectively, which is then read out with an increased SNR by the SETs compared to directly sensing the central part of the device²⁷. This cascaded readout scheme is designed to keep the number of electrons in each DQD constant. Figure 1b-ii provides a schematic of the unblockaded PSB readout cascade on the left half of the device and the blockaded on the right half. Calibration and the difference in visibility are shown in Supplementary Fig. 4.

Spin up and down states are split by the Zeeman energy ~ 14 GHz (~ 58 μeV) due to an external in-plane DC magnetic field of $B_0 = 0.5$ T. Small differences in electron g -factors allow direct addressability of all qubits with separate resonant ESR pulses³⁵. Single-qubit gates $X_{\pi/2}$ are realized by resonantly exciting the electrons with a timed microwave pulse, while $Z_{\pi/2}$ gates are applied by a virtual phase shift in the microwave source³⁶. The Heisenberg exchange interaction between two neighboring qubits is controlled via baseband control of the barrier gates J by which controlled phase gates (CZ) are realized^{32,37,38}. The SET top-gate operation voltage and the qubits' Larmor frequencies are being tracked and corrected by real-time feedback protocols³⁹.

All measurements were performed with the given electron numbers in each dot provided in Table 1 with results of the lateral double dots being acquired simultaneously. The same is true for the characterization of the two central pairs.

Qubit characterization

All eight quantum dots were tuned to accommodate a qubit each by adjusting gate voltages and operational parameters for initialization, control and readouts. Rabi chevrons of all measured qubits are shown in Fig. 1d. The extended top-gate dimensions and the pitch to their neighbors did not facilitate the most obvious electrostatic gate voltage configuration by applying a similar voltage on all gates. Significantly more negative potentials were applied to evenly indexed barrier gates in order to spatially confine electron pairs, enabling the formation of qubits.

The qubits' g -factors are distributed over $\Delta g = 2.17 \times 10^{-3}$ from each other, allowing individual addressability via ESR drive. Figure 2a shows their individual, relative g -factors. A larger spread of $\Delta g = 7 \times 10^{-3}$ has been predicted from atomistic tight binding simulations in a similar platform³¹. The difference is likely to be due to the larger dot sizes in this work. Similar Larmor frequencies are particularly interesting for global control techniques where qubits are constantly driven to allow scalable qubit base-band control and decouple qubits from quasi-static noise^{40,41}. Further, variations of g -factors can be modified by changing the angle of B_0 as shown in Supplementary Fig. 6^{31,42,43}.

Qubit Rabi frequencies are all in the range 141(1)–204.5(6) kHz (Fig. 2b). This, together with the lack of significant Rabi frequency change as a function of gate voltages, hints towards mostly magnetic drive through the used line antenna^{44,45}. Consistent Rabi speeds are further favorable for global control protocols^{40,46}. Qubit driving frequencies are limited by the distance of the microwave antenna to the quantum dots compared to similar devices^{20,21}. Further, the power on the antenna was kept low due to the observation of Larmor frequency shifts as a function of the driving amplitude, likely stemming from heating effects^{37,47,48}. The reduced Rabi speeds compared to similar devices^{20,22,30} are likely attributable to the antenna design and distance from the qubit array, rather than to an inherent limitation of the qubits themselves. Temporal ensemble coherence times T_2^* , summarized in Fig. 2c are measured within a ~ 4 min time window by performing a Ramsey-type experiment followed by a state projection along all directions on the Bloch-sphere to calculate the state purity. The qubits provide up to 41(2) μs of coherence, with an average of 21(9) μs . Hahn-echo coherence times T_2^{Hahn} reach up to 1.31(4) ms, with an average of 0.7(4) ms, as shown in Fig. 2d. These values and variations are comparable to those reported for devices fabricated using a similar foundry process²², and exceed results from devices fabricated in academic facilities^{20,30}.

Reliably controlling electron exchange within a given DQD is not trivial with the given top-gate layout due to dots forming underneath the barrier gate [see Fig. 1c (iv) and Supplementary Fig. 5a] or by significant lateral shifts of the electrons' spatial distribution [see right half of Fig. 1c(i)] with increasing voltage on the barrier gates. By loading a sufficient number of electrons into the P1-P2 sub-system, we found an occupation providing a continuous range of J voltages without causing charge movements. The remaining DQDs did not show exchange branching of their qubits' electron spin resonance spectrum before one of the electrons tunneled to another spurious quantum dot. To characterize the CZ gate, we prepare one qubit in a superposition state $|\psi\rangle = \frac{1}{\sqrt{2}}(|\uparrow_1\rangle + |\downarrow_1\rangle) \otimes |\downarrow_2\rangle$ and ramp to a certain gate voltage on J as well as detuning $\epsilon_{\text{P1-P2}}$ for a fixed wait time of 1 μs . The qubit state is projected along the positive and negative x - and y -axis of the Bloch sphere, using $\pm X_{\pi/2}$ and $\pm Y_{\pi/2}$ single qubit to determine the qubit's phase accumulation. This so-called 'finger-print' measurement is shown in Fig. 3a.

Despite the non-uniform geometry of the quantum dots' charge stability, the phase coherence is well preserved, hinting at low charge noise in the vicinity of the qubits⁴⁹. The finger-print map further reflects the bent structure of inter-dot electron crossings and even suggests a diagonal intra-dot transition above 150 mV, resulting in a sudden speed up of exchange oscillations²¹. This measurement is repeated without applying a gate detuning $\epsilon_{\text{P1-P2}}$ while varying the wait time at the exchange voltage, as shown in Fig. 3b. The inset displays the exchange speed for each barrier gate voltage and an exponential turn-on of 33.69(1) dec/V in qubit exchange is determined.

Figure 3c shows the tuning of the phase adjustment of the CZ gate over up to 38 gate repetitions. Black and orange horizontal line cuts are shown in Fig. 3d. The barrier gate voltage is increased via a square pulse for each CZ gate repetition; further pulse engineering can still improve the repeatability of the phase rotation.

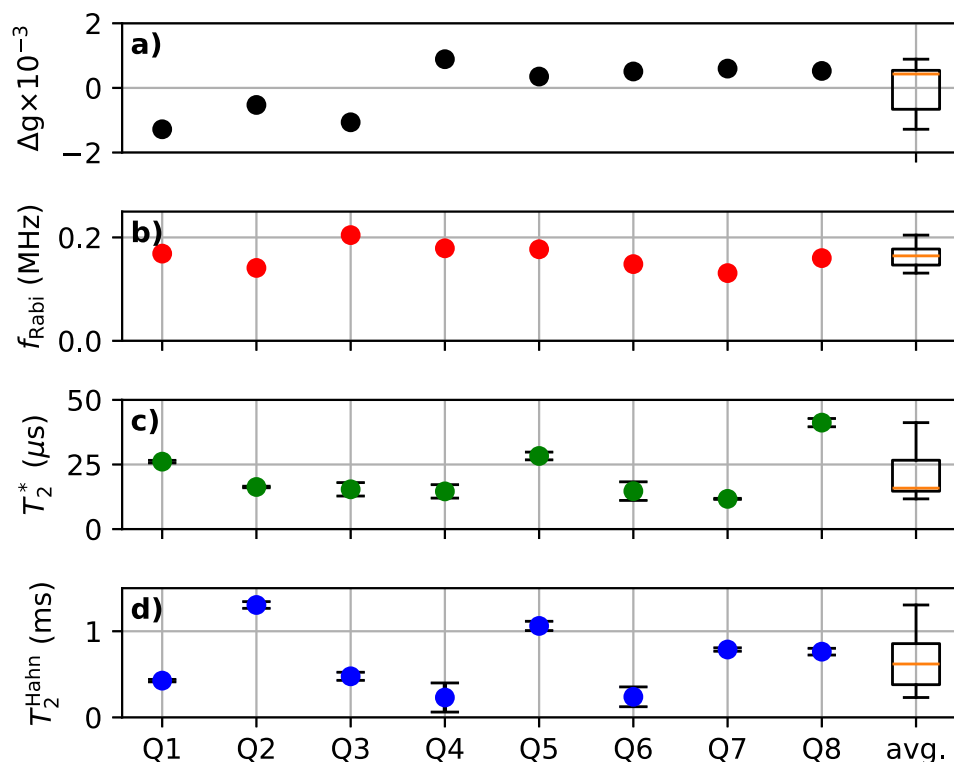


Fig. 2 | Qubit characteristics summary. **a** Larmor frequencies, **b** Rabi frequencies, **c** Ramsey coherence times T_2^* , and **d** Hahn echo coherence times T_2^{Hahn} . Error bars indicate one standard deviation. The box symbol shows the spread of values as well as their mean and standard deviation.

Qubit exchange in the remaining DQDs did not turn on with barrier gate voltage, except for DQD P7–P8, which showed a sudden increase in exchange interaction as shown in Supplementary Fig. 5b. It is possible that with even higher electron occupancies, the valence electrons' wave functions overlap is increased to facilitate smooth qubit exchange⁴⁴. Devices from a similar foundry process with reduced gate size and pitch, as reported in ref. 22, have shown reliable and high-fidelity exchange control across all devices. Similarly, ref. 30 demonstrates that smaller gate pitches in a university-fabricated device enable reliable exchange among all neighboring qubits. Albeit this is not a demonstration of the scalability of two-qubit gate tuning, it shows low electrical noise being present in devices from this fabrication process^{22,50}.

Discussion

This work presents the coherent operation of eight silicon spin qubits in a 300 mm foundry-fabricated linear quantum dot array. All eight qubits were successfully tuned and individually addressed, exhibiting coherence times consistent with or close to state-of-the-art^{22,51}. Double quantum dot cells, as they are calibrated in this work, break down the tuning complexity into $N/2$ units. To verify this approach, entangling gates among qubit pairs remain to be demonstrated. This was not easily feasible here, given the gate dimensions of the device and the expected shape of the electrons' wave functions³¹. Increasing the number of electrons captured in a dot increases the size of the qubits' wavefunction^{44,52} and thus the qubits' potential to exhibit Heisenberg exchange with its neighbors. However, the higher charge occupancy leads to a tradeoff between expanded tuning complexity, lower charging energies and low excited state energies^{44,52}.

One-dimensional qubit arrays are a starting point to develop synchronous control techniques, giving insight into qubit statistics, and potentially enabling initial error correction codes⁵³. Scalable, fault-tolerant spin qubit-based error mitigation routines require higher-order qubit connectivity like bi-linear^{16,24} or sparse 2D arrays²⁵. A

dielectric resonator should be used for qubit driving in the higher-dimensional architectures^{54,55}, and the global driving scheme^{40,41,56} to scale single-qubit driving. Demonstrating on-demand control over more complex multi-quantum dot structures will enable the investigation of many proposed error-correction schemes that are the foundation of a large-scale quantum computer. Looking forward, continued progress in fabrication, including refined lithographic techniques, will be necessary to reduce feature sizes while preserving yield and uniformity, enabling robust qubit confinement and reliable exchange control in larger-scale devices.

Methods

Fabrication

The device was fabricated at imec using a 300-mm wafer process engineered for low charge noise, high uniformity, and qubit-specific integration with a 90 nm gate pitch^{26,29}. Optical and electron-beam lithography were combined to balance throughput with patterning precision. The starting material was an epitaxially grown silicon layer isotopically purified to a residual ²⁹Si concentration of 400 ppm. Thermal oxidation of the silicon surface yielded the Si/SiO₂ interface where the electron spin qubit is hosted, with the interface quality maintained through dedicated cleaning steps. A triple-layer overlapping polysilicon gate stack was defined by electron-beam lithography and dry etching, with adjacent gates isolated by thin interstitial high-temperature oxide. Highly doped polysilicon was used to minimize interface strain at cryogenic temperatures. An aluminum strip line antenna above the qubit array was integrated to enable electron spin resonance control of individual spin states.

Measurement

The device was cooled in an Oxford Instruments Kelvinox 400HA dilution refrigerator. An Oxford Instruments Mercury IPS controlled the internal vector magnet, providing a static magnetic field of 0.5 T, chosen to place the qubit Larmor frequencies in a regime where the on-

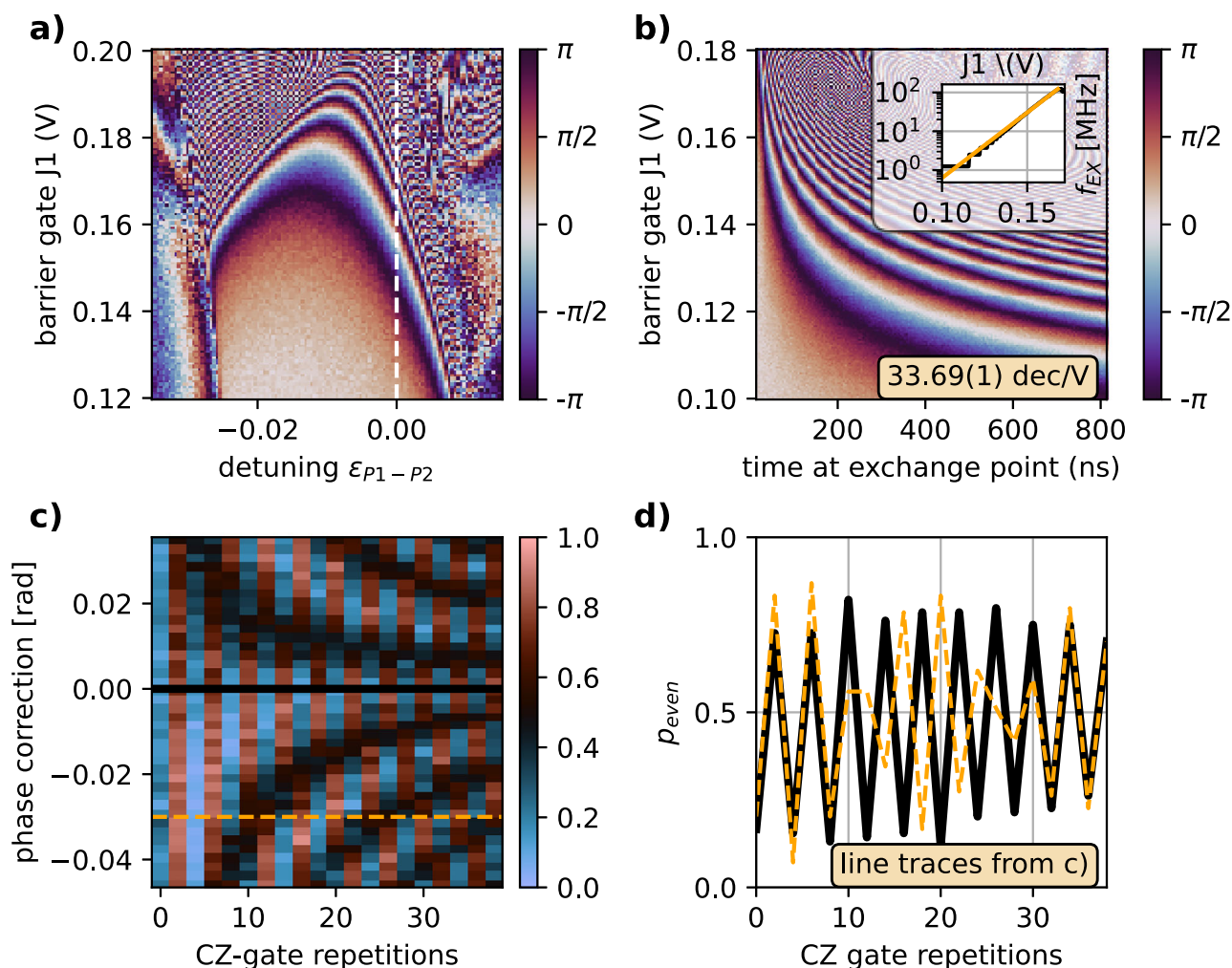


Fig. 3 | Two-qubit exchange in P1-P2. **a** Exchange decoupled 'fingerprint' map at a fixed exchange period of 1 μ s for barrier gate voltage J_1 vs. P1-P2 detuning voltage. **b** Exchange oscillations vs. barrier gate voltage J_1 . The scan is performed along the

white dotted line in (a). **c** Phase calibration of controlled-phase gate (CZ). **d** Line cuts along the black and orange line in (c).

chip stripline antenna operates efficiently. d.c. bias voltages were applied through filtered lines (bandwidth ≤ 30 Hz) via a Q-Devil QDAC-II. A Quantum Machines OPX1000 served as the central controller for pulse generation, with a 1 ns sampling time on LF-FEM baseband modules. Voltage pulses were combined with d.c. offsets at room temperature using custom linear bias combiners and delivered through lines with a 50 MHz bandwidth, imposing a minimum rise time of 20 ns that was mitigated by smoothing fast pulse edges. Microwave excitation up to 10.5 GHz was provided by the MW-FEM module integrated within the OPX1000, which also synthesized the in-phase, quadrature, and pulse modulation waveforms. The dedicated Keysight E8267C vector signal generator was used to synthesize pulses up to 20 GHz with baseband in-phase and quadrature pulses from an OPX LF-FEM module. Charge readout was performed via two SETs in d.c. mode, placed on the lateral ends of the qubit array. The sensor current was integrated over $t_{int} = 100 \mu$ s, converted to a voltage with a room-temperature transimpedance amplifiers (Basel SP983c), and digitized by the OPX1000.

Data availability

The data supporting this work is available in a Zenodo repository (19583373) as a QCoDeS database.

Code availability

All results were acquired using a custom open-source measurement framework, with data analysis performed using the associated inspection tools [arbok-driver](#) and [arbok-inspector](#).

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Author contributions

A.N. conducted the experiments under T.T. and A.S.D.'s supervision and with input from N.D.S., A.S., A.L., C.H.Y., P.S., J.D.C., M.K.F., S.S., E.V. and C.C.E. The imec team, consisting of S.K., J.J., Y.C., S. Baudot, Y.S., R.L., C.G., B.R., S. Beyne and D.W. and led by K.D.G., developed the 300 mm spin-qubit process, fabricated the device and performed an initial electrical device screening at wafer-scale. W.H.L., K.W.C. and F.E.H. packaged the device for measurements. A.N. wrote the paper with the input of all authors.

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Competing interests

A.S.D. is the chief executive officer and a director of Diraq Pty Ltd. N.D.S., W.H.L., T.T., M.K.F., S.S., J.D.C., E.V., F.E.H., K.W.C., A.L., C.H.Y., A.S., C.C.E. and A.S.D. declare equity interest in Diraq. The other authors declare no competing interests.

Additional information

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