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Fabrication of a thin, flexible chip package using liquid crystal polymers

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ABSTRACT

Thin, flexible packaging of integrated circuits (ICs) is essential for next-generation implantable devices, where extreme miniaturisation must be achieved without compromising reliability. This work presents a fabrication process for ultrathin chip packages based on liquid crystal polymer (LCP), selected for its biocompatibility, chemical stability, and barrier properties. Dies thinned to 30 μ m were embedded into laser-skived cavities within a high- and low-temperature LCP stack using vacuum lamination. Electrical access was achieved using a hybrid picosecond-laser and reactive ion etching (RIE) via process, followed by metallisation and fan-out patterning. The approach was validated using PTCE daisy-chain structures and MSP430 microcontrollers. Across 11.704 vias, all were electrically functional with negligible resistance contribution. Of 16 encapsulated MSP430 devices, 62.5% remained programmable. Assembly on flexible substrates yielded high pad-level connectivity (96.8% PTCE, 99.1% MSP430) and 75% functional yield. Full LCP encapsulation was demonstrated as a proof of concept, confirming the feasibility of this scalable ultrathin packaging approach.

1. Introduction

Active medical implants are increasingly relevant and currently exist for a variety of applications such as brain stimulation, cardiac monitoring and stimulation, and emerging neuromodulation therapies. The major challenge in fabricating such implantables lies in achieving miniaturisation without compromising device longevity. Today, most long-term implantable electronics rely on rigid titanium housings, which exhibit excellent long-term reliability but are rigid and large, increasing biological impact and restricting the number of potential implantation locations [1]. This has motivated a shift towards thin, flexible, polymer-based implantable systems [2].

Among polymer materials compatible with thin-film microfabrication, three candidates stand out: polyimide, parylene-C, and Liquid Crystal Polymer (LCP) [3–6]. Polyimide combined with ALD layers can yield excellent barrier performance but the layer thickness and the use of spincoating limits its ability to encapsulate circuits with significant topography [7,8]. Parylene-C provides highly conformal coverage and has been used successfully in simple neuromodulation implants, though its relatively low thermal stability constrains subsequent processing steps [9–11]. Additionally, parylene-C has relatively low hermeticity and must be combined with additional layers such as ALD to improve the barrier properties, increasing process complexity and cost [12,13]. LCP offers an appealing alternative due to its biocompatibility, low moisture uptake, and outstanding chemical and thermal stability [14,15]. Its lamination-based processing yields hermetic multilayer structures and enables the embedding of components, making it increasingly attractive for highly integrated implantable systems [16].

Before LCP emerged in biomedical research, it had already gained significant traction in high-frequency and microwave electronic packaging, where its low dielectric constant, low moisture absorption, and dimensional stability enabled fabrication of substrates for high frequency applications such as antennas and integration of RF chips into multilayer substrates [17,18]. Early work in this domain also showed that LCP could be processed into both rigid and flexible substrates compatible with wire-bonding, flip-chip assembly, and lead-free solderings [19]. More recently, the use of LCP has been explored for highly demanding applications such as space applications [20] and has extensively been tested for long-term durability [21–23].

For biomedical applications, Dyconex AG has demonstrated highly reliable multilayer LCP technologies for implantable substrates and electrodes, achieving consistent electrical performance and long-term

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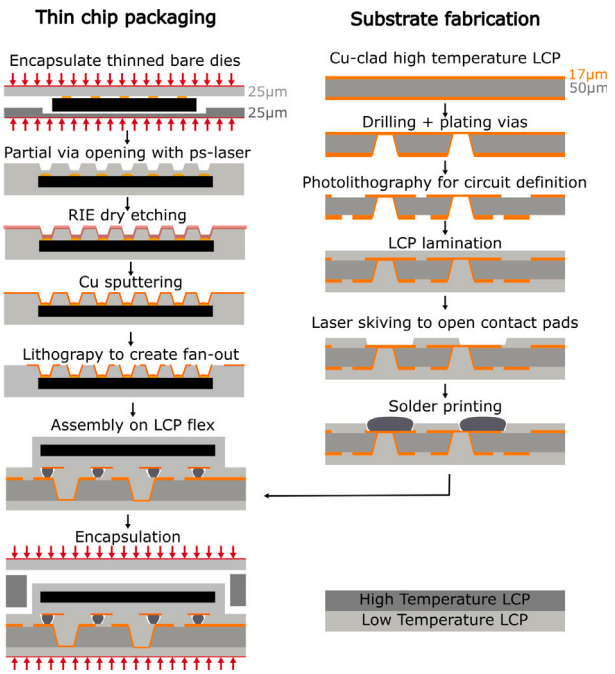


Fig. 1. The fabrication flow for ultrathin LCP-based chip packages as well as for fabrication of flexible LCP PCB's used for assembly of the thin chip packages and the proposed final encapsulation step.

stability in demanding physiological environments [24–26]. Other research groups have similarly explored LCP-based electrode fabrication and neural interfaces [27,28] and more recently including microchannels [29] and in combination with graphene films as conductive layers [30]. However, most reported LCP-based implantable packaging concepts rely on high-temperature bonding of thermoformed lids [16,31–34] or custom flexible silicon electronics [35].

In contrast, this work investigates a manufacturing process for embedding commercially fabricated ultrathin bare dies directly into an all-LCP substrate, followed by via formation, fan-out metallisation to produce assembly-ready chip packages which can assembled and further encapsulated.

To achieve this goal, several technical challenges must be addressed. First, embedding thinned dies in LCP requires precise control over cavity geometry to ensure mechanical stability while avoiding die damage during processing and lamination, a challenge considering the high processing temperatures and narrow lamination process window of LCP materials. Second, reliable electrical connection to the embedded ICs requires high-quality vias with tight dimensional tolerances. Conventional laser drilling approaches are either insufficiently precise or risk damaging thin bond-pad metallisation, motivating the use of a more controlled via-opening strategy. Finally, these steps must be integrated into a fully LCP-based process flow that supports metallisation, assembly onto flexible substrates, and final encapsulation without inducing misalignment, defects, or deformation caused by polymer flow at elevated temperatures.

2. Fabrication method

A major advantage of LCP is that it can obtained in a high-temperature (HT) and low-temperature (LT) variant, differing only slightly in chemical composition. This allows use of the HT-material as the substrate and the LT material as the bonding layer, resulting in a homogeneous package. In this work, Rogers LCP was used as the primary material for process development and optimisation as it was available throughout the project. Since Rogers LCP is no longer in production, Dycoplast LCP represents a relevant alternative for future implementation. Preliminary experiments were conducted on Dycoplast LCP (LT and HT material provided by Dyconex) to assess transferability of selected process steps, although full optimisation for this material is outside the scope of the present study. Therefore, unless stated otherwise, all fabrication experiments were performed using Rogers high- and low-temperature LCP materials (Rogers Ultralam 3850HT and 3908). The properties of the used materials are summarised in Table 1.

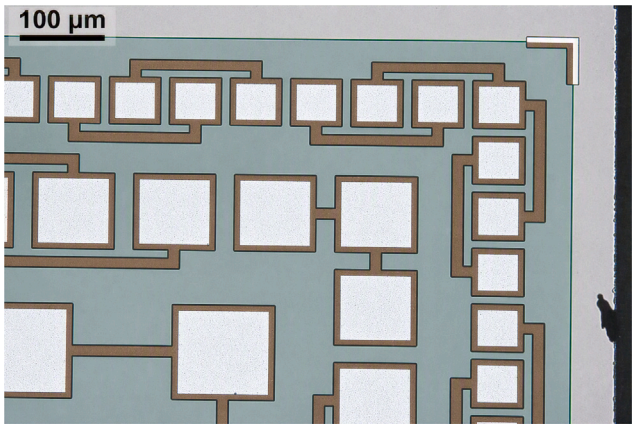


Fig. 2. Image of the PTCE daisy-chain test structures used for via integrity evaluation.

Fig. 1 provides an overview of the fabrication flow. Bare dies are embedded in high-temperature LCP using laser-skived cavities and encapsulated via vacuum lamination with low-temperature LCP. Electrical connection is obtained through vias opened using a hybrid laser-RIE process, followed by TiW/Cu metallisation and lithographic patterning. The resulting thin chip packages are subsequently assembled onto flexible (LCP) substrates and can be fully encapsulated using additional LCP lamination steps. The flexible substrates are either polyimide or LCP flexible PCB's. For both materials, the base material is a Cu-cladded sheet which is patterned using lithography and etching. For the polyimide substrates, a laser-cut solder mask is laminated on the substrate. For the LCP substrates, a layer of LT LCP is laminated on top, which was opened up using laser skiving. Both substrates were treated with an OSP surface finish prior to assembly.

Two types of IC will be used: (1) an MSP430-microcontroller (MSP430F1611, Texas Instruments) and (2) a custom made test chip with patterns to allow daisy chain testing of vias (Fig. 2) named PTCE (made and designed by imec, Leuven, Belgium). The PTCE dies contain bond pads with size 40 × 40, 70 × 70 and 90 × 90 µm^2 with pitch of 60, 100 and 200 µm respectively. Both types of ICs were supplied on pre-thinned wafers with a thickness of 30 µm. The MSP430-microcontrollers already had a thin NiAu bumping while the PTCE dies did not, providing a small difference between the types of die in terms of via pad metallisation.

2.1. Laser skiving of cavities

For chip encapsulation in LCP, various layer build-ups are possible, as discussed in Section 2.2. A promising configuration consists of high-temperature LCP with a shallow cavity as this enables fabrication of ultrathin devices while preserving the mechanical stability of the substrate. These cavities were fabricatedthrough a laser-skiving process using parallel scan lines, originally using a 532 nm picosecond YAG-laser (3d MicroMac). However, the process required approximately 80 min to fabricate four cavities. A 355 nm laser source was subsequently adopted, reducing the fabrication time to approximately 12 min as polymers have increased absorption in the UV-range [36].

Table 1
Properties of low temperature (LT) and high temperature (HT) LCP materials from Rogers and Dycoplast including melting temperatures and coefficient of thermal expansion (CTE).

	Rogers 3908 LT LCP	Rogers 3850HT HT LCP	Dycoplast LT LT LCP	Dycoplast HT HT LCP
Melting temperature (°C)	280	310	280	310
CTE x/y (ppm/°C)	17	18	18	15
CTE z (ppm/°C)	–	200	–	–

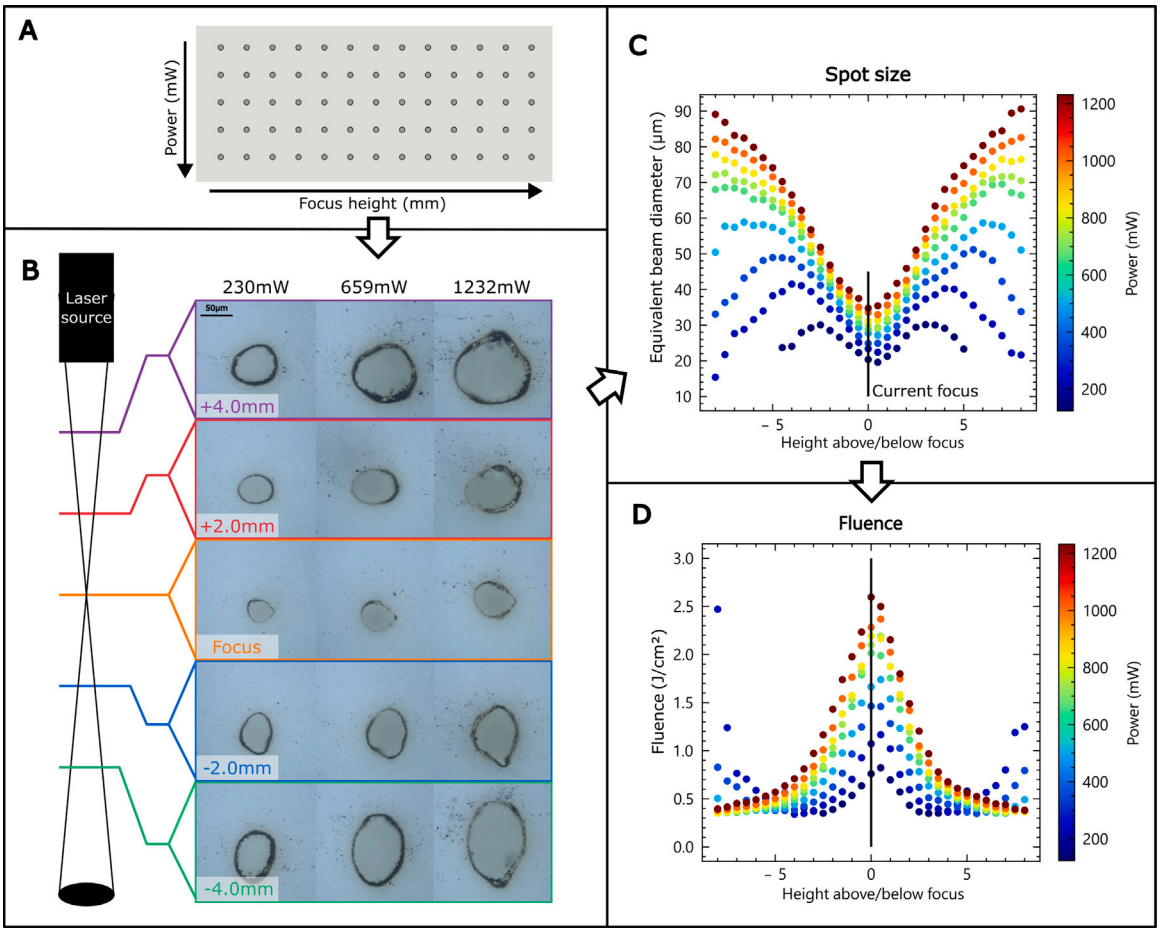


Fig. 3. Influence of laser power and focal position on spot size and fluence during static pulse ablation on high-temperature LCP. **A.** Parameter sweep varying focus height and attenuation. **B.** Images of spot size for varying focus height for 3 power values. **C.** Spot size measurements. **D.** Fluence calculations.

As a relatively large volume of material must be removed, an efficiency study was performed, based on the approach described by Zemaitis et al. [37]. The laser attenuation (and thus output power) and focal position along the z-axis were varied for two cases: (1) dynamic ablation of square 1 ×1 mm^2 cavities and (2) static ablation using 100-pulse bursts. The pulse repetition frequency and scan speed were kept constant at 50 kHz and 300 mm/s. The scanline pitch was fixed at 6 µm to ensure consistent inter-pulse distance on the horizontal and vertical axis. At this repetition rate, individual pulses can be treated as quasi-independent, allowing the influence of inter-pulse effects such as heating to be neglected.

Spot size was determined by manually outlining the ablated areas of the 100-pulse bursts in ImageJ and is shown in Fig. 3B–C. These values were combined with the output power to calculate the corresponding fluence using Eq. (1), where r_0 denotes the spot radius, f_p the pulse repetition frequency, and P the laser output power (Fig. 3D).

$$Fluence[\mathrm{J/cm^2}] = \frac{P[\mathrm{mW}] * 10^{-3}}{\pi(r_0[\mathrm{cm}]^2)} \cdot \frac{1}{f_p[\mathrm{Hz}]} \quad (1)$$

Cavity and burst depths were measured using an optical profiler (Veeco WYKO NT3300). For static pulse bursts, the ablated volume was estimated assuming a Gaussian ablation profile via Eq. (2) using the spot size and the ablated depth d. For dynamic cavity ablation, the depth was used as a proxy for ablated volume since this conversion is linear.

$$Burst\ volume[\mu\mathrm{m}^3] = 2 \cdot \pi \cdot d[\mu\mathrm{m}] \cdot (r_0[\mu\mathrm{m}]/2)^2 \quad (2)$$

For both static and dynamic ablation regimes, an increase in ablated volume was observed under defocused conditions, as shown in Fig. 4E–F. This effect became more pronounced at higher laser powers and resulted in increase in ablation efficiency up to threefold. The increased ablation volume under defocus can be attributed to the larger effective beam diameter combined with a reduction in fluence. Approximating the threshold fluence by increasing the spot size promotes material removal by avoiding excessive local heating.

At higher laser powers and extreme defocus positions, cavity homogeneity deteriorated and local melting effects were observed as the fluence approached the empirically determined ablation threshold

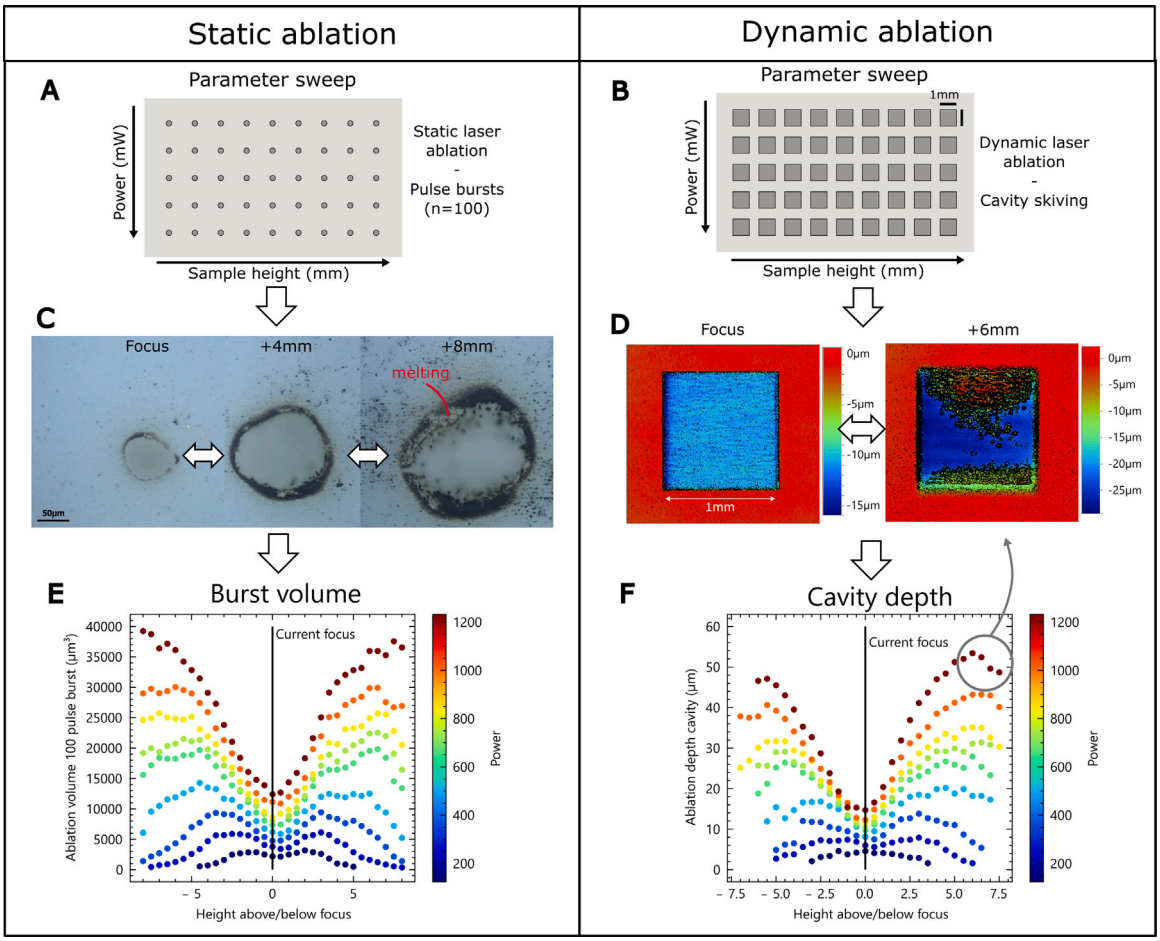


Fig. 4. Effect of focal offset and laser power on ablated volume for static pulse bursts and dynamic cavity ablation in high-temperature LCP. **A.** Parameter sweep for static ablation (bursts of 100 pulses). **B.** Parameter sweep for dynamic cavity ablation (size 1 × 1 mm^2). **C. D.** Optical profilometry in-focus and out-of-focus showing melting effect. Images of resulting craters with melting far out-of-focus. **E.** Measured burst volume. **F.** Measured cavity depth.

of approximately 0.35 J/cm^2 as shown in Fig. 4C–D. These melting phenomena occurred in an inhomogeneous manner, likely due to minor local variations caused by acceleration effects in beam steering and sample heating.

Based on this parameter study and a target ablation depth of approximately 20 µm, a laser power of 250 mW combined with a +2 mm defocus was selected, which further reduced processing time to 5 min for four cavities. This configuration provided sufficient ablation efficiency while producing cavities suitable for subsequent die embedding and lamination.

2.2. Lamination

One of the main advantages of using LCP is that it can serve as both substrate and bonding material through the combination of high-temperature (HT) and low-temperature (LT) variants. This enables fabrication of a homogeneously encapsulated structure, minimising interface-related issues such as poor adhesion or coefficient of thermal expansion (CTE) mismatch.

LCP bonding introduces challenges due to the high melting temperatures of LCP (290 °C and 330 °C for LT and HT variants, respectively), the limited difference in flow temperature between the two materials and the low viscosity of the molten LCP.

Bonding was performed via lamination using a vacuum lamination press (HML-30, Haseneder Maschinenbau). As this equipment is primarily designed for large-area substrates processed at lower temperatures, adaptations were required for the small-area samples used in this work (5 ×5 cm^2). A modified lamination stack-up was implemented to ensure homogeneous pressure distribution, consisting of thermally stable press pads (Fiberfrax, Insulcon) and release foils (Thermofilm, Pacothane) (Fig. 5A). This stack provided homogeneous pressure across the lamination area but high pressures were observed on the sample edges as verified using pressure-sensitive films (FUJIFilm Prescale 4LW) (Fig. 5B–C). Therefore, the stack-up was supplemented with stainless steel and/or polyimide spacers to fill the unused press area to ensure homogeneous pressure across each sample, as shown in Fig. 5D–E.

To identify suitable lamination processing windows, a series of polymer flow tests was performed based on IPC-TM-650 method 2.3.17.1b as shown in Fig. 5F. Various combinations of peak temperature and applied pressure were evaluated, using lamination cycles consisting of gradual heating over 60 min starting at 50 °C, a 30 min dwell at peak temperature, and gradual cooling over 60 min to 50 °C. A constant pressure and mild vacuum conditions (10 mbar) were maintained throughout the cycle. These tests aimed to find lamination setpoints with sufficient LT-LCP flow while minimising deformation of HT-LCP features by avoiding flow of the HT-LCP material.

Table 2 shows representative flow temperatures for the Rogers and Dycoplast HT and LT-materials. These values are indicative as they are highly dependent on the stack-up and lamination press. Two observations can be made: firstly, the effective flow temperature of both LT and HT-LCP decreases with increasing pressure. Second, the practical difference between the flow temperatures of LT and HT-LCP was approximately 10 °C rather than the nominal 30 °C, highlighting the need for precise process control. The Dycoplast material must be

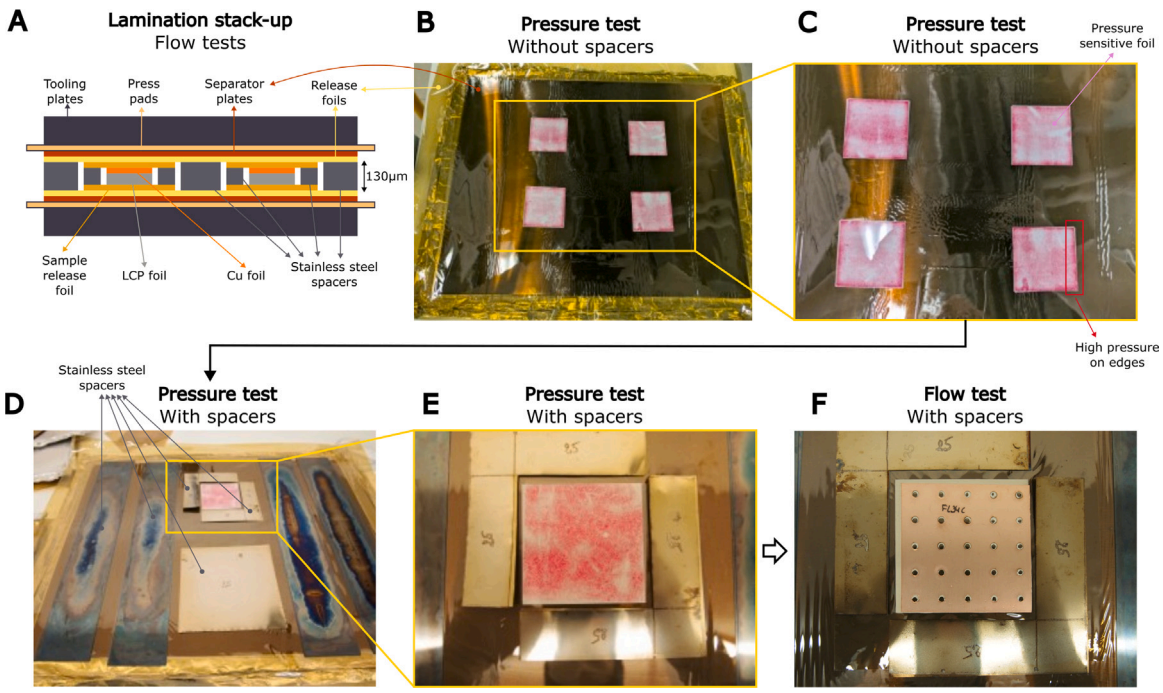


Fig. 5. Lamination configuration. **A.** Schematic of lamination stack-up **B.** Sample pressure evaluated using pressure-sensitive foils in the proposed stack-up **C.** Close-up image showing increased edge pressure. **D.** Stack-up modification to include spacers. **E.** Close-up of resulting homogeneous pressure distribution across sample **F.** LCP flow test in the modified configuration.

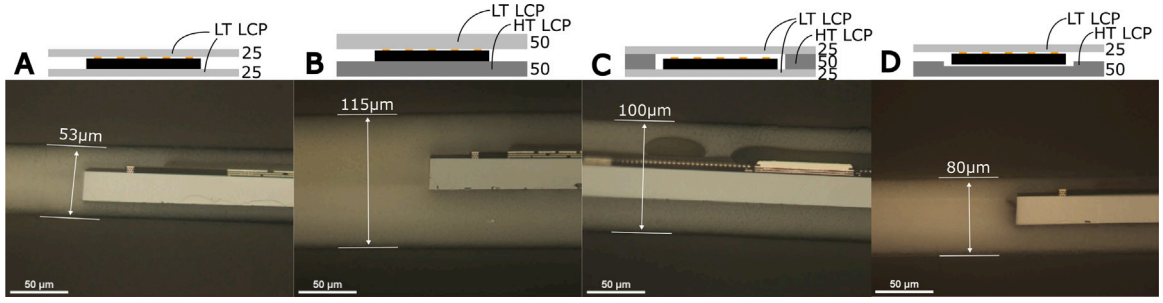


Fig. 6. Cross-sectional images of selected LCP build-ups. **A.** LT-LCP only **B.** HT- + LT-LCP **C.** HT-LCP with laser-cut cavities plus two LT-LCP layers **D.** Skived HT-LCP with LT-LCP.

Table 2
Representative flow temperatures for Rogers and Dycoplast LT and HT materials.

	Rogers		Dycoplast	
	LT	HT	LT	HT
1 bar	310 °C	320 °C	295 °C	305 °C
5 bar	300 °C	310 °C		
20 bar	280 °C	290 °C		

processed at lower temperatures and a similar small processing window can be observed.

LCP lamination can be performed either between the flow temperatures of the LT and HT materials or above the HT-LCP flow temperature. While lamination above the HT-LCP flow temperature is expected to improve interlayer fusion and thus bonding quality, it may also induce deformation of patterned metallisation on the HT-LCP substrates. For chip encapsulation, this deformation is less critical and higher lamination temperatures may be preferential to reduce the risk of void formation. In contrast, substrate fabrication for subsequent assembly requires lamination below the HT-LCP flow temperature to preserve integrity of the circuit layer.

For chip encapsulation, several LCP build-ups were evaluated using a 25 µm LT-LCP covering layer as summarised below. Dies were manually placed in the cavities with the aid of an optical microscope and tweezers without the use of any adhesives. The cavity dimension was set at the size of the die +500 µm both horizontally and vertically. After encapsulation, cross-sections were made to evaluate encapsulation quality as seen in Fig. 6

A. **LT-LCP only:** yielded thin packages but exhibited warpage.

B. **HT- plus LT-LCP:** resulted in thicker packages and increased risk of die fracture due to direct pressure application on the die.

C. **HT-LCP with laser-cut cavities plus two LT-LCP layers:** voids formed when using 50 µm HT-LCP due to excessive cavity height; reducing HT-LCP thickness to 25 µm mitigated this issue but introduced die displacement during lamination preparation due to the dies 'slipping' underneath the laser-cut foil.

D. **Skived HT-LCP with LT-LCP:** enabled ultrathin packages with improved mechanical stability.

Build-ups C-D emerged as the most promising. Build-up D enabled fabrication of ultrathin packages down to approximately 50 µm total thickness, while build-up C offered a simplified process flow by eliminating the laser-skiving step but at the cost of lower yield due to die breakage.

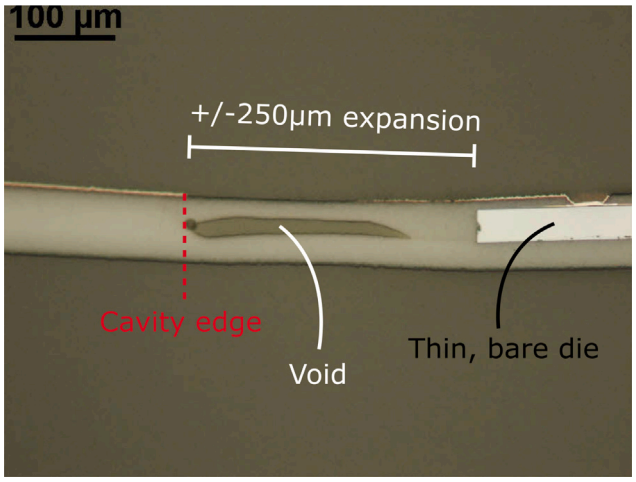


Fig. 7. Image showing void formation next to the embedded die, attributed to excessive cavity-to-die clearance during lamination.

The influence of lamination conditions on void formation was further evaluated using the flow temperatures in Table 2. Contrary to expectations, no consistent reduction in void occurrence was observed at higher lamination temperatures or pressures as voids remained present around the dies. An example of a typical void can be seen in Fig. 7. This suggests that cavity geometry plays an important role in addition to the lamination condition: increased clearance around the die locally reduces pressure during lamination, thereby locally limiting polymer flow and thus increasing the risk of void formation.

The resulting LCP encapsulation layer above the embedded die was approximately 15 µm thick and remained sufficiently transparent to facilitate optical alignment of subsequent processing steps. The final chip package is approximately 53 µm thick as confirmed by measurements on cross-sections.

2.3. Via fabrication

Several approaches for fabricating via openings through the LCP encapsulation were considered. Direct picosecond-laser drilling offers high spatial resolution but carries a significant risk of damaging the aluminium bond pads of the PTCE dies and the ultrathin gold finishes present on the MSP430 dies. Hard-mask-based plasma etching, as employed in the UTCP process, enables precise via definition but significantly adds complexity due to the additional deposition, lithography, and mask-removal steps required [7]. CO_2-laser ablation provides polymer selectivity but lacks the spatial resolution needed for the pad dimensions considered in this work.

A hybrid approach combining partial laser ablation with a 355 nm picosecond YAG-laser followed by Reactive Ion Etching (RIE) was therefore selected. This method is feasible due to the relatively thick LCP encapsulation layer (approximately 15 µm) covering the contact pads, which provides sufficient margin to avoid damage to the underlying metallisation during laser processing. With thinner encapsulation layers, this margin would be significantly reduced, making the process increasingly sensitive to thickness variations across the die.

The laser was used to partially ablate the via openings to a depth of approximately 12 µm using a square scan pattern. Subsequently, RIE (CHF3-5sccm + O2-20sccm, 150 W, 100mTorr) was applied to remove the remaining LCP and fully clear the vias with an etch rate of approximately 0.8 µm/min. Total etch times varied between 20 to 30 min depending on via clearance, which was verified by optical inspection. As no hard mask was employed, the entire surface was etched, which had the added effect of surface roughening, improving adhesion of the subsequently deposited metallisation as verified in Section 2.5.

For the PTCE dies, NiAu bumping was performed to provide a conductive, non-oxidising surface finish. In some samples, step plating was observed around the edges of the bondpads, especially for the smaller contact pads (40 × 40 µm^2) as seen in Fig. 8A.3. This can be attributed to catalyst poisoning as the stabiliser diffuses to the pads where the concentration becomes too high and the plating is locally halted [38,39]. This effect did not impair electrical performance in the finalised samples.

2.4. Metallisation and lithography

Metallisation was performed by sputtering a 1 µm Cu layer, preceded by a 25 nm TiW adhesion layer. Copper was selected to simplify the lithography and etching processes compared to biocompatible, noble metals such as Au and Ti which require alternate, more complicated lithography strategies such as lift-off and/or more agressive etchants. Biocompatible metallisation strategies such as Ti or Au have been proven to be compatible with LCP by a.o. Dyconex so this does not affect the proof-of-concept of the proposed packaging process [24,27]. During lithography, sufficient sample flatness is critical for reliable, high resolution lithography. Therefore, the samples are temporarily bonded to a 1" glass carrier using double-sided heat release tape (Revalpha RA95H(N), release temperature 160 °C) using a hot-roll laminator (Cheminstruments). The bonding strength of the heat release tape was sufficient to mitigate sample warpage after lamination.

For lithography, alignment was performed using laser-written crosses which were created during opening of the vias so is aligned perfectly with the vias and matches with corresponding crosses on the glass mask. The photoresist AZ4562 was spincoated on the sample, followed by a soft bake. Samples were illuminated with an exposure energy of 350 mJ/cm^2 (EVG 620) using a glass mask followed by development (Microposit developer with a 1:1 dilution) and a thorough rinse before a final hard bake. Etching was done using Mecbrite CA-92 for the Cu layer and H2O2 for the TiW layer. The resist was stripped using a sequence of acetone and an acetone/IPA solution followed by thorough rinsing.

Representative patterned samples are shown in Fig. 8B–C for both PTCE and MSP430 dies. For the PTCE dies, the metallisation pattern consisted of daisy-chain interconnects with additional contact pads, enabling measurement of sections of the daisy chains. For the MSP430 microcontrollers, a fan-out was implemented towards pads with dimensions of 150 × 150 µm^2 and a pitch of 600 µm. The design additionally included footprints for passive components required for standalone operation during functional testing. A set of seven contact pads for pogo-pins was provided to enable programming of the encapsulated microcontrollers using a custom PCB in combination with an EZ-FET debugging probe (Texas Instruments).

2.5. Mechanical testing

LCP-LCP adhesion. LCP–LCP adhesion was evaluated using peel tests on laminated samples representative of the chip encapsulation stack-up. Samples were fabricated by laminating 25 µm LT-LCP onto 50 µm HT-LCP at lamination conditions where only the LT-LCP was expected to flow. Polyimide foils were incorporated to create free "tails" suitable for mechanical clamping during testing.

Peel tests were performed according to ASTM D1876 (T-peel test for flexible substrates) on samples with a width of 1.5 cm and a pulling speed of 25 mm/min (Fig. 9A). For samples based on Rogers LCP material, an average peel force of approximately 3.0 N/cm was measured, whereas samples using Dycoplast material exhibited an average peel force of approximately 2.3 N/cm (Fig. 9B). These values represent baseline adhesion without dedicated surface pretreatment and should be considered as a reference point for future experiments due to the

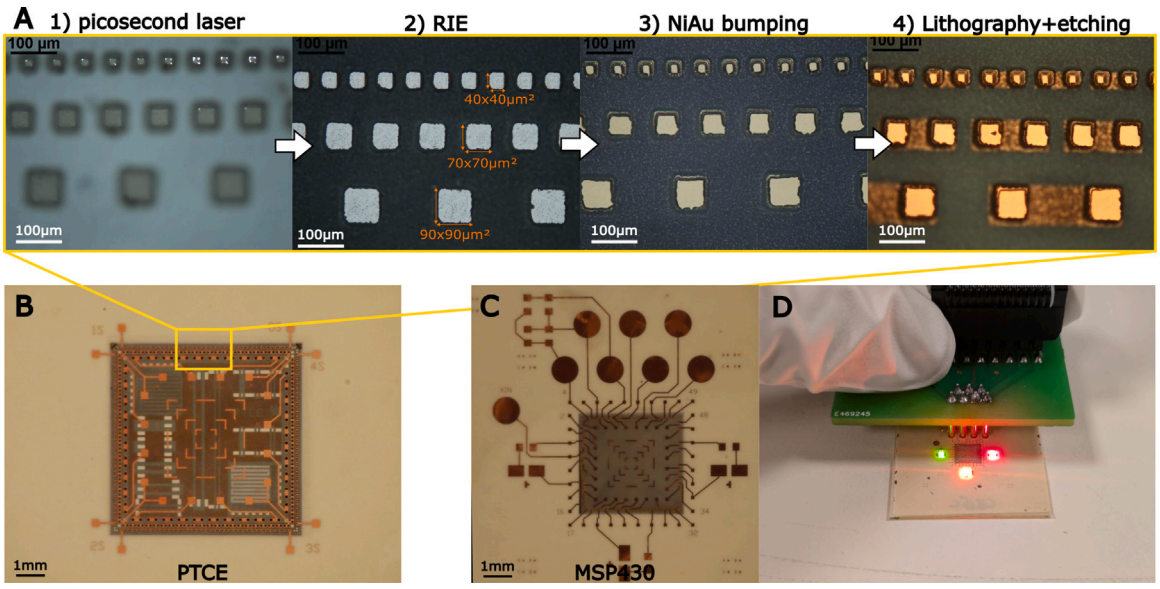


Fig. 8. **A.** Key fabrication steps for ultrathin LCP chip packages: (1) partial via opening by laser ablation, (2) RIE-cleared vias, (3) NiAu-plated contact pads with some step plating observed, and (4) patterned metallisation. **B.** Image of final PTCE pattern. **C.** Image of final MSP430 pattern. **D.** Picture of functional MSP430 demonstrator with assembled LED's, resistors and capacitors.

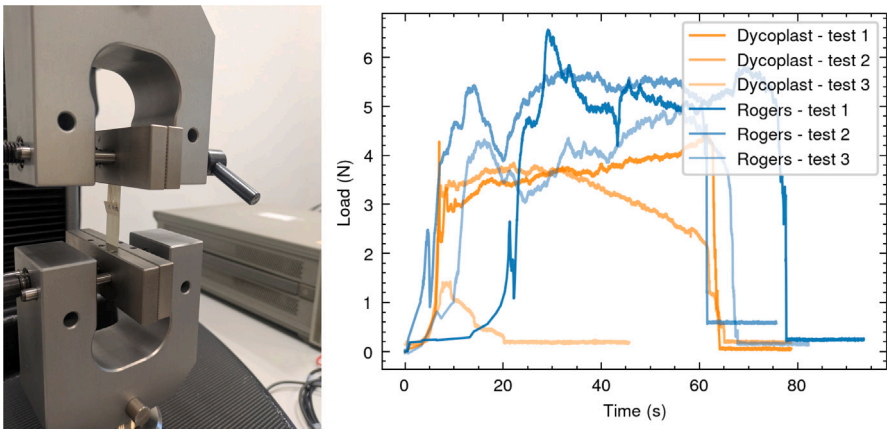


Fig. 9. **A.** Set-up for LCP-LCP peel test **B.** Force applied during LCP-LCP peel test for Rogers and Dycoplast materials.

limited sample size and high sample variability. The variability can be partially explained by material tears during the peel test, which was most egregious in sample 3 of the Dycoplast material. The higher adhesion observed for the Rogers material can be attributed to the increased surface roughness resulting from its original Cu cladding, which was removed by wet etching prior to processing.

LCP–LCP adhesion could be further improved by applying surface activation steps, such as plasma pretreatment of the HT-LCP prior to bonding, as suggested by material datasheets. Additionally, briefly increasing the lamination temperature above the HT-LCP flow temperature is expected to enhance interlayer fusion, though this must be carefully balanced against the risk of substrate deformation.

LCP-Cu adhesion. LCP–Cu adhesion was assessed using laminated samples consisting of 50 µm Rogers HT-LCP and 25 µm LT-LCP, processed identically to the chip encapsulation samples, including RIE exposure and metallisation. Tape tests were performed according to ASTM D3359 using a 90° peeling angle for tape removal.

In regions not exposed to RIE, partial removal of the Cu layer was observed after the initial tape test, indicating marginal to poor adhesion. By contrast, in areas subjected to RIE prior to metallisation, the initial tape test primarily removed a thin Cu oxide surface layer, while subsequent peel cycles resulted in little to no further delamination, and the remaining Cu layer stayed intact as shown in Fig. 10.



Fig. 10. LCP-substrate after LCP-Cu tape test. Left side was subjected to RIE while the right side was not.

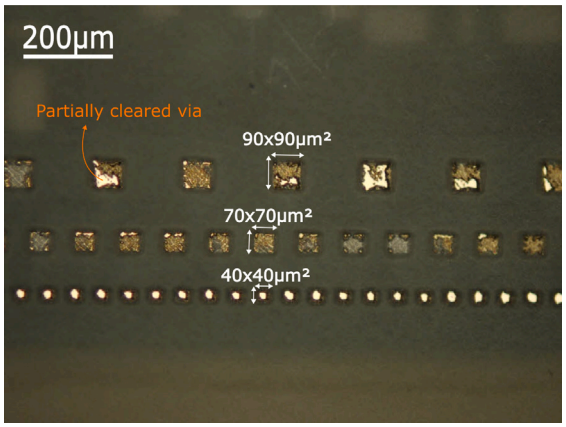


Fig. 11. Example of insufficient RIE clearance resulting in LCP residues on the contact pads, which was identified as the root cause for electrical failure of the vias.

Table 3
Average and standard deviation of via chain resistance for PTCE die (n = 19).

Pad size	Pitch	Nr vias	R avg	R std
40 × 40 µm²	60 µm	362	88.9 Ω	1.4 Ω
70 × 70 µm²	100 µm	175	74.8 Ω	1.4 Ω
90 × 90 µm²	200 µm	79	66.7 Ω	1.0 Ω

This behaviour indicates that the surface roughening induced by the RIE process significantly enhances LCP–Cu adhesion up to an excellent level.

2.6. Functional testing

Via validation using PTCE structures. Via integrity was first evaluated using the PTCE daisy-chain test structures, allowing isolation of via performance from active IC functionality. Six samples, each containing four PTCE dies (n = 24), were fabricated for this validation run. Of these, five embedded dies were excluded from electrical testing due to insufficient RIE clearance as shown in Fig. 11, which was identified during post-processing optical inspection and would have been avoidable with additional in-process verification.

The remaining samples were electrically characterised using a probe station by measuring the resistance of the full daisy-chain structures and the resulting resistance values are summarised in Table 3. Across a total of 11.704 evaluated vias, all tested daisy chains exhibited electrical continuity. The measured resistance was dominated by the metallic interconnects, indicating that the contribution of the vias themselves was negligible and confirming reliable via fabrication over all pad sizes evaluated.

Via validation and programmability of MSP430 microcontrollers. Via integrity and functional performance were further assessed using the embedded MSP430 microcontrollers. Four samples were fabricated, each containing four encapsulated dies (n = 16), with each die featuring 64 bond pads, resulting in 1.024 vias evaluated in total.

Via integrity screening was performed using ESD diode measurements relative to the AVSS pin. All pads exhibited the expected diode behaviour, confirming electrical connectivity to the on-chip protection structures. While this test verifies pad-level electrical connection, it does not assess full IC functionality.

Functional integrity was therefore evaluated through programmability testing using an EZ-FET debugging probe. Out of the 16 encapsulated microcontrollers, 10 could be successfully programmed, corresponding to a yield of 62.5%. This reduction relative to the ESD screening yield indicates that, although electrical connection to the pads and IC protective structures was maintained, some damage is present resulting in devices that were no longer fully functional after processing. The exact failure mechanism could not be conclusively identified. Micro-fracturing of the thinned dies during processing is considered a plausible cause, but was not verified in this work. The dies were not functionally verified prior to encapsulation so damage to the dies prior to processing cannot be excluded.

2.7. Assembly

After chip packaging, two assembly and encapsulation strategies were considered, as illustrated in Fig. 12.

In the first strategy, passive components are assembled directly onto the patterned metallisation of the encapsulated chip using solder paste, followed by encapsulation through additional LCP lamination. While this approach is relatively simple, it currently limits integration to a single embedded die, as lithography alignment is performed relative to the die position. Furthermore, restriction to a single conductive layer and the absence of a solder mask limit circuit complexity and increase the risk of solder-related defects. As a result, this strategy was used only for preliminary demonstrators. For this demonstrator, solder paste (Interflux DP5505, type 3) was manually dispensed, followed by manual component placement and reflow soldering in a reflow oven (IBL SLC 300). Functional demonstrator circuits containing LEDs, resistors, and capacitors were successfully assembled using this method (Fig. 8D).

In the second strategy, the thin LCP chip packages were cut out using a picosecond laser, released from the carrier using a hotplate and assembled onto a flexible substrate alongside the required passive components, followed by full encapsulation. This approach enables individual alignment and placement of multiple chip packages as well as integration of passive components and was therefore identified as the most promising route towards scalable system integration. Challenges remain in avoiding reflow of previously placed components during subsequent assembly steps, which may be addressed in future work through localised heating, underfill application, or the use of transient liquid phase sintering (TLPS) materials.

Assembly substrates were fabricated using either polyimide or LCP, each with a single conductive layer for these initial demonstrators although the process is compatible with double-sided substrates. Copper-clad substrates were patterned using established lithography and etching flows for double-sided flexible substrates. The substrates were micro-etched using Circuposit etch 3330 in an automated micro-etching and degreasing line (PILL). Riston FX920 film resist was laminated to using a dry film laminator (MEGA-electronics). The resist was exposed using a foil mask in a large area UV exposure machine (Bungard) with an intensity of 40 mJ/cm^2. The substrates were developed using sodium carbonate (0.8 wt%) in an automated development line (PILL). Etching was performed in a semi-automated Bungard spray etching line using a CuCl/HCl mixture as etchant. Substrates were rinsed and resist was manually stripped using NaOH. Polyimide substrates were provided with a laser-cut solder mask (ShengYi SF305C 0525) via vacuum lamination. LCP substrates were coated with a 25 µm LT-LCP layer laminated below the HT-LCP flow temperature. Solder mask openings in the LCP substrates were formed by laser skiving, followed by a brief RIE step to remove polymer residues and ensure good solder wetting. An organic solderability preservative (OSP) finish was applied to both substrate types prior to assembly using Mecbrite CA-92 for a micro-etch and Mecseal CL-5018 for the finish itself.

Solder paste (LMPA Q6, type 5) was stencil-printed using a 50 µm laser-cut stainless-steel stencil. Thin LCP chip packages were aligned and placed using a Finetech pick-and-place system. During placement, a contact force of 5 N was maintained while the substrate was heated to 250 °C for 90 s to reflow the solder (see Fig. 13). The placement tool was released only after cooling to ensure positional stability during solidification.

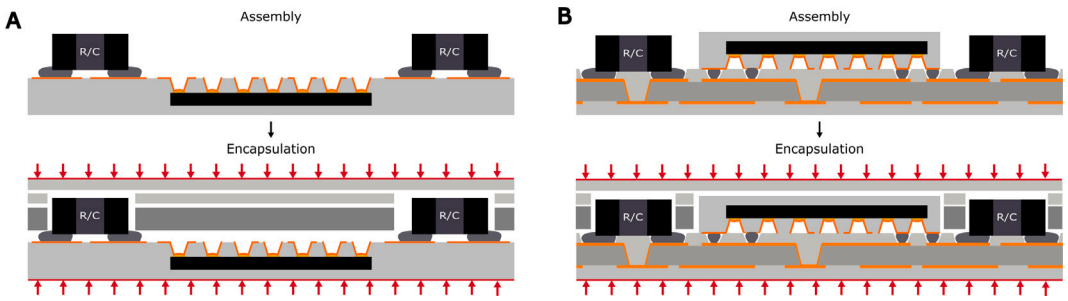


Fig. 12. Schematic overview of two encapsulation strategies: **A.** direct component assembly on embedded dies and **B.** assembly of thin chip packages and passive components followed by full encapsulation.

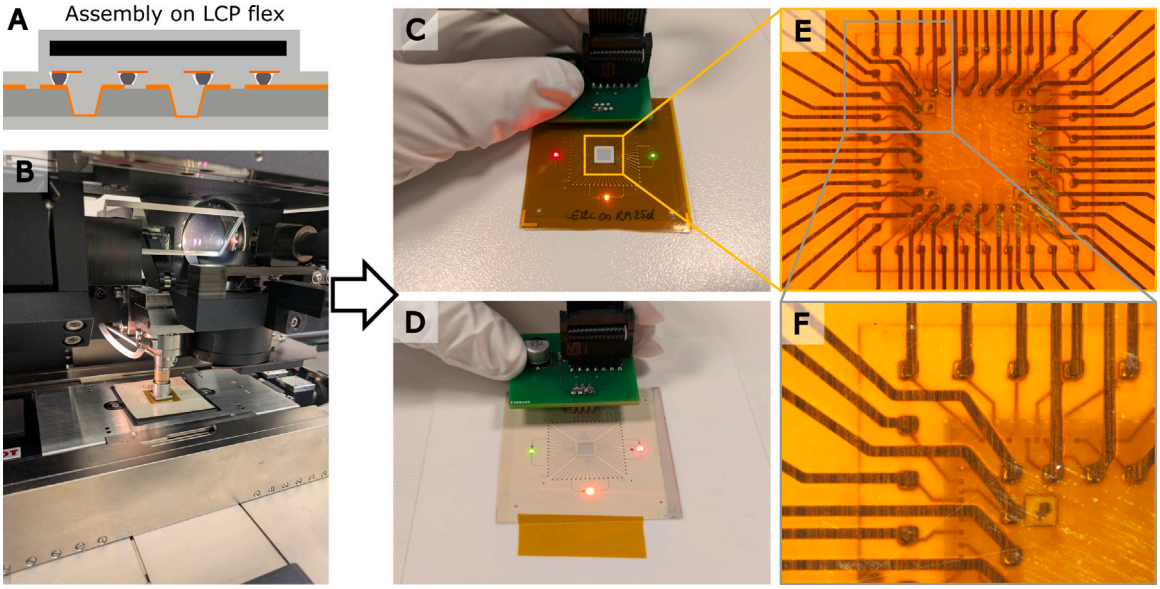


Fig. 13. Assembly of ultrathin LCP chip packages on flexible substrates (flexible PCB's based on polyimide or LCP patterned foils). **A.** Schematic illustration of process **B.** Picture of Finetech tool during assembly **C.** Assembled LCP thin chip package on polyimide substrate **D.** Assembled LCP thin chip package on LCP substrate **E.** Image of backside of assembled thin chip package on polyimide, visualising the Cu structures on the substrate and the thin chip package **F.** Detailed image of corner of assembled thin chip package on polyimide substrate.

Assembly results. For the PTCE chip packages, a substrate-level fan-out connected to the 24 measurement pads on each chip package (200 × 200 μm^2, minimum pitch 750 μm) was provided. This allowed verification of the functionality via measurement of the via chain resistance using the substrate-level fan-out. Four chip packages were assembled on LCP substrates, of which two were assembled without defects. In the remaining two samples, a total of three contact pads failed to connect successfully, resulting in an overall pad-level yield of 96.8%.

Similarly, MSP430 chip packages were assembled using the fan-out defined on the chip package itself. Of eight assembled samples on LCP substrates, five were assembled without defects and all 64 pads were verified using ESD protection measurements. Among the remaining three samples, one sample was initially poorly assembled for reasons that could not be conclusively determined and the two others had 2 unconnected pads each. After repeating the assembly process, 51 out of 64 pads were successfully contacted. Overall, excluding the initially misassembled sample, 444 out of 448 pads were successfully connected, corresponding to a pad-level yield of 99.1%. Including the misassembled sample, the yield drops to 96.7%. Following assembly, six out of eight microcontrollers remained programmable, resulting in a functional yield of 75%.

The misassembled samples, both for the PTCE and MSP430 dies, indicates a fragility with the current approach, possibly partially due to the lack of mechanical support which could be mitigated via the use of underfill.

2.8. Encapsulation

Two PTCE samples were fully encapsulated as shown in Fig. 12B. Following encapsulation, the contact pads were reopened using a picosecond laser. Electrical measurements were then repeated and compared to the results obtained prior to encapsulation. Out of 48 evaluated pads across both samples, 27 exhibited electrical characteristics consistent with pre-encapsulation measurements, corresponding to a post-encapsulation yield of 47.9%.

The observed reduction in connectivity indicates that all lamination steps remain critical and yield-limiting. While the results confirm the feasibility of fully encapsulating LCP-embedded chip packages, they also highlight the sensitivity of the current process flow to lamination-induced effects such as die displacement, void formation, or deformation of thin metallisation layers. These aspects are further discussed in Section 3.

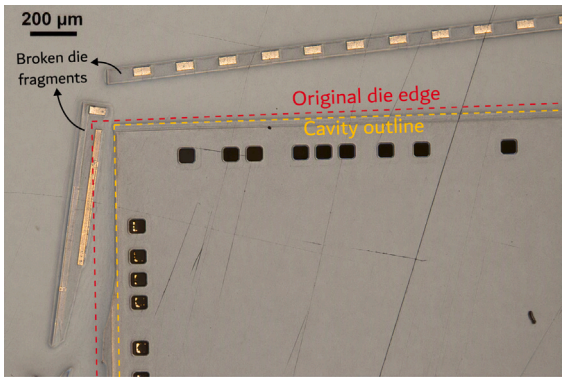


Fig. 14. Optical image of a fractured MSP430 die after lamination.

3. Discussion

The work presented here demonstrates the feasibility of fabricating ultrathin, fully LCP-based chip packages suitable for integration into flexible electronic systems. While the overall process flow from cavity formation to lamination, via opening, metallisation, assembly and encapsulation proved functional, several aspects of the process can be further investigated to improve yield, reliability and manufacturability.

3.1. Observations

Die embedding. The use of laser-skived cavities enabled embedding of thinned dies with good mechanical stability. However, voids were observed in several samples, indicating imperfect flow during lamination, likely attributed to the relatively large margin between the cavity outline and die size. This should be further investigated by varying the lamination conditions and cavity margins, including cross-sections and X-ray inspection for non-destructive analysis post-lamination.

Reducing the cavity clearance is expected to improve encapsulation uniformity but will also increase the risk of the dies "escaping" the cavity leading to component breakage as seen in Fig. 14. A mitigation could be implemented by using a curable glue/underfill during placement. An added advantage is that it would allow multi-IC placement and alignment, allowing lithography to be performed on multiple samples simultaneously. However, the impact of the glue/underfill on the lamination results is currently hard to predict due to the high lamination temperatures as there may be a mismatch between rigid, cured underfill and the flowing LCP so this step must be carefully investigated when implemented.

Lamination control. The use of both high-temperature (HT) and low-temperature (LT) LCP types allows fabrication of homogeneous multilayer structures but the small difference in flow temperatures makes precise control essential. The current lamination setup was adapted from equipment primarily intended for large substrates rather than small samples, requiring stack-up modifications to achieve uniform pressure distribution. Despite these efforts, inconsistencies in lamination results and flow could still be observed across samples. Improved temperature and pressure control could be achieved by using a dedicated tool with improved control and smaller processing area. Besides flow behaviour, LCP-LCP adhesion could (and should) be further improved by surface treatments such as plasma activation of (LT/)HT-LCP prior to bonding using the current results as a baseline.

Via fabrication. In terms of via fabrication, the hybrid laser-plus-RIE approach yielded reliable and damage-free openings. The high via yield observed on both PTCE and MSP430 devices confirms the robustness of this method, as indicated by the near perfect yield of via fabrication. Importantly, the hybrid approach provides robustness against thickness variations in the encapsulating LCP layer, which would be difficult to accommodate using purely laser-based approaches.

Assembly. The assembly process demonstrated high soldering yields but also revealed specific limitations. Heating the entire substrate during each chip placement introduces thermal cycling that may affect previously soldered joints. A local-heating assembly approach, or the use of underfill materials with suitable processing conditions, could mitigate this risk. Another limitation was the use of an OSP finish on the assembly substrates as this type of finish degrades at temperatures above 160 °C as used during the assembly process which was performed at 250 °C. This degradation was visible as a discolouration on the Cu structures. Ideally, an ENIG finish would be used though this was omitted in the current work for simplicity.

Encapsulation. Full-device encapsulation represents one of the most challenging steps, yet it was feasible to fully encapsulate two PTCE samples in a first proof-of-concept. The contact pads were successfully opened afterwards and showed a drop in successful connections, indicating that trace deformation may have occurred during lamination. In the current process, the active side of the die is covered by LT-LCP and as a consequence, the metallisation is fabricated on the LT-LCP. During encapsulation all LT-LCP will melt, introducing risk of movement of Cu tracks. Future process iterations will therefore investigate placing dies face-down into HT-LCP, allowing vias and metallisation to be supported by the mechanically stable HT substrate. A possible drawback of this approach is that it will conflict with the possibility to add glue/underfill when placing the dies as the glue will be located on the active side.

Material. While the majority of the results presented here were obtained using Rogers LCP, preliminary tests with Dycoplast LCP indicate comparable lamination behaviour and adhesion trends. However, differences in surface finish, flow behaviour and processing windows require dedicated optimisation. Future work will therefore focus on full process transfer to commercially available LCP grades, including Dycoplast materials.

3.2. Future research directions

The current work demonstrates the feasibility of the proposed fabrication process. Future work will focus firstly on improving and optimising the proposed processing steps and secondly on expanding the functional and mechanical tests of the chip packages.

Hermeticity and reliability. Long-term hermeticity testing of the ultrathin LCP packages, both at the material level and at the assembled device level, will be essential to determine lifetime and suitability for chronic implantation. The combination of LCP with ALD or parylene barrier layers could further enhance device performance and longevity but has not been tested yet for a functional device [14]. Finally, expanding functional testing beyond programming yields, such as full microcontroller operation, thermal cycling, and mechanical fatigue testing, would provide a more complete picture of device robustness and bonding quality.

Towards an implantable neurostimulation device. For medical device fabrication, the metallisation must be adapted from Cu to the biocompatible and inert Au or Ti, which has already been demonstrated but was omitted in this work for simplicity [24–26]. Additionally, the device must be integrated with electrodes fabricated in LCP as this is a crucial component for most implantable devices. Literature has already demonstrated the feasibility of fabrication of multi-layer LCP electrodes so new research will focus on integration of these electrodes within a functional device [27].

4. Conclusion

This work presents a complete fabrication route for ultrathin, fully LCP-based chip packages integrating thinned dies, high-density vias, patterned metallisation and assembly onto flexible substrates. By combining laser-skived cavities, controlled LCP lamination, a hybrid laser-plus-RIE via opening strategy and sputtered Cu–TiW interconnects, the process achieves reliable electrical connection to embedded chips while maintaining a total package thickness suitable for future flexible implantable systems.

The results demonstrate the viability of the proposed approach. Over 11.000 vias were successfully fabricated with negligible via resistance, and most embedded microcontrollers remained functional after full processing and assembly. High soldering yields on both PTCE and MSP430 devices confirm that the LCP packaging process is compatible with standard assembly flows. Moreover, successful full encapsulation of PTCE samples, despite some loss of pad connectivity, highlights the potential for multilayer all-LCP device integration, while also identifying important challenges in die alignment and lamination-induced deformation.

Overall, the findings establish that LCP is a strong candidate for ultrathin chip packaging, offering mechanical flexibility, chemical stability, low moisture uptake, and compatibility with both fine-feature routing and high-temperature processing. While improvements are still needed, particularly in cavity sizing, lamination control, void mitigation, and encapsulation yield, the demonstrated performance provides a solid foundation for future development of highly miniaturised, conformable implantable electronics. Future work will focus on enhancing long-term hermeticity, transitioning towards noble-metal metallisation for improved biostability, expanding to multi-IC integration, and incorporating electrode fabrication directly into the LCP stack. These advancements will further strengthen the potential of ultrathin LCP-based packaging as a scalable platform for next-generation biomedical devices.

CRediT authorship contribution statement

Sofie Lasure: Conceptualization, Methodology, Investigation, Writing – original draft. **João Alves Marques:** Resources. **Thomas Löher:** Resources. **Eckardt Bihler:** Resources. **Wim Van Paepegem:** Resources. **Robrecht Raedt:** Supervision. **Maarten Cauwe:** Conceptualization, Supervision, Writing – review & editing. **Rik Verplancke:** Conceptualization, Supervision, Writing – review & editing. **Pieter Bauwens:** Supervision, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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