A Highly-Integrated 1536-Channel Quad-Shank Monolithic Neural Probe in 55nm CMOS for Full-Band Raw-Signal Recording

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Abstract

We present a highly integrated neural probe for *in vivo* recordings, boasting a record of 1536 channels and 5120 TiN electrodes. The probe is optimally engineered with integrated capless LDOs and a low-power LVDS transmitter for energy-efficient data transfer, achieving a high level of integration and minimizing the number of external components. Innovative block-level optimization techniques result in a total area of $0.012mm^2$/ch, a total power of 19.34μW/ch, and the lowest total power-efficiency factor, while attaining excellent performance uniformity across channels. The probe is fabricated using a fab-compatible 300-mm post-CMOS process and fully validated in saline, demonstrating its ability to record full-band neural signals.

Introduction

CMOS neural probes have revolutionized electrophysiology by enabling dense electrode arrays and high channel counts [1], [2]. Yet, the quest for even higher channel densities persists to unravel complex neural dynamics. While efforts to shrink the AFEs have been key to achieve high channel densities [2]-[6], neural probes featuring innovative direct-to-digital AFEs have resulted in larger electrode pitches, wider shanks, and limited number of channels [5]-[7]. Thus, surpassing the current density limits requires a holistic approach, encompassing advanced monolithic integration and system-level innovations. This work introduces a monolithic neural probe with unparalleled channel density, featuring 5120 electrodes and 4x more readout channels (1536) within the same probe base area than our previous work [2]. By using innovative circuit-level optimizations, this probe achieves state-of-the-art area, power, and noise, while its high level of integration optimizes the overall system size and power.

Probe Architecture and Circuit Descriptions

Fig. 1 shows the high-level architecture of our neural probe, monolithically integrating 4 implantable shanks and a non-implantable base. Each shank includes 1280 selectable recording electrodes (pixels) and a tip reference electrode, allowing for simultaneous recording from 1536 electrodes via full-band readout channels at the base. This streamlined design integrates 96 16:1 analog MUXs, 96 12b compact SAR ADCs, a power management unit (PMU), and a digital control implementing a high-speed serializer and a low-power LVDS interface.

The recording channel is optimized for minimal area and power without compromising signal integrity, essential for recording full-band raw signals. An AC-coupled low-noise instrumentation amplifier (IA) with a 0.5Hz high-pass cutoff ensures rail-to-rail electrode-DC-offset (EDO) tolerance, crucial for performance uniformity across numerous channels. The input capacitors, placed over the active circuits, do not occupy area. The IA (Fig. 2(a)) is followed by 2 pseudo-differential buffers (Fig. 2(b)) that drive the MUX and ADC at 480kS/s (30kS/s per channel). Dynamic biasing is used for the buffers, active for only 2 of the 16 MUX periods, thereby reducing their power by 65%. This technique was not applied to the IA to prevent noise degradation as in [3]. The 12b SAR ADC (Fig. 2(c)) adopts a digital-less linearity-improving approach to reduce the complexity and area of the digital back-end. The compact (0.5fF unit) capacitive-DAC (CDAC) uses 5b thermometric plus 7b binary encoding, with 3 techniques further mitigating the mismatch, settling and noise errors: i) a "semi-switching-back" scheme in the 5 MSBs; ii) 3 redundant bits; and iii) majority voting for the 3 LSBs. To optimize area and power, 4 shared low-noise buffers, based on a low-power, fast-transient flipped voltage follower (FVF) with dual response loops (Fig. 2(d)), provide the reference voltage to the 96 ADCs. The fast loop (in blue) rapidly provides a high current for MSB conversions and reduces the CDAC settling errors, while the slow loop (in red) ensures precise LSB conversions. The buffers consume a total of 571.2μW, corresponding to only 5.95μW per ADC.

To miniaturize the whole system and packaging, the PMU integrates 3 capless LDOs using a pass-NMOS architecture with two feedback loops, which deliver both high precision and fast transient response [8]. The 1.8V digital IO supply is used as LDO input voltage. A sub-BGR generates the mid-supply and ADC-reference voltages with minimum power.

A high-speed serializer delivers the ADC data (552.96Mbps) to a low-power LVDS transmitter (TX). A PLL generates a 1.536GHz clock, which is then divided to generate the 614.4MHz serializer clock. A custom LVDS is designed with 200mV common mode and $200mV_{p\text{-}p}$ differential output, achieving an energy efficiency of 9.4pJ/b.

Measurement

The neural probe was fabricated in a 55nm 9-metal-layer CMOS technology, followed by a fab-compatible 300mm-wafer process for i) stress compensation (<100μm shank bending), ii) via formation, iii) TiN electrode patterning ($12{\times}12μm^2$), iv) bond-pad opening, v) deep Si etching, and vi) dicing-before-grinding singulation. Fig. 3 shows a singulated probe with SEM images of the shank tips and neck. The shanks are 10mm long, 70μm wide and 30μm thick, while the base occupies an area of $15.67mm^2$. The electrical performance of the whole signal chain (from pixel to ADC) is characterized for all the 1536 channels. The total power consumption is 29.7mW, including all the blocks and data telemetry. Fig. 4 shows the measured channel input-referred noise (IRN) spectrum and the integrated noise histograms (n=1536). The average noise is $6.01{\pm}0.39μV_{rms}$ in the AP band (300-10kHz) and $7.58{\pm}0.79μV_{rms}$ in the LFP band (0.5-1000Hz). Fig. 5(a) shows the acquired output data with a $10mV_{pp}$, 1kHz sinusoidal pixel input, while the histograms (n=1536) of the channel gain, input-referred offset, and THD are shown in Fig. 5(b)-(d). The measured channel transfer function is shown in Fig. 6. As shown in Fig. 7, the SNR and SNDR of the SAR ADC are 67.63dB and 64.92dB, respectively, demonstrating 4.09dB SNDR improvement with the proposed "semi-switching-back" scheme. Detailed area and power breakdowns are shown in Fig. 8. Finally, full-probe functionality is demonstrated by applying a pre-recorded neural signal to a saline solution where the probe shank is immersed (Fig. 9(a)). The recorded signal from a subset of channels is shown in Fig. 9(b).

Table I summarizes the performance of our probe and compares it with state-of-the-art full-band (LFP+AP) raw-signal neural recording designs. We achieve the highest number of channels, one of the smallest channel areas, the best total power-efficiency factor (PEF) and the highest level of integration, while maintaining a 15μm electrode pitch, a rail-to-rail EDO cancellation, and good noise performance. This groundbreaking neural probe outperforms its predecessor [2] by achieving 22% lower noise, 4.1× smaller channel area, and 4.6× lower channel power, setting a new benchmark for neural recording technology.

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References

[1] C. M. Lopez, *et. al*, *TBioCAS*, 2017. [2] S. Wang, *et. al*, *TBioCAS*, 2019. [3] D. Y. Yoon, *et. al*, *VLSI* 2021. [4] X. Yang, *et. al*, *JSSC* 2023. [5] D. De Dorigo, *et. al*, *JSSC* 2018. [6] D. Wendler, *et. al*, *JSSC* 2022. [7] F. Boi, *et. al*, *bioRxiv* 2020. [8] W. Y. Hsu, *et. al*, *ESSCIRC* 2023.

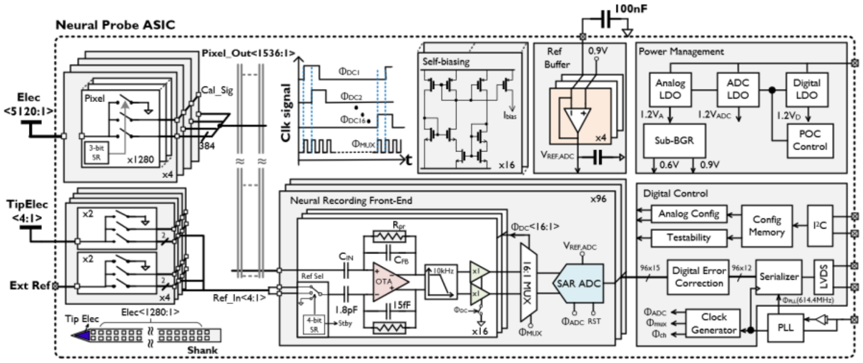


Fig. 1. High-level diagram of the monolithic CMOS neural probe IC.

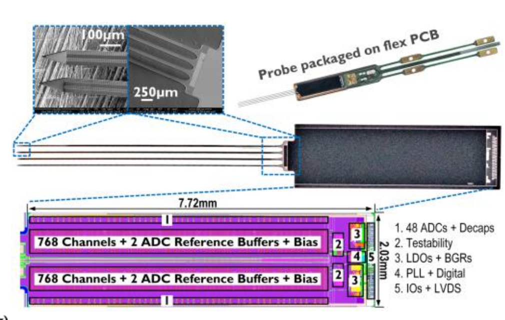


Fig. 3. Micrograph and SEM images of the singulated neural probe after post-CMOS fabrication and packaging.

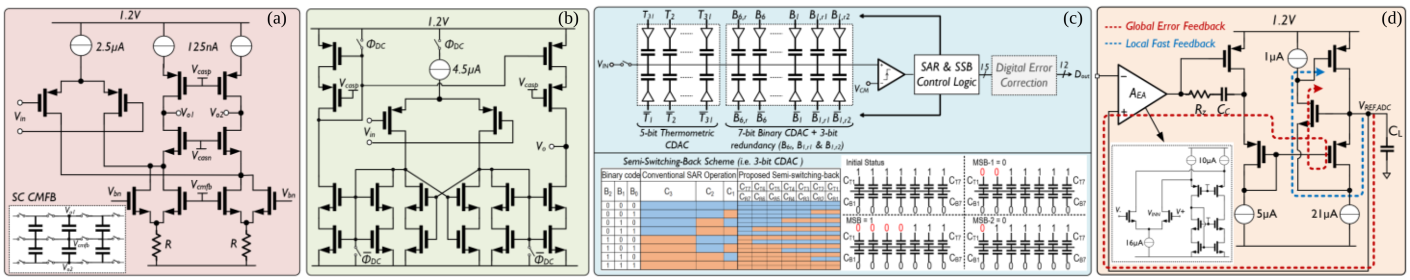
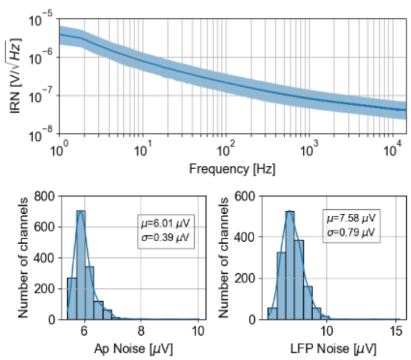


Fig. 2 (a) Schematic of the IA OTA; (b) Dynamic-biased buffer; (c) 12-bit SAR ADC with semi-switching-back scheme; (d) ADC reference-voltage buffer.



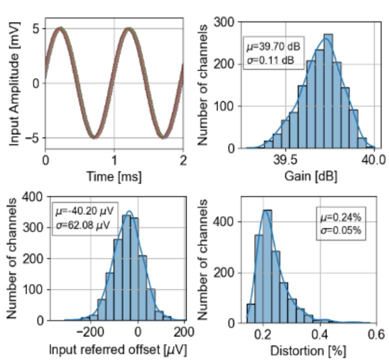


Fig. 4. Full-band IRN spectrum across all channels, and integrated noise histograms (n=1536) for the AP and LFP bands.

Fig. 5. Transient output waveform with a $10mV_{pp}$,1kHz sine input, and the histograms of gain, offset and THD across channels.

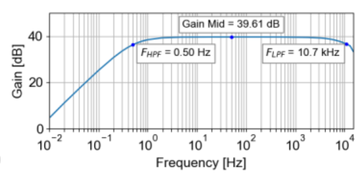


Fig. 6. Measured channel transfer function.

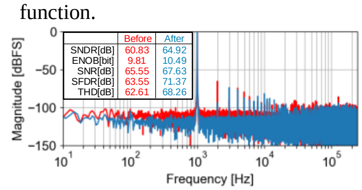
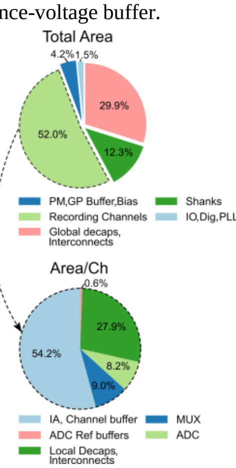


Fig. 7. Measured ADC output spectrum with semi-switching-back ON and OFF.



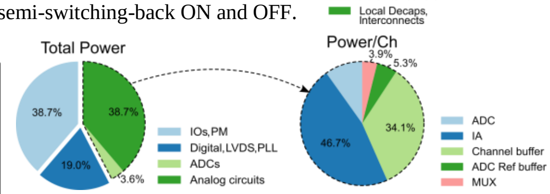


Fig. 8. Area and power breakdowns of the neural probe.

TABLE I. Comparison with State-of-the-Art Full-Band, Raw-Signal Neural Recording ICs

		This Work	[1]	[2]	[5]	[6]	[7]	[3]	[4]
Device Type		Monolithic Probe	Monolithic Probe	Monolithic Probe	Monolithic Probe	Monolithic Probe	Monolithic Probe(c)	ROIC+Flexible Electrodes	ROIC
Probe Specifications									
No. of Electrodes		5120	966	5120	144	8	1024	--	--
Electrode Pitch		15μm	20μm	15μm	70μm	55μm	29μm	--	--
Shank Width/Thickness		70μm/30μm	70μm/24μm	70μm/24μm	70μm/50μm	>84μm/--	80μm/30μm	--	--
Shank Length		4 x 10mm	10mm	4 x 10mm	10.5mm	--	5mm	--	--
Readout Specifications									
Technology / Supply (V)		55nm / 1.2	130nm / 1.2	130nm / 1.2	180nm / 1.8	180nm / 1.8	180nm / NA	65nm / 1.2	22nm / 0.8
Channel topology		AC-coupled IA+SAR	AC-coupled IA+SAR	AC-coupled IA+SAR	DC-coupled IΔΣ	DC-coupled IΔΣ	DC-coupled IA+Off-chip ADC	AC-coupled IA+SAR	AC-coupled 1st-order Δ2Σ
Application		AP+LFP	AP+LFP	AP+LFP	AP+LFP	AP+LFP	AP+LFP	AP+LFP	AP+LFP
Level of Integration	ADC	Yes	Yes	Yes	Yes	Yes	No	Yes	No
	Digital Control	Yes	Yes	Yes	No	No	No	Yes	Yes
	PMU	Yes	No	Yes	No	No	No	Yes	No
	LVDS & PLL	Yes	No	No	No	No	No	No	No
No. of Channels		1536	384	384	144	8	1024	1024	128
Area/Channel (mm^2)		0.0062	NA	0.035	0.0049	0.0046	NA	0.0062	0.0045
Total Area/Channel (mm^2)		0.012[a)]	0.12	0.0497	NA	NA	0.011[(c)]	0.02	0.0051[b)]
Bandwidth (Hz)		0.5-10k	0.5-10k	0.5-10k	0-10k	0-10k	1-7.5k	5-10k	0.5-10k
AP Noise (μVrms) (0.3~10kHz)		6.01± 0.39	6.36± 0.8	7.74± 0.72	13.43	9.21	6.5± 2.1 (300-7kHz)	8.89	7.71± 0.36
LFP Noise (μVrms) (0.5~1kHz)		7.58 ± 0.79	10.32± 1.89	7.78± 0.93	9.95	11.83	8.5± 2.7 (1-300Hz)	6.8 (5-1k)	11.9 ± 1.13
Power/Channel (μW)		7.03	NA	45.3	39.14	14.62	6[(c)]	2.72	6.02
Total Power/Channel (μW)		19.34	49.06	95.1	46.08	25.75	NA	24.1	12.57
AC input range (mV_{pp})		10	10	12.5	22.5	15.2	NR	0.75-4.87	43
Channel PEF[(d)] (AP band)		37.6	NA	401.5	1044.3	183.5	50	31.8	52.9
Total PEF (AP band)		103.3	293.6	842.8	1229.5	323.1	NA	281.9	110.5
EDO Tolerance (mV)		Rail-to-rail	Rail-to-rail	Rail-to-rail	<22.5	60	NR	Rail-to-rail	Rail-to-rail

NA: Do not apply, NR: Not reported. a) The whole ASIC area including shanks, and IOs; b) Includes only the chip core; c) With 32 off-chip ADCs ; (d) PEF = $Vn^2 x(2xP_{tot}/V_T 4k_B T\pi BW)$

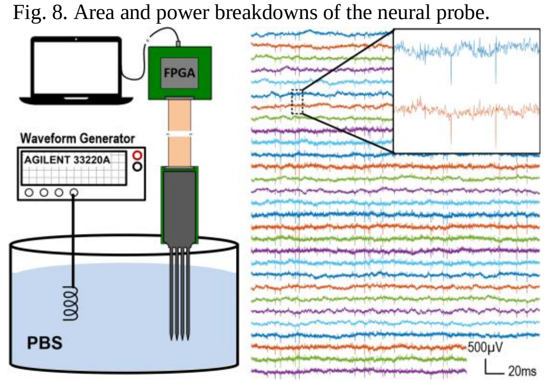


Fig. 9 (a) Saline test setup, and (b) recorded full-band neural signals from a subset of channels.