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Electrochemical deposition of indium from chloride bath for low-temperature microbump bonding

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Indium chloride bath was characterized towards the application of low-temperature thermal compression bonding. The electrochemical behavior of the indium chloride bath was analyzed using the cyclic voltammetry method. Electrochemical deposition of indium was carried out at various deposition factors on different materials such as copper, nickel, and cobalt. Based on the results of indium deposition obtained from the blanket films, indium bumps were electrochemically fabricated inside a through-resist hole pattern at various current densities. In addition, stacked indium bumps with various metals (Cu/In, Cu/Ni/In, Cu/Co/In) were formed for a practical application of micro bump bonding. Moreover, the formation of the intermetallic compounds between indium and under bump metallization was investigated. © 2022 The Japan Society of Applied Physics

1. Introduction

In the past decades, the performance of electronic devices was well improved along with Moore's law. However, in recent days, the scaling was confronted with several limitations such as design complexity, exponentially increased manufacturing cost, and low yields of processes when the feature size shrunk under several nanometer scales. Therefore, three-dimensional (3D) packaging technologies have become inimitable for high-performance electronic devices.¹⁾ Among these 3D packaging technologies, thermal compression bonding (TCB) by solder base micro bump was one of the critical technologies for stacking. Tin (Sn) is the material widely used for solder bump bonding. However, the sequence of (relatively slow) ramp-up and compression during die stacking increases the throughput for die-to-wafer stacking, which increases the cost of ownership. The previous report by Lin Hou et. al confirmed that low-temperature bonding reduces total stacking process time since the ramp-up time can be shortened.²⁾ In order to reduce the interfacial temperature with good connectivity with Sn, a unique bottom pad is utilized in the stacking. For further simplification of the low-temperature stacking, replacing Sn with a low melting point metal is ideal.

Indium was one of the promising alternatives for low-temperature bump bonding due to its low melting temperature (157 °C). In addition, indium has several unique properties, such as high thermal and electrical conductivity and good ductility in cryogenic environments.^{3,4)} Therefore, indium has been comprehensively investigated for bump application, in particular for infrared (IR) detector array, silicon readout electronics, IR focal plane array, silicon pixel detector, and X-ray detector⁵⁻⁷⁾ where CTE mismatch can be a limiting factor when high-temperature bonding is used. Indium enables low-temperature bonding for such devices mitigating the CTE mismatch between Si and III/V or II/VI substrates for lower than 20 μm pitch micro bumps. Therefore, the number of pixels can be very high using high-density interconnects which is critical for some space and medical devices such as MRI. These indium bumps were deposited by vapor phase evaporation methods⁶⁻⁹⁾ and electrochemical deposition (ECD).^{3,4,10-22)} Most of the indium bumps were fabricated by the ECD method because

ECD is suitable for filling into high-aspect-ratio structures with a high deposition rate compared with the vacuum deposition method. Indium sulfamate bath has been mainly used for indium bump fabrication.^{3,13-21)} However, indium sulfamate bath has a complex composition, and indium sulfamate salt has hard accessibility. Furthermore, a study on indium bump ECD on under bump metallization (UBM) materials has also been insufficient. A deep understanding of ECD indium on UBM materials is essential to determine reflow temperature and bonding temperature.

This research investigated the ECD of indium film and bump using indium chloride bath on various UBM materials. As for the candidates of UBM, we have been investigated Co on top of standard Sn system UBMs, which are Ni and Cu. In our previous study, we found that Co is a promising Sn system UBM because the Co/Sn IMC growth is suppressed compared with others when the temperature is below 150 °C.²³⁾ Therefore, we have analyzed Co as well in this study since In system is typically lower temperature than the Sn system.

In addition, the chloride bath has the advantage of self-cleaning the UBM oxide layer prior to plating which is essential to get good adhesion or IMC formation between the indium and UBM layer. The electrochemical behavior of the indium chloride bath was analyzed by the cyclic voltammetry method. Indium films were deposited at various current densities and UBM materials based on the cyclic voltammetry results. A stacked 20 μm pitch bump structure with indium and various UBM were fabricated. At last, IMC formation behavior between indium and various UBM materials was studied.

2. Experimental methods

All ECD and analysis were conducted in a glass cell with a conventional three-electrode system described in Fig. 1. Cleaved blanket and patterned substrates were mounted in a sample holder with an opening area of 1.54 cm² connected with a rotating disk electrode (RDE) system. The sample mounted on RDE was used as a working electrode. Blanket substrates were prepared on 300 mm Si wafers followed 50 nm plasma-enhanced chemical vapor deposition of SiN, physical evaporation deposition (PVD) of TiW (30 nm)/Cu (150 nm). Both Ni and Co substrates were prepared by ECD

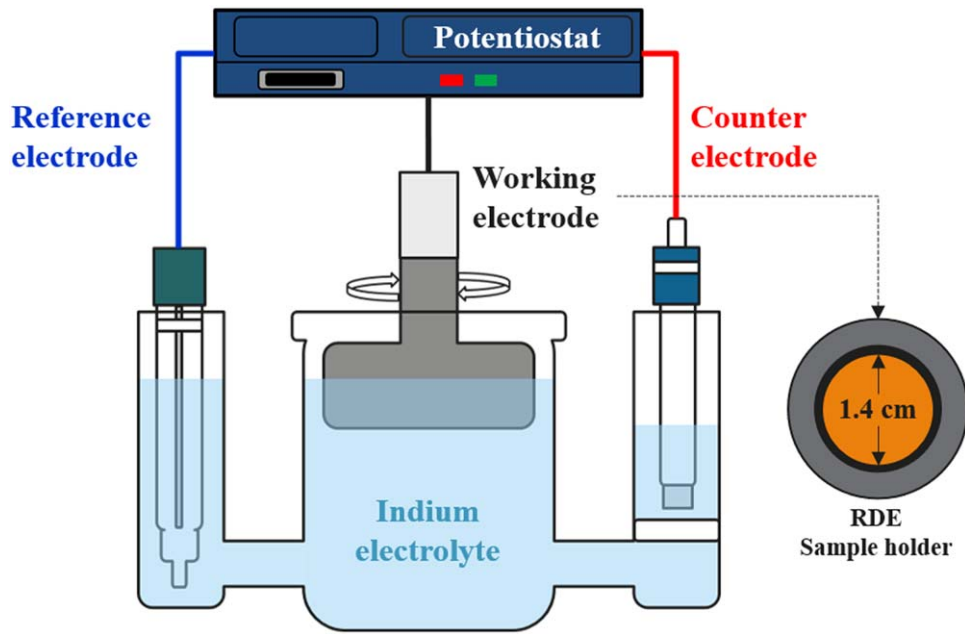


Fig. 1. (Color online) Cell configuration for indium film and bump electrochemical deposition.

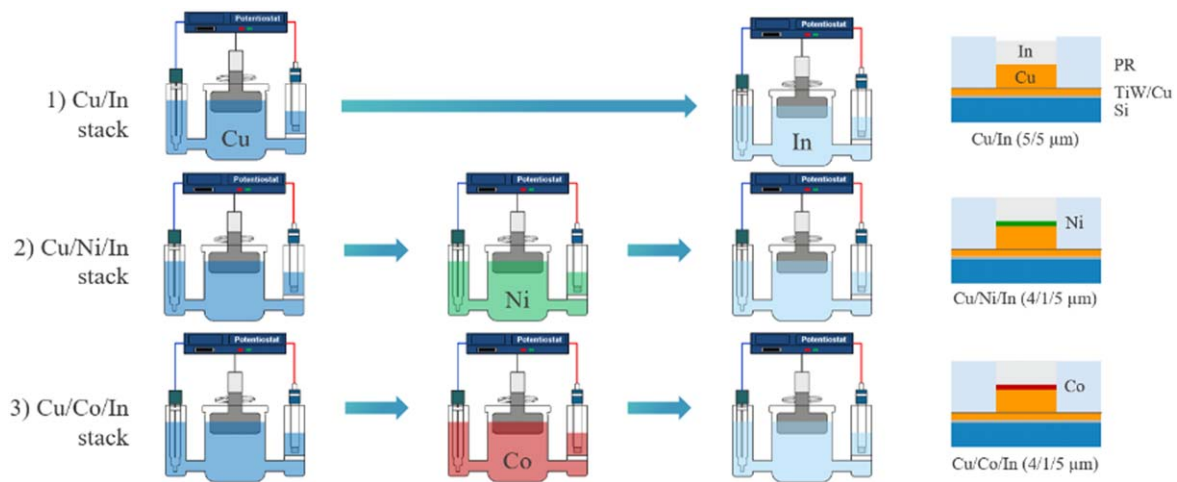


Fig. 2. (Color online) Schematic diagram of stacked bumps deposited on various UBM materials.

with 1 μm thickness on Cu blanket substrate. A 14 μm photoresist was coated and patterned on the PVD Cu seed layer for the bump patterned sample. The through-resist hole pattern was 8 μm diameter (20 μm pitch) and 14 μm height. A Pt-coated Ti plate was used as the counter electrode and a 3.0 M Ag/AgCl electrode as the reference electrode.

Reagent-grade chemicals were utilized for all indium ECD and electrochemical analysis experiments. The electrolytes for indium ECD consisted of 0.25 M indium chloride (InCl_3), 0.50 M potassium chloride (KCl) in 250 ml of 18.6 Mohm deionized water. The pH value of the as-mixed indium electrolyte was 3.2, and pH was adjusted to 1.5 by using hydrochloric acid (HCl).

Electrochemical analysis and deposition were conducted using a potentiostat/galvanostat (PARSTAT4000, AMETEK Co). For the analysis of electrochemical behavior and appropriate current density selection, cyclic voltammetry (CV) analysis was conducted at the potential range between 0.4 and -1.4 V versus Ag/AgCl with a scan rate of

10 mV s^{-1} without agitation. Indium film and bump were deposited galvanostatically at -10 and -50 mA cm^{-2} with the rotation speed of 100 rpm until total deposition charge density was accumulated to 7.5 C cm^{-2} . For the observation of indium bumps on various UBM materials, Cu/In, Cu/Co/In, and Co/Ni/In stacked bumps were fabricated through several steps of ECD presented in Fig. 2. For the Cu/In stacked bump, the Cu bump with 5 μm height was firstly deposited on a patterned substrate, and then In with 5 μm height was deposited on Cu. For the case of the Cu/Co/In and Co/Ni/In stacked bumps, Cu with 5 μm height was firstly deposited on the patterned substrate, then Co or Ni bump with 1 μm height was deposited on Cu, and finally In with 5 μm height was deposited on Cu/Co or Cu/Ni. Deposited indium films and bumps were observed using scanning electron microscopy (SEM; FEI, Nova NanoSEM) and atomic force microscopy (AFM; Bruker, Icon PT). The behavior of IMC formation between indium and various UBM materials was studied using the in situ resistance

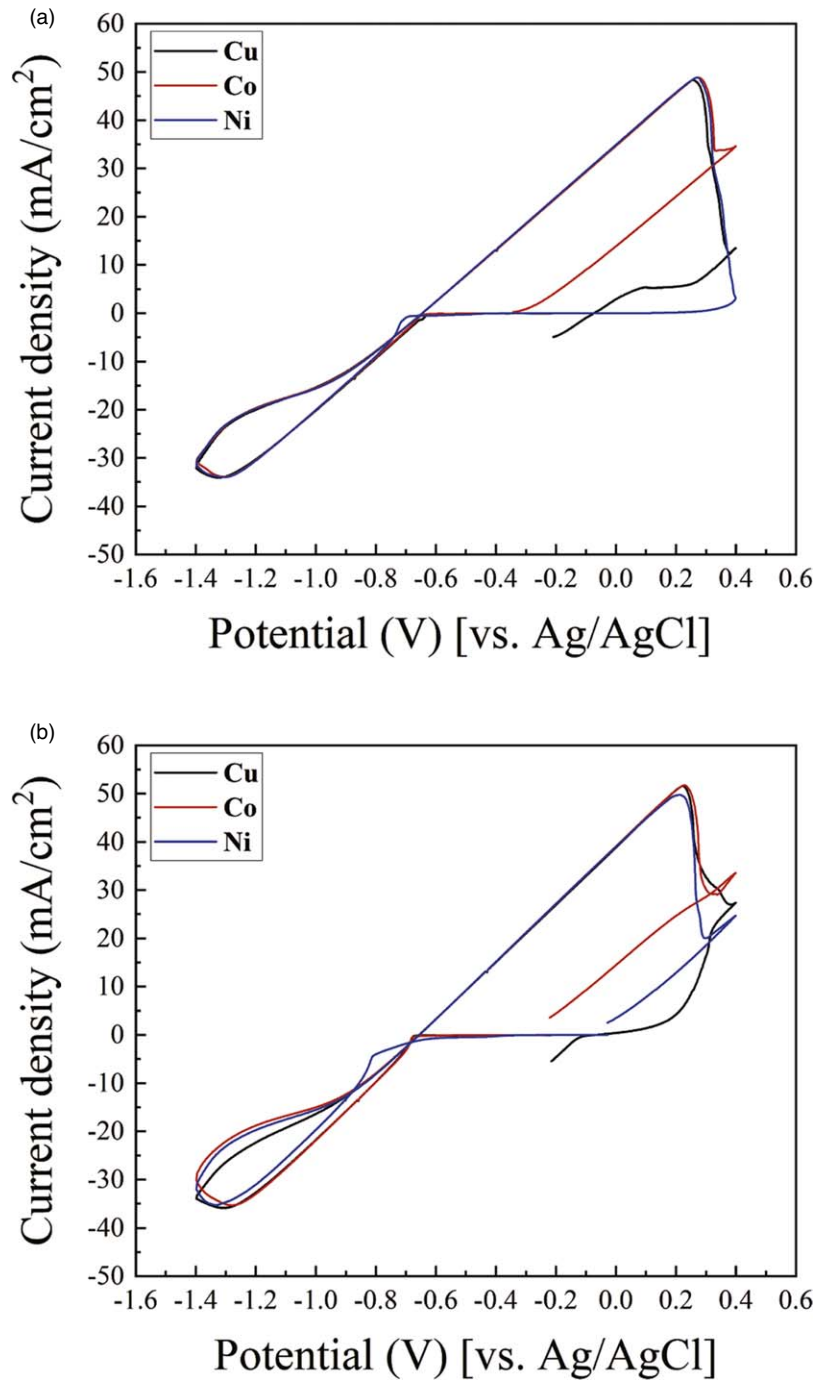


Fig. 3. (Color online) Cyclic voltammogram of indium chloride electrolyte at (a) pH 3.2 and (b) pH 1.5 on Cu, Co, and Ni substrate.

measurement method reported by Lin Hou et al.²⁴⁾ The measurement was performed in a closed chamber with a thermal chuck and four electrical probes under N₂ atmosphere. Resistance was measured every 15 s. Three indium on UBM samples that Cu/In, Ni/In, and Co/In were measured using this in situ resistance measurement method. All the measurements were conducted at 140 °C for 24 h.

3. Results and discussion

3.1. Electrochemical analysis of indium chloride bath

For analyzing the electrochemical behavior of indium chloride baths and determining the appropriate current density range, cyclic voltammetry was conducted. Cyclic voltammograms from indium chloride bath at pH 3.2 and 1.5 are shown in Figs. 3(a) and 3(b), respectively. The inset

graph in Fig. 3 was indicated an enlarged part of the cathodic scan to distinguish the potential where the reduction was initiated. Overall, regardless of pH value, indium reduction was observed at the cathodic direction scan, and indium oxidation was observed at the anodic direction scan. Similar electrochemical behavior of these cyclic voltammograms was observed in the previous report.¹⁰⁾ At pH 3.2, indium reduction potential on Cu and Co was -0.6 V, and reduction potential on Ni was -0.7 V. However, the reduction potential of indium was slightly shifted to the negative direction at pH 1.5; -0.68 V on Cu and Co substrates and -0.8 V on Ni substrate. This negative shift was not typical behavior. Reduction potential is generally shifted to positive when the pH is decreased, according to the Nernst equation. It indicates that this abnormal behavior was caused by the effect

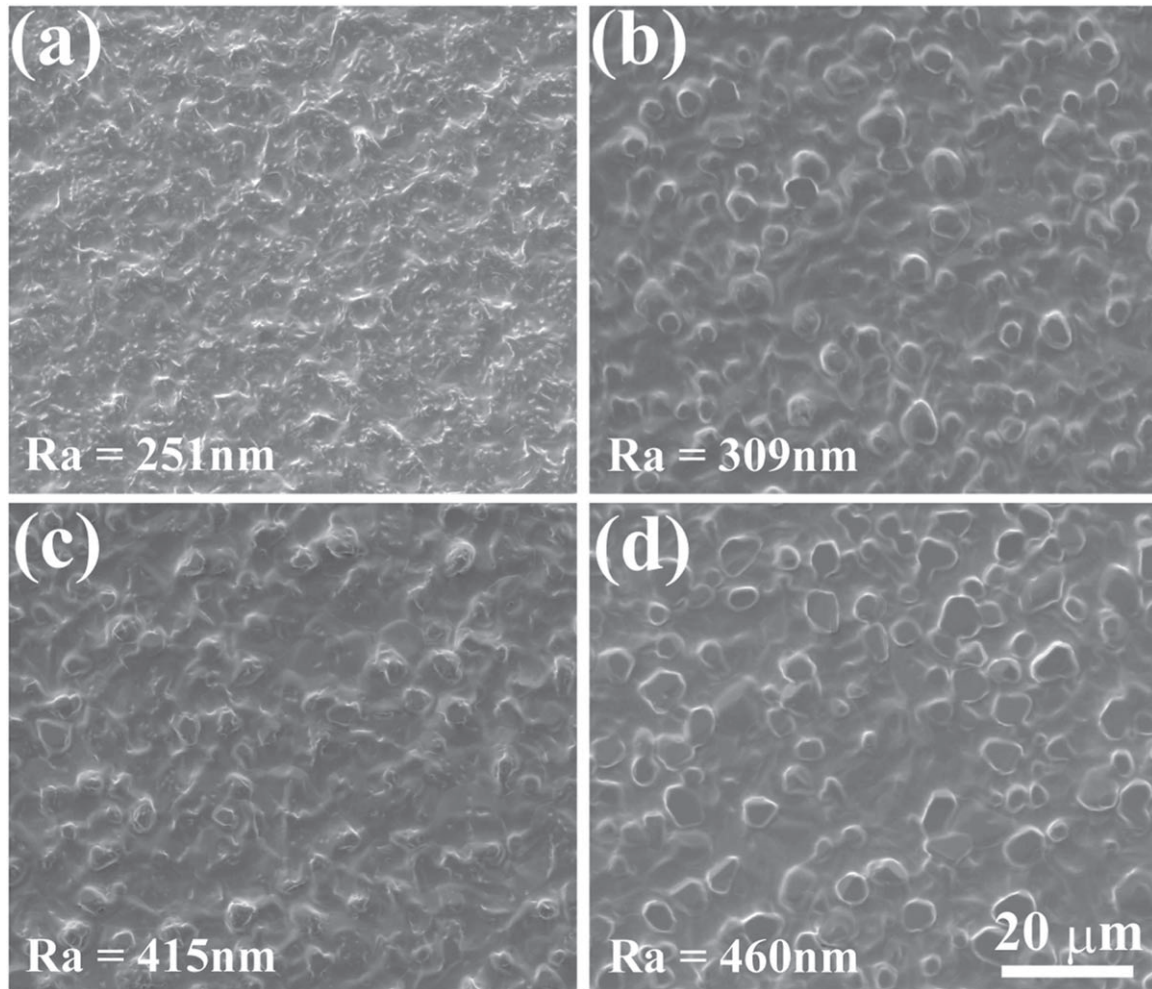


Fig. 4. SEM images of indium films electrochemically deposited at (a) pH 1.5, -10 mA cm^{-2} , (b) pH 1.5, -50 mA cm^{-2} , (c) pH 3.2, -10 mA cm^{-2} , and (d) pH 3.2, -50 mA cm^{-2} .

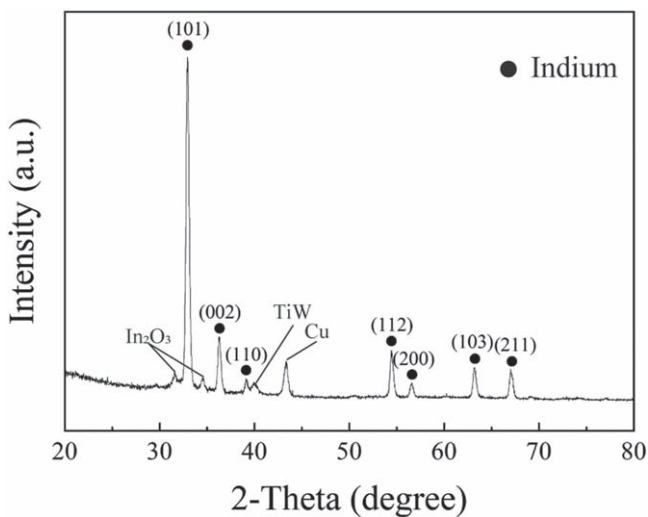


Fig. 5. XRD pattern of indium film electrochemically deposited at pH 1.5, -10 mA cm^{-2} with a charge density of 7.5 C cm^{-2} .

of chloride ion concentration; in other words, chloride ions might form a complex with metal ions at high chloride concentration.²⁵⁾

3.2. Characterization of ECD indium films deposited from indium chloride bath

Based on the results of CV analysis, indium films were electrochemically deposited on Cu blanket substrate at each

pH (1.5 and 3.2) and current densities (-10 and -50 mA cm^{-2}) with a charge density of 7.5 C cm^{-2} . These SEM images and roughness values from AFM analysis were shown in Fig. 4. All indium films were deposited uniformly on the Cu blanket substrate. There was no significant change on deposited indium films regardless of deposition condition; however, the roughness was increased when pH and current density were increased. From the CV analysis, it was known that the current density of -50 mA cm^{-2} was higher than that of the limit current density. Therefore, the morphology of indium film at -50 mA cm^{-2} was rougher than that of indium film at -10 mA cm^{-2} . To confirm that the deposited indium film is metallic pure indium, XRD analysis was carried out on indium film deposited on Cu blanket substrate at pH 1.5 and -10 mA cm^{-2} as shown in Fig. 5. Body-centered tetragonal indium (JCPDS 01-085-1409) was observed at this XRD pattern; therefore, it was confirmed that deposited indium films from indium chloride electrolyte were metal indium. Not only on Cu UBM, ECD of indium film was also conducted on Ni and Co blanket substrates at pH 1.5 with current densities of -10 and -50 mA cm^{-2} . Figure 6 shows the top view SEM images of Indium deposited on Co and Ni film. Uniform growth of indium films was also observed on Ni and Co. The surface roughness was decreased as current density decreased, which is similar behavior to Cu. However, indium films on Ni were rougher surface than

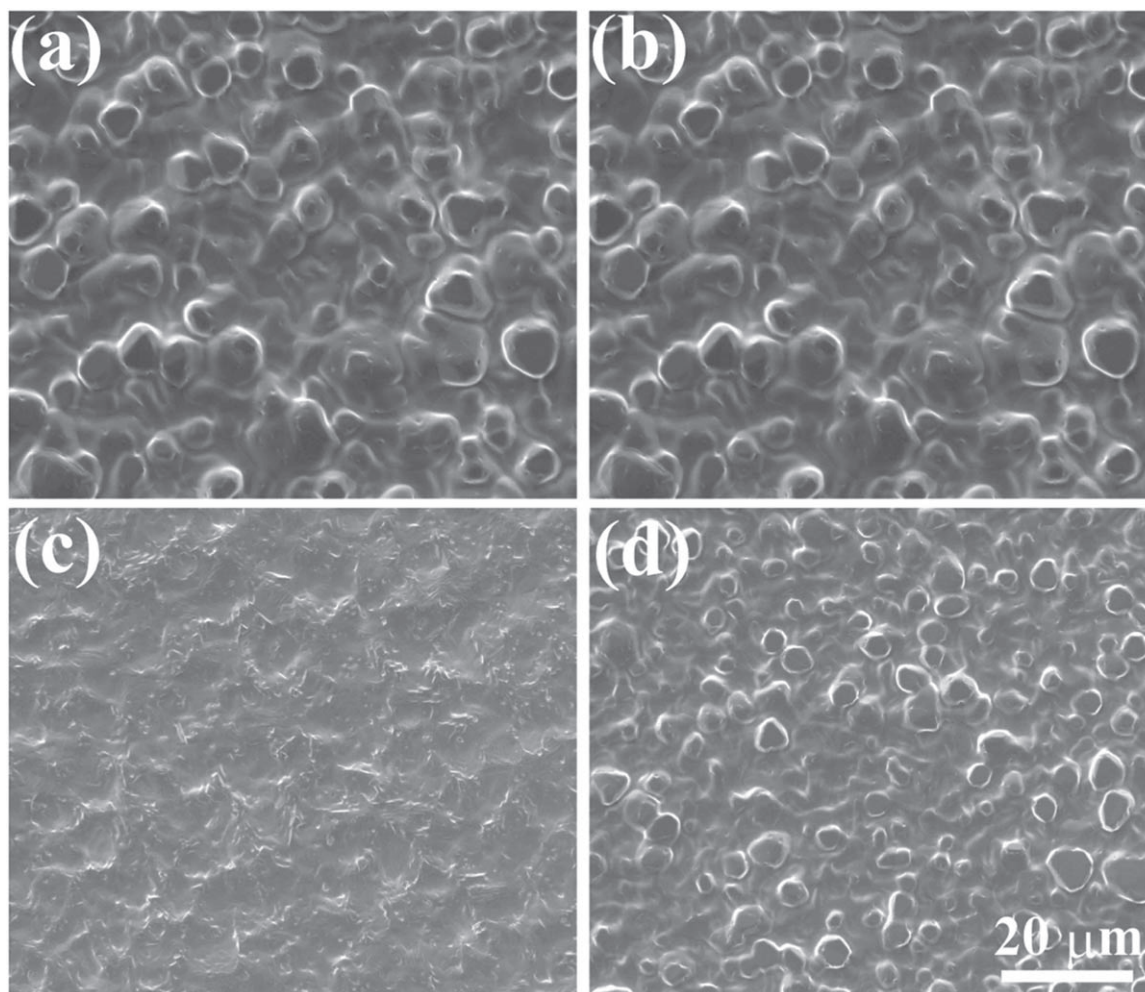


Fig. 6. SEM images of Indium films deposited on (a) Ni UBM at -10 mA cm^{-2} , (b) Ni UBM at -50 mA cm^{-2} , (c) Co UBM at -10 mA cm^{-2} , and (d) Co UBM at -50 mA cm^{-2} .

indium films on Cu and Co, while the surface of indium film on Co was similar to that on Cu. It was because indium reduction potential on Ni was more negative than the reduction potential on Cu and Co as we observed in Fig. 3.

3.3. Through-hole resist plating

By these results of indium film ECD, indium bumps were fabricated at pH 1.5 and current densities of -10 and -50 mA cm^{-2} . Figure 7 shows the tilt view SEM images of indium bump directly deposited on the Cu seed layer. Indium bumps were successfully formed by ECD from indium chloride bath and its bump shape was similar to the bump shape formed from indium sulfamate bath.^{13,14,21)} By changing the current density, the top surface of the bump was expected to be changed as it was seen on flat samples. However, their top surface was not drastically changed regardless of current density. It might be due to the indium ion concentration being lower inside through-resist hole than the flat surface; therefore the diffusion flux of indium ion was limited at the bottom part of the hole pattern regardless of current density. It resulted in similar shapes of bump top surface at both current densities of indium deposition.

Cu underneath the indium bump is necessary to achieve better resistivity as an aspect of the micro bump application. Therefore, Cu/In stacked micro bumps were fabricated on a patterned substrate at pH 1.5 and current densities of -10 and -50 mA cm^{-2} . Figure 8 shows tilt view SEM images of

Cu/In micro bumps. the Cu/In micro bumps were successfully fabricated without any defects at the interface. Unlike the case only deposited indium inside the through-resist hole, the Cu/In bumps surface was controlled by current density as we observed on flat samples. It may be due to the aspect ratio towards the bottom of the pattern. The diffusion of indium ion at the bottom part (here, top of ECD Cu) was much closer than diffusion towards the PVD Cu (bottom of the resist). Therefore, the deposition reaction becomes like blanket samples.

After the indium bump on Cu, indium bump ECD on other UBM materials was also conducted. Cu/Ni/In and Cu/Co/In stacked micro bumps were fabricated at pH 1.5 and a current density of -10 mA cm^{-2} . Figure 9 shows the tilt view SEM images of Cu/Ni/In and Cu/Co/In micro bumps. These metal stacks were also successfully fabricated without any defects at the interface. However, the surface shape of Cu/Ni/In bumps was concave while that of Cu/In and Cu/Co/In bumps was seemed to flat. It was caused by the negative reduction potential of indium on Ni UBM as confirmed by previous results.

3.4. Characterization of ECD indium films deposited from indium chloride bath

In addition to fabrication of In bumps on various UBM materials, it is essential to know about the behavior of IMC formation between In and UBM materials at high storage

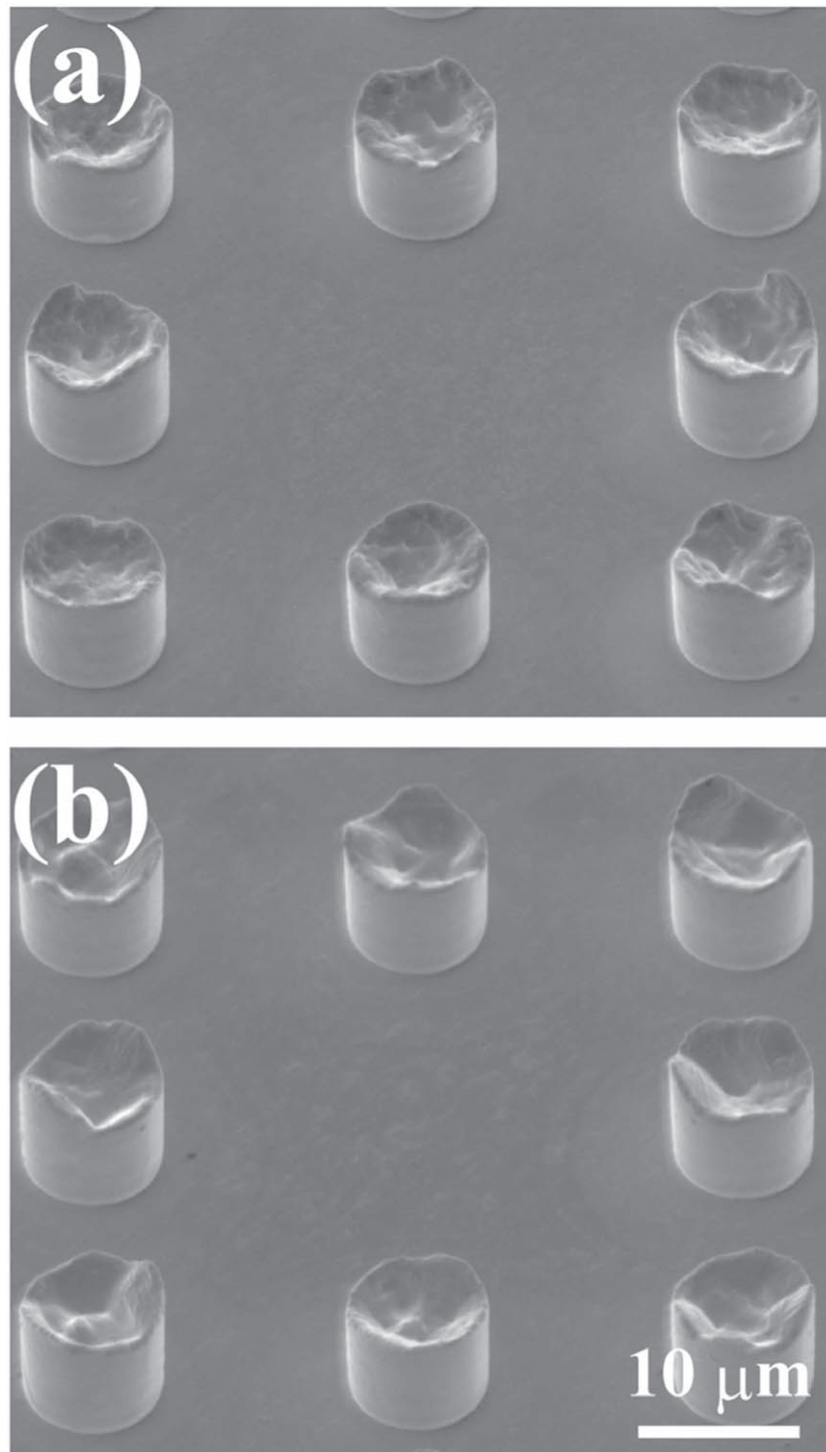


Fig. 7. SEM images of indium bump deposited on patterned substrate at (a) -10 mA cm^{-2} , and (b) -50 mA cm^{-2} .

temperature for the reliability of bump bonding. Therefore, IMC formation behavior of Cu/In, Ni/In, and Co/In structures was observed using the in situ resistance measurement method at $140 \text{ }^\circ\text{C}$ for 24 h. The transients of resistance and vertical SEM images of the samples before and after measurements were presented in Figs. 10 and 11, respectively. Resistance of Cu/In sample was rapidly increased at the beginning, and it was gradually increased until the measurement was finished as shown in Fig. 10(b). It indicates that Cu–In IMC was rapidly formed and the diffusion continues during the measurement. The confirmation of IMC should be executed by qualitative elemental analysis,

e.g. energy-dispersive X-ray, or X-ray Fluorescence. In fact, we have executed these analyses for indium and metal stacks. However, the sample prep for the thin film caused some artifacts to distinguish between indium and IMC. Therefore, we defined the IMC formation by contrast difference in SEM and refer to previous reports on relatively thick films. The Cu–In IMC formation was confirmed from the SEM images in Figs. 11(a) and 11(d). It is worth noting that Cu–In IMC already existed at the as-deposited Cu/In sample because CuIn_2 can be spontaneously formed even at $-40 \text{ }^\circ\text{C}$.²⁶⁾ The IMC is being formed even at staging at room temperature. From the resistance transient of Ni/In structure in Fig. 10(c),

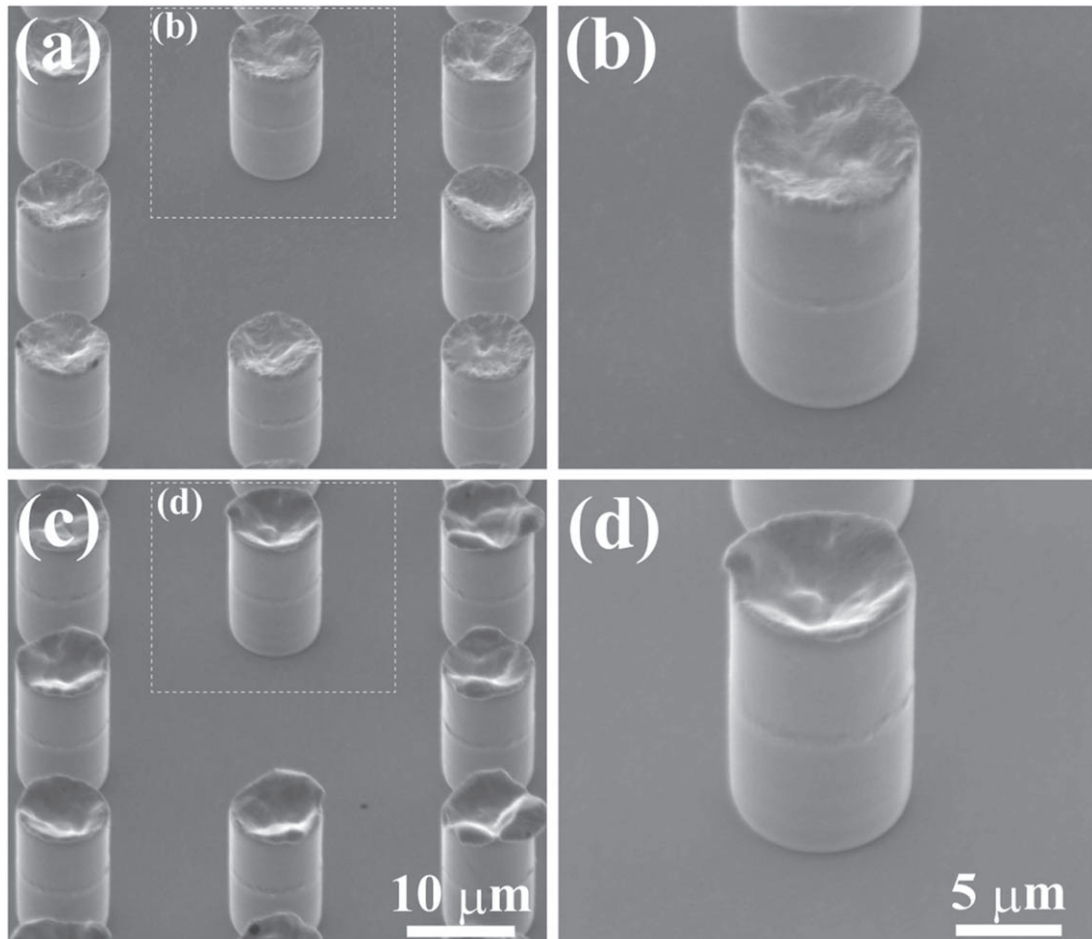


Fig. 8. SEM images of Cu/In stacked bump deposition on patterned substrate at (a) -10 mA cm^{-2} , and (b) -50 mA cm^{-2} .

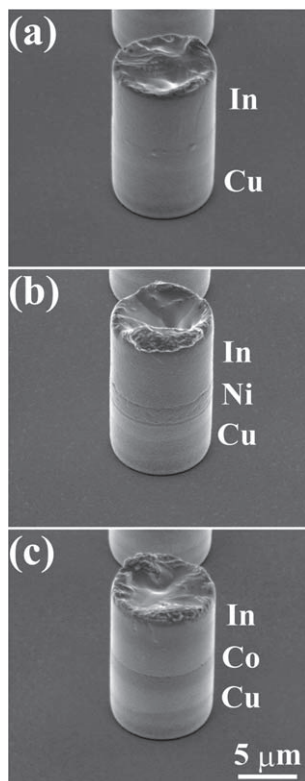


Fig. 9. SEM images of various types of stacked bump deposition on a patterned substrate; (a) Cu/In, (b) Cu/Ni/In, and (c) Cu/Co/In.

resistance was also continuously increased until the measurement was finished. IMC formation between Ni and In was also observed from Fig. 11(e). However, indium was not fully reacted with Ni UBM compared with Cu/In structure. On the contrary, the resistance of Co/In was not significantly increased during the measurement in Fig. 10(d). In addition, it was not easy to distinguish IMC in Fig. 11(f). These in situ resistance measurements were indicated that IMC formation was shown in different behaviors on UBM materials. IMC formation was suppressed in the case of Ni and Co UBM while indium IMC was significantly formed on the Cu UBM. Further analysis such as EDX and cryogenic FIB are required to identify the corresponding IMC phases. A similar trend has been observed from the Sn base system as we reported before.²⁷⁾ It was found that CoSn_3 IMC grows slow at temperatures below $150 \text{ }^\circ\text{C}$. However, it has rapid growth at temperatures above $150 \text{ }^\circ\text{C}$ due to very low activation energy and very high interdiffusion coefficient. We would assume a similar principle can be applied for indium with cobalt. The observations suggest that Cobalt is the best candidate of diffusion barrier for low-temperature stacking with indium-based solder.

4. Conclusions

Using a simplified indium chloride electrodeposition bath, we successfully fabricated the indium films and micro-bumps on various UBM materials. Indium chloride bath was shown

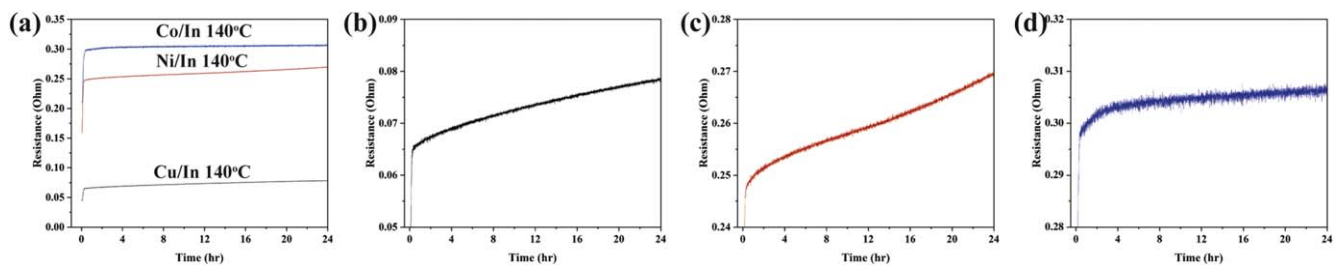


Fig. 10. (Color online) Time transients of resistance during In-situ resistance measurement at 140 °C for 24 h (a) whole samples, (b) Cu/In, (c) Ni/In, and (d) Co/In sample.

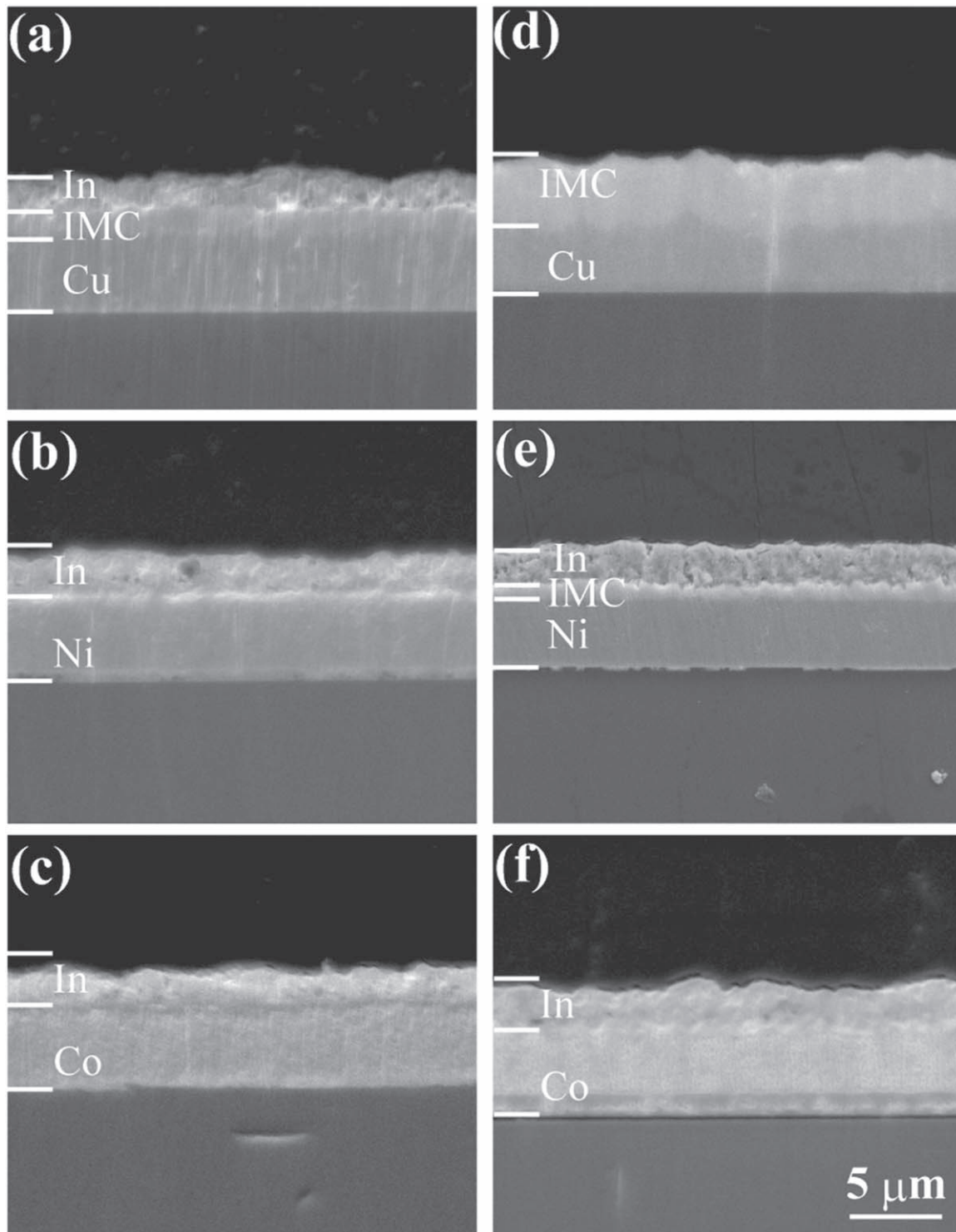


Fig. 11. Cross-sectional SEM images of in situ resistance measurement samples; before the measurement of (a) Cu/In, (b) Ni/In, (c) Co/In sample, and post-measurement of (d) Cu/In, (e) Ni/In, and (f) Co/In sample.

similar electrochemical behavior of indium sulfamate bath. Equivalent indium films and bumps were also formed from the indium chloride bath compared to the indium sulfamate bath. It was indicated that a simple indium chloride bath can be used as an alternative to an indium source for the 3D application. IMC behavior between indium and various UBM materials was studied using the in situ resistance measurement method. The IMC barrier properties are varied on the different UBM materials. Co outperforms Ni and Cu for staging temperature at 140 °C for 24 h.

The feasibility study of generating indium solder and cobalt UBM barrier is performed in 20 μm pitch through resist pattern. Provided that can be reduced TCB temperature to realize high throughput and scaled micro bump stacking.

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- 1) E. Beyne, *IEEE Des. Test* **33**, 8 (2016).
- 2) L. Hou, J. Derakhshandeh, G. Capuz, E. Beyne, and I. D. Wolf, *IEEE Trans. Compon., Packag. Manuf. Technol.* **10**, 669 (2020).
- 3) Y. Tian, C. Liu, D. Hutt, and B. Stevens, *J. Electron. Mater.* **43**, 594 (2014).
- 4) Y. Qin et al., 2016 IEEE 66th Electronic Components and Technology Conf. (ECTC), 2016, p. 2151.
- 5) P. Merken, J. John, L. Zimmermann, and C. V. Hoof, *IEEE Trans. Adv. Packag.* **26**, 60 (2003).
- 6) J. Jiang, S. Tsao, T. O'Sullivan, M. Razeghi, and G. J. Brown, *Infrared Phys. Technol.* **45**, 143 (2004).
- 7) C. Broennimann, F. Glaus, J. Gobrecht, S. Heising, M. Horisberger, R. Horisberger, H. C. Kästli, J. Lehmann, T. Rohe, and S. Streuli, *Nucl. Instrum. Methods Phys. Res. A* **565**, 303 (2006).
- 8) S. Cihangir and S. Kwan, *Nucl. Instrum. Meth. A* **476**, 670 (2002), [in English].
- 9) A. Manasson, M. Bah, B. Desmarais, D. Douglass, C. Outten, J. Schumacher, M. Robinson, and C. Zhang, *Proc. SPIE* **10639**, 106392I (2018).
- 10) E. Szocs, F. Schwager, M. Toben, and N. Brese, 2008 2nd Electronics System-Integration Technology Conf. 2008, p. 347, DOI: [10.1109/ESTC.2008.4684373](https://doi.org/10.1109/ESTC.2008.4684373).
- 11) Q. Huang, G. Xu, G. Quan, Y. Yuan, and L. Luo, *J. Semicond.* **31**, 116004 (2010).
- 12) Y. Tian, C. Liu, D. Hutt, B. Stevens, D. Flynn, and M. P. Y. Desmulliez, 2009 11th Electronics Packaging Technology Conf., 2009, p. 31, DOI: [10.1109/EPTC.2009.5416576](https://doi.org/10.1109/EPTC.2009.5416576).
- 13) Q. Huang, G. Xu, and L. Luo, 2009 Int. Conf. on Electronic Packaging Technology & High Density Packaging, 2009, p. 650, DOI: [10.1109/ICEPT.2009.5270670](https://doi.org/10.1109/ICEPT.2009.5270670).
- 14) Q. Huang, G. Xu, Y. Yuan, X. Cheng, and L. Luo, *J. Micromech. Microeng.* **20**, 055035 (2010).
- 15) M. Volpert, L. Roulet, J. F. Boronat, I. Borel, S. Pocas, and H. Ribot, 2010 Proc. 60th Electronic Components and Technology Conf. (ECTC), 2010, p. 1739, DOI: [10.1109/ECTC.2010.5490736](https://doi.org/10.1109/ECTC.2010.5490736).
- 16) J. Coleman, A. Rowen, S. Mani, W. G. Yelton, C. Arrington, R. Gillen, A. Hollowell, D. Okerlund, and A. Ionescu, *Proc. SPIE* **7590**, 75900F (2010).
- 17) U. Lo Cicero, C. Arnone, M. Barbera, A. Collura, and G. Lullo, *J. Low Temp. Phys.* **167**, 535 (2012).
- 18) J. Son, Y. H. Kim, K. H. Kim, S. H. Kim, H. J. Im, N. H. Kim, and H. Jung, *Proc. SPIE* **11002**, 110022B (2019).
- 19) Y. Tian, D. A. Hutt, C. Liu, and B. Stevens, 2009 Int. Conf. on Electronic Packaging Technology & High Density Packaging, 2009, p. 456, DOI: [10.1109/ICEPT.2009.5270712](https://doi.org/10.1109/ICEPT.2009.5270712).
- 20) F. Inoue, K. Park, J. Derakhshandeh, and B. Yoo, 2021 7th Int. Workshop on Low Temperature Bonding for 3D Integration (LTB-3D), 2021, p. 31, DOI: [10.1109/LTB-3D53950.2021.9598451](https://doi.org/10.1109/LTB-3D53950.2021.9598451).
- 21) L. Hou et al., 2017 IEEE SOI-3D Microelectronics Unified Conf., S3S, 2017, DOI: [10.1109/S3S.2017.8309244](https://doi.org/10.1109/S3S.2017.8309244).
- 22) L. Hou, J. Derakhshandeh, E. Beyne, and I. D. Wolf, *IEEE Trans. Compon. Packag. Manuf. Technol.* **10**, 30 (2020).
- 23) W. Shao, G. Pattanaik, and G. Zangari, *J. Electrochem. Soc.* **154**, D201 (2007).
- 24) Q. Huang, K. Reuter, S. Amhed, L. Deligianni, L. T. Romankiw, S. Jaime, P. P. Grand, and V. Charrier, *J. Electrochem. Soc.* **158**, D57 (2011).
- 25) J. Derakhshandeh et al., 2021 IEEE 71st Electronic Components and Technology Conf. (ECTC), 2021, p. 1119, DOI: [10.1109/ECTC32696.2021.00183](https://doi.org/10.1109/ECTC32696.2021.00183).