Impact of the Channel Doping on the Low-Frequency Noise of Gate-All-Around Silicon Vertical Nanowire pFETs

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1. Abstract

In this work, the impact of the channel doping on the low-frequency noise of silicon Gate-All-Around (GAA) Vertical Nanowire (VNW) pMOSFETs on Silicon-on-Insulator (SOI) substrates will be described and discussed. It is demonstrated that the dominant fluctuation mechanism of the 1/f noise in weak inversion changes from mobility ($\Delta\mu$) to number (Δn) fluctuations with increasing doping density of the silicon nanowires. At the same time, the lowest input-referred voltage noise Power Spectral Density is observed for an intermediate boron concentration of 5×10^{18} cm^{-3}.

2. Introduction

Future CMOS technology nodes will rely on Gate-All-Around (GAA) FETs that ensure ultimate control over the short-channel effects [1]. In this class of devices, GAA Vertical Nanowires (VNWs) offer some clear integration advantages over horizontal architectures. While their integration requires a somewhat more complex processing scheme, these devices can be implemented in a 3D architecture, for example, as selectors in memory circuits [2]. When fabricating VNW transistors on a bulk silicon substrate, the latter serves at the same time as the source, using a backside contact. It has been shown that this leads to a clear asymmetry in the DC current-voltage characteristics [3] and, as shown more recently, also in the low-frequency (LF) noise performance [4-5]. For a true 3D implementation of VNW FETs, a separate source contact should be fabricated, not using the wafer backside as electrode. This can be emulated by starting from Silicon-on-Insulator (SOI) wafers and implementing a top source contact on the silicon film.

Another processing factor that deserves some attention is the doping density of the silicon nanowires, that are generally grown by Chemical Vapor Deposition (CVD) epitaxy. Undoped silicon NWs are usually slightly n-type, while in-situ doping with B or P yields p- or n-type wires. It has been shown in the past for horizontal NWs on SOI that a junctionless architecture may result in favorable DC and LF noise characteristics [6,7]. In addition, optimal noise performance has been demonstrated for medium doping density, in the range of 5×10^{18} cm^{-3} [7].

In this work, we will describe the impact of the channel doping on the low-frequency noise of junctionless (JL) silicon GAA VNW pMOSFETs on SOI, on its magnitude and the underlying fluctuation mechanisms.

3. Experimental details

The silicon VNWs with a diameter of ~26 nm and a gate length (defined vertically) of up to ~100 nm have been patterned on epitaxial films grown on 300 mm diameter SOI substrates. The effective gate length and

width are estimated 100 nm and 8.2 μm, respectively. The channels of these devices are either undoped (corresponding to intrinsic, undoped epitaxially grown Si layers) or in-situ B-doped; the doping concentration indicated by [B] was varied between 2×10^{18} cm^{-3} and 1×10^{19} cm^{-3}. In the latter case, a junctionless (JL) type of transistor structure was achieved by sandwiching the nanowires between 50 nm thick highly in-situ B-doped SiGe (25%) contact layers. The gate-first stack consists of IL-SiO_2/HfO_2/TiN/W with an Equivalent Oxide Thickness (EOT) of ~1.0 nm. A simplified schematic of these devices' configuration and an example of a Secondary Electron Microscopy (SEM) image obtained during their fabrication are shown in Fig. 1.

Low-frequency (LF) measurements have been executed on wafer in linear operation (V_{DS}=-0.05 V), with the gate voltage V_{GS} stepped from weak to strong inversion. The studied pFETs have 10 by 10 NWs in parallel, so in total 100 nanowires. The input-referred voltage noise Power Spectral Density (PSD) S_{VG} has been calculated from the drain current noise PSD (S_I) by dividing with g_m^2 in each bias point (g_m the device transconductance).

4. Results and Discussion

It has been shown that the LF noise spectra are predominantly 1/f-like [5]. This is illustrated by Fig. 2 for a JL p-type nanowire FETs with a [B] of 2×10^{18} cm^{-3}. From the frequency-normalized spectrum $f\times S_I$ it can be derived that there is also a small Lorentzian Generation-Recombination (GR) component present at higher frequencies (f>100 Hz). At the same time, it is shown that there is little asymmetry between the noise measurements in Forward (F) and Reverse (R) operation. In latter case, the roles of source and drain have been interchanged. This stands in contrast to the behavior of the GAA VNW pFETs on a bulk substrate where a clear asymmetry has been reported [4]. Evidently, the use of a top source contact removes this artefact.

According to the S_I versus drain current (I_D) in Fig. 3a, the noise PSD at 10 Hz increases roughly proportionally with I_D^2. This also follows from the normalized current noise PSD in Fig. 3b, exhibiting a plateau in weak inversion followed by a roll-off in strong inversion. This is typical for 1/f noise dominated by number

fluctuations [8-11] or Δn mechanism. The parallelism with the $(g_m/I_D)^2$ function confirms this idea. Again, no asymmetry is found in the 1/f noise PSD. The same can be concluded from the S_{VG} versus gate voltage. shown in Fig. 4. The increase at more negative V_{GS} indicates the higher impact of the parasitic access resistance on the 1/f noise [12,13].

Similar trends are observed for the undoped (UD) VNW pFETs, as can be derived from the normalized current noise PSD in Fig. 5a or the S_{VG} in Fig. 5b. In the first instance, there is no pronounced impact of the channel doping on the LF 1/f noise behavior for low [B]. Of course, there is an impact on the threshold voltage and maximum transconductance.

The picture changes when [B] becomes higher than 2×10^{18} cm^{-3}, as illustrated by Fig. 6). Here, the S_{VG} at 10 Hz for a set of VNW JL pFETs is shown with [B] $=5\times10^{18}$ cm^{-3}. In this case, a V-shaped dependence on gate voltage is observed, with a minimum occurring around the threshold voltage V_T. The difference is the clear roll-off of the 1/f noise PSD found in the subthreshold regime (higher V_{GS}). This indicates the presence of an additional flicker noise source with different, non-Δn origin. This picture is further confirmed by comparing the normalized drain current noise PSD with the $(g_m/I_D)^2$ function in Fig. 7a and 7b. A transition of the dominant 1/f noise mechanism from Δn at low [B] (also found for the undoped NWs) to $\Delta\mu$ for [B]$\geq5\times10^{18}$ cm^{-3} is observed. This indicates a change in the hole transport in the NW from near the Si/SiO_2 interface (low [B]) to along the nanowire core (high [B]). This is more clearly illustrated by the S_{VG} data of Fig. 8.

Finally, as can be observed in Fig. 9, the lowest average S_{VG} is found for [B]= 5×10^{18} cm^{-3}. This is very similar to what has been concluded for horizontal silicon GAA NWs on SOI substrates.

Fig. 10 and Fig. 11

5. Conclusions

The channel doping has a clear impact on the flicker noise of GAA VNW pMOSFETs on SOI by changing the noise PSD and the dominant fluctuation mechanism. This can be useful for optimizing the analog performance of such junctionless devices.

Acknowledgements

This work has been performed in the frame of imec's GAA Nanowire Core Partner Program.

References

[1] A. Veloso, G. Eneman, T. Huynh-Bao, A. Chasin, E. Simoen, E. Vecchio, K. Devriendt, S. Brus, E. Rosseel, A. Hikavyy, R. Loo, V. Paraschiv, B. T. Chan, D. Radisic, W. Li, J. J. Versluijs, L. Teugels, F. Sebaai, P. Favia, H. Bender, E. Vancoille, J. Scheerder, C. Fleischmann, N. Horiguchi, and P. Matagne, “Vertical nanowire and nanosheet FETs: device features, novel schemes for improved process control and enhanced mobility, potential for faster & more energy efficient circuits,” International Electron Devices Meeting, IEEE Xplore, pp. 230-233, Dec. 2019, https://doi.org/10.1109/IEDM19573.2019.8993602.

[2] A. Veloso, G. Eneman, A. De Keersgieter, D. Jang, H. Mertens, P. Matagne, E. Dentoni Litta, J. Ryckaert and N. Horiguchi, “Nanosheet FETs and their potential for enabling continued Moore’s law scaling,” in Proc. of the 5th IEEE Electron Devices Technol. & Manufact. Conf. (EDTM), IEEE Xplore, p. 1, May 2021, https://doi.org/10.1109/EDTM50988.2021.9420942.

[3] M. Liu, F. Lentz, S. Trellenkamp, J.-M. Hartmann, J. Knoch, D. Grützmacher, D. Buca, and Q.-T. Zhao, “Diameter scaling of vertical Ge Gate-All-Around nanowire pMOSFETs,” IEEE Trans. Electron Devices, vol. 67, pp. 2988-2994, Jul. 2020, https://doi.org/10.1109/TED.2020.2996183.

[4] E. Simoen, A. Veloso and P. Matagne, “On the asymmetry of the DC and low-frequency noise characteristics of vertical nanowire pMOSFETs with bulk source contact,” in: Proc. EUROSOI-ULIS 2021, IEEE Xplore, p. 1, Sep. 2021, https://doi.org/10.1109/EuroSOI-ULIS53016.2021.9560186.

[5] E. Simoen, P. Matagne, A. Veloso, and C. Claeys, “Impact of processing factors on the low-frequency noise of gate-all-around silicon vertical nanowire FETs,” ECS Trans., vol. 104, no. 3, pp. 3-13, Oct. 2021. https://doi: 10.1149/10404.0003ecst.

[6] E. Simoen, A. Veloso, P. Matagne, N. Collaert, and C. Claeys, “Junctionless versus inversion mode gate-all-around nanowire transistors from a low-frequency noise perspective,” IEEE Trans. Electron Devices, vol. 65, pp. 1487-1492, Apr. 2018, https://doi.org/10.1109/TED2018.2799617.

[7] E. Simoen, A. Vinicius Oliveira, A. Veloso, A. Chasin, R. Ritzenthaler, H. Mertens, N. Horiguchi, and C. Claeys, “Low frequency noise performance of horizontal, stacked and vertical silicon nanowire MOSFETs,” Solid-State Electron., vol. 184, p. 108087, 2021, https://doi.org/10.1016/j.sse.2021.108087.

[8] G. Ghibaudo, O. Roux, Ch. Nguyen-Duc, F. Balestra, and J. Brini. “Improved analysis of low frequency noise in field-effect MOS transistor”, Phys Status Solidi (a), vol. 124, pp. 571-81, 1991, https://doi.org/10.1002/pssa.2211240225.

[9] E. Simoen and C. Claeys, “On the flicker noise in submicron silicon MOSFETs”, Solid-State Electron., vol. 43, pp. 865-82, 1999, https://doi.org/10.1016/S0038 1101(98)00322.0.

[10] G. Ghibaudo and T. Boutchacha, “Electrical noise and RTS fluctuations in advanced CMOS devices,” Microelectron Reliab., vol. 42, pp. 573-82, 2002, https://doi.org/10.1016/S0026.2714(02)00025.2.

[11] E. Simoen, H.-C. Lin, A. G. Brammertz, C. Merckling, J. Mitard et al., “Border traps in Ge/III-V channel devices: analysis and reliability aspects”, IEEE Trans Device and Mater Reliability, vol. 13, pp. 444-55, 2013, https://doi.org/TDMR.2013.2275917.

[12] E. Vandamme, L.K.J. Vandamme, E. Simoen, R. Schreutelkamp, and C. Claeys, “The noise behavior of silicided and non-silicided MOSFETs,” Solid-State Electron., vol. 38, no. 11, pp. 1893-1897, Dec. 1995; https://doi.org/10.1016/0038-1101(95)00011-H.

[13] D. Boudier, B. Cretu, E. Simoen, R. Carin, A. Veloso, N. Collaert, and A. Thean, “Low frequency noise assessment in n- and p-channel sub-10 nm triple-gate FinFETs: Part II: Measurements and results,” Solid-State Electron., vol. 128, pp. 109-114, Feb. 2017; https://doi.org/10.1016/j.sse.2016.10.013.

Figure Captions

Figure 1: Schematic cross-section of a GAA VNW FET on SOI (a) and SEM image taken prior to the top electrode (TE) formation (b). BE=bottom electrode.

Figure 2: Drain current noise spectra in linear operation and for V_{GS}~V_T for a junctionless GAA VNW pFET and corresponding frequency-normalized ($f\times S_I$) spectra in forward and reverse operation. [B]=2×10^{18} cm^{-3}.

Figure 3: Drain current noise PSD at f=10 Hz in linear operation versus I_D and (b) corresponding normalized current noise PSD and $(g_m/I_D)^2$ of a junctionless GAA VNW pFET in forward and reverse operation. [B]=2×10^{18} cm^{-3}.

Figure 4: Input-referred voltage noise PSD at 10 Hz for a JL VNW pFET in Forward and Reverse operation at V_{DS}=-0.05 V. [B]=2×10^{18} cm^{-3}.

Figure 5: Normalized drain current (a) and input-referred voltage noise PSD (b) at 10 Hz for an undoped VNW pFET in Forward and Reverse operation at V_{DS}=-0.05 V.

Figure 6: Input-referred voltage noise PSD at 10 Hz for a JL VNW pFET in Forward and Reverse operation at V_{DS}=-0.05 V. [B]=5×10^{18} cm^{-3}.

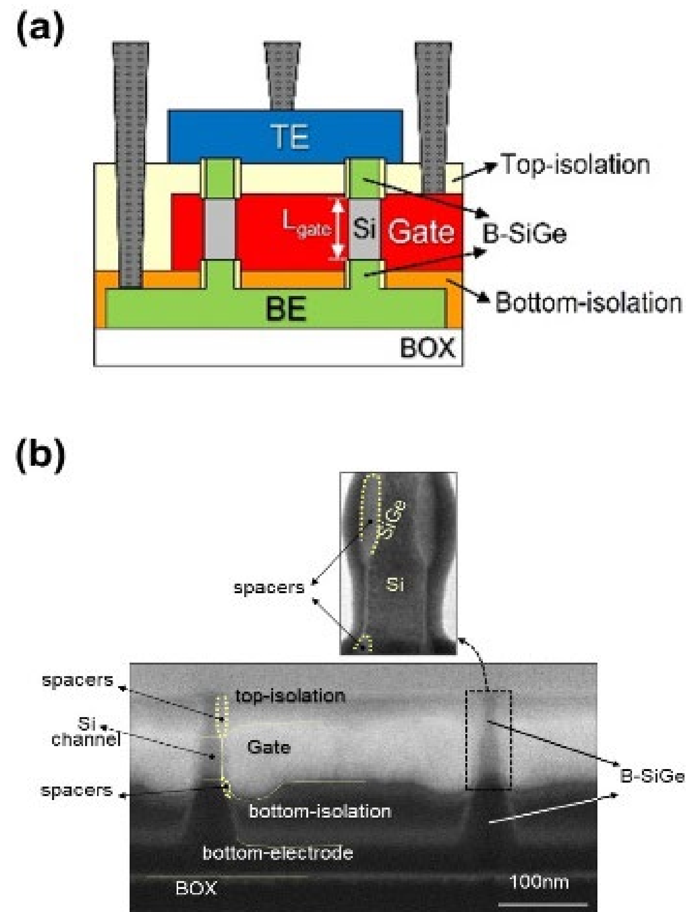
Figure 7: Normalized current noise PSD and $(g_m/I_D)^2$ versus absolute I_D in linear operation and f=10 Hz for a junctionless GAA VNW pFET with (a) [B]=2×10^{18} cm^{-3}; (b) [B]=5×10^{18} cm^{-3}.

Figure 8: Input-referred voltage noise PSD at 10 Hz for VNW pFETs with different channel doping, in linear operation at V_{DS}=-0.05 V.

Figure 9: Average S_{VG} at 10 Hz and V_{DS}=-0.05 V for GAA VNW pFETs with different [B].

Figure 10: Average S_{VG} at 10 Hz and V_{DS}=-0.05 V versus threshold voltage for GAA VNW pFETs with different [B].

Figure 11: Average S_{VG} at 10 Hz and V_{DS}=-0.05 V versus maximum transconductance for GAA VNW pFETs with different [B].



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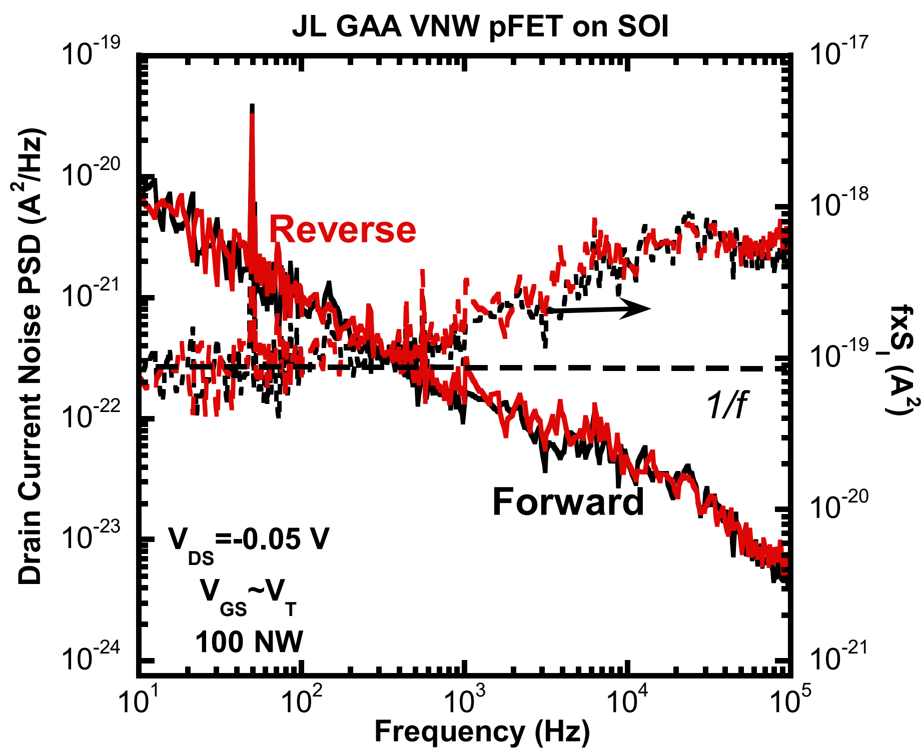

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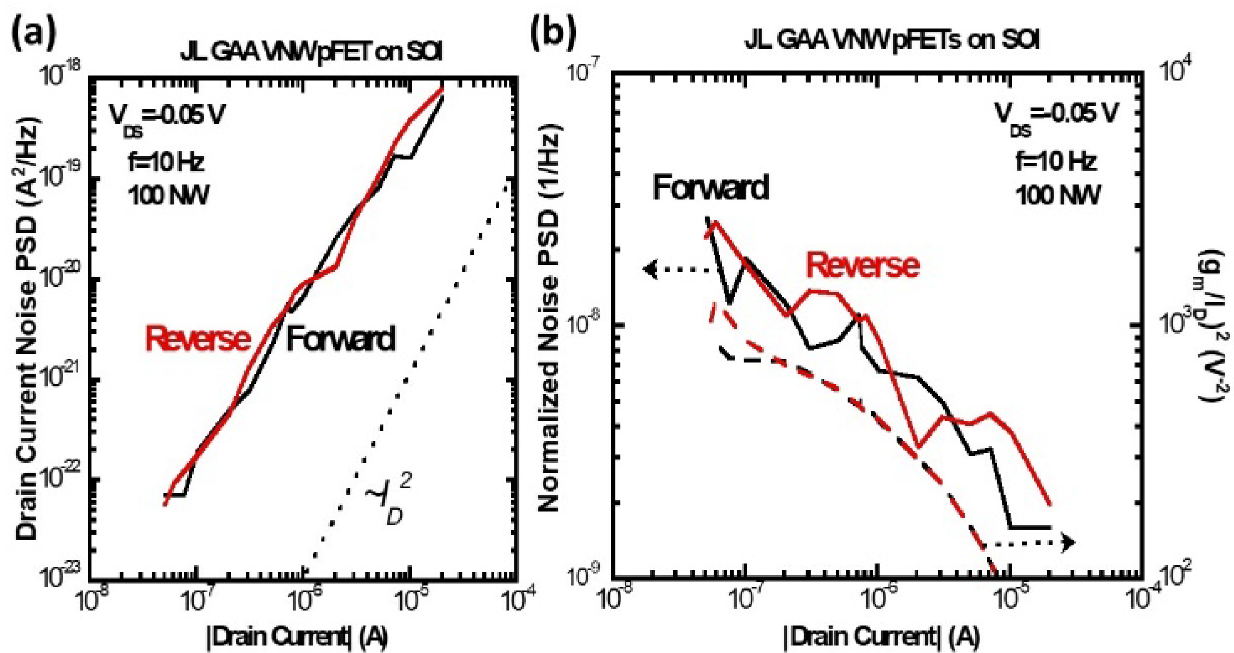

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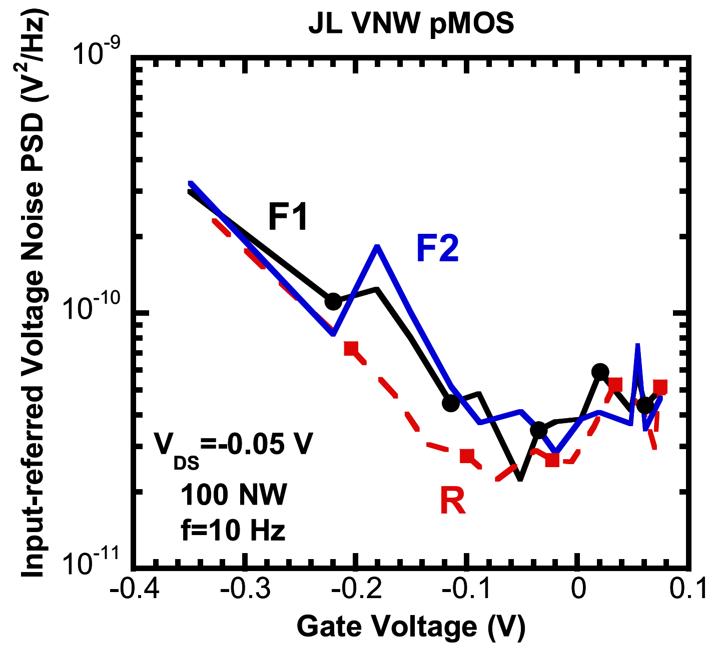
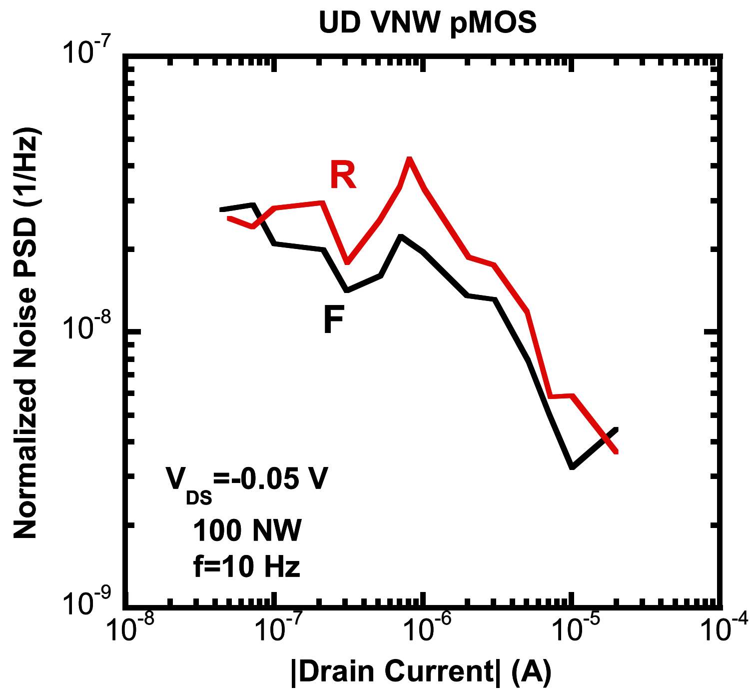
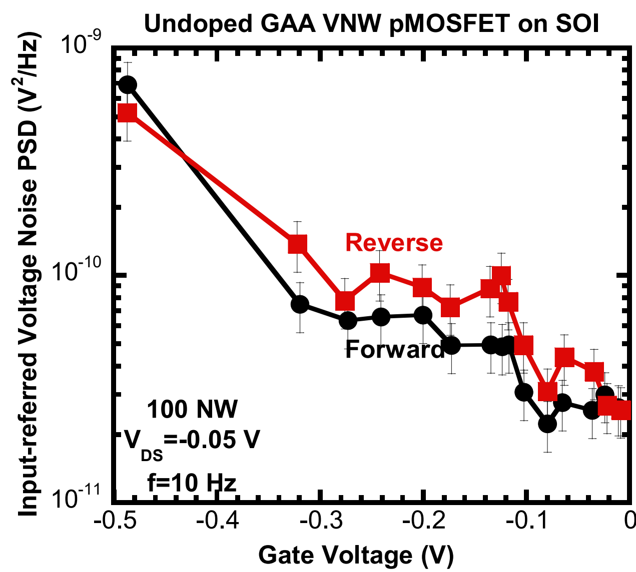


Figure 4: Input-referred voltage noise PSD at 10 Hz for a JL VNW pFET in Forward and Reverse operation at V_{DS}=-0.05 V. [B]=2×10^{18} cm^{-3}.



(a)



(b)

Figure 5: Normalized drain current (a) and input-referred voltage noise PSD (b) at 10 Hz for an undoped VNW pFET in Forward and Reverse operation at V_{DS}=-0.05 V.

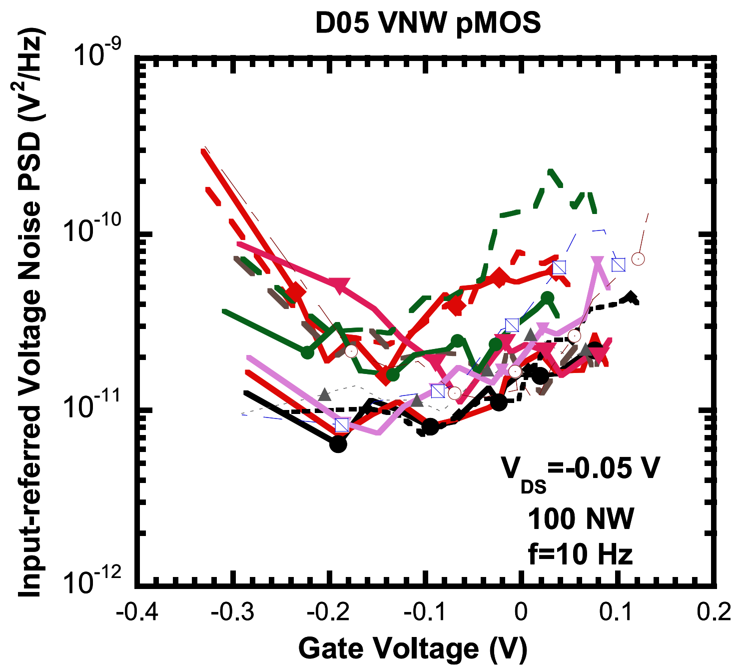


Figure 6: Input-referred voltage noise PSD at 10 Hz for a JL VNW pFET in Forward and Reverse operation at V_{DS}=-0.05 V. [B]=5×10^{18} cm^{-3}.

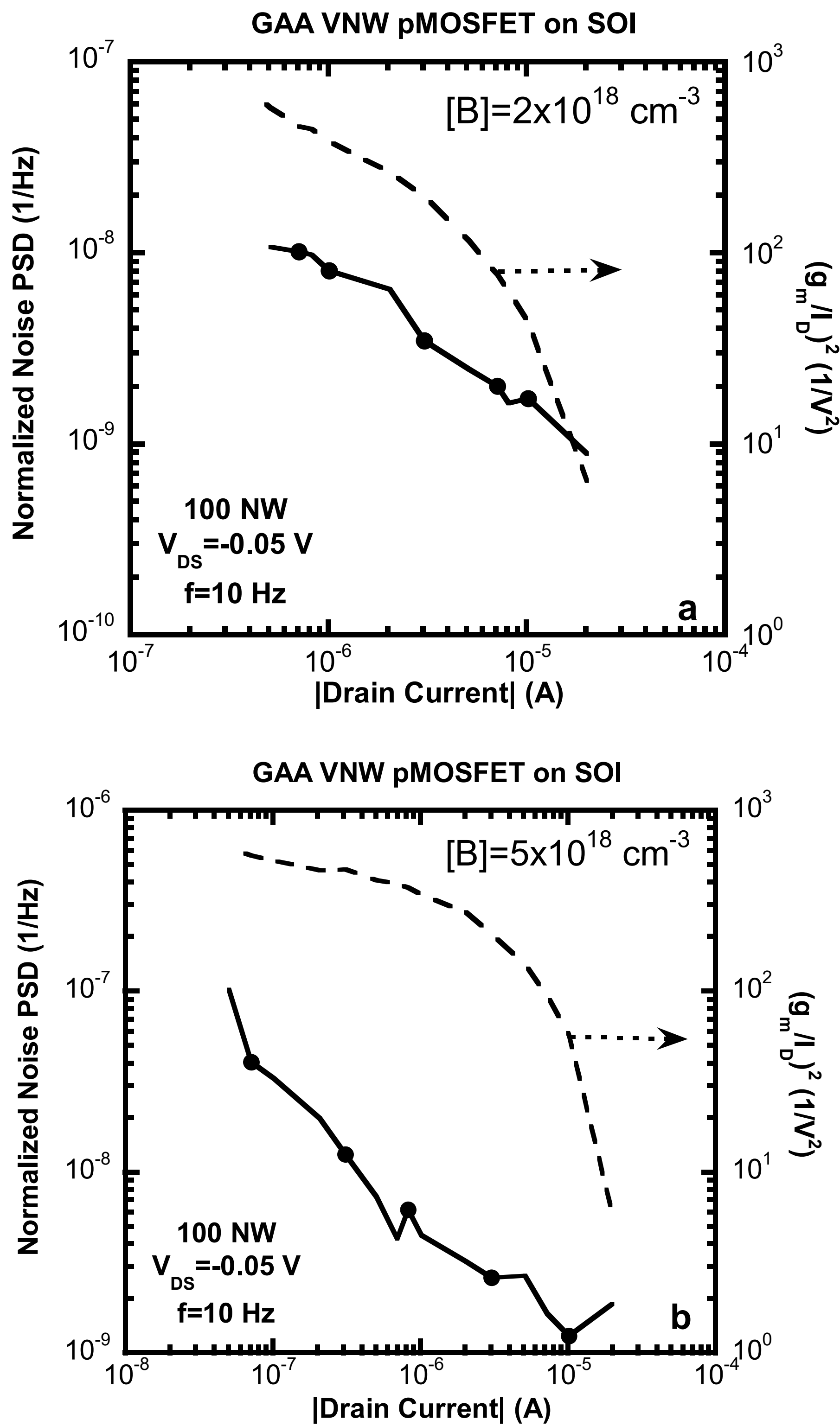
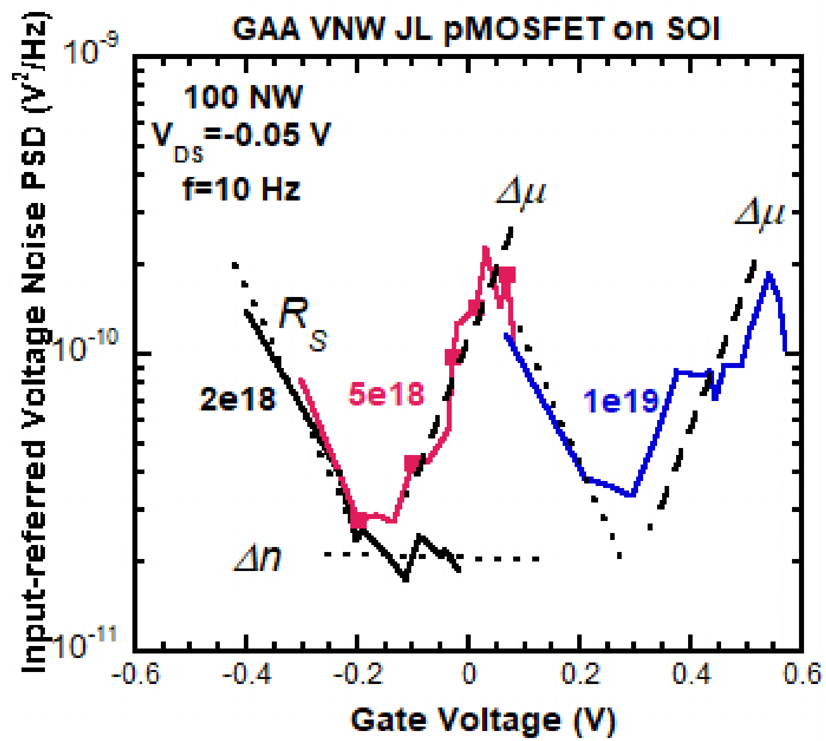


Figure 7: Normalized current noise PSD and $(g_m/I_D)^2$ versus absolute I_D in linear operation and f=10 Hz for a junctionless GAA VNW pFET with (a) $[B]=2\times10^{18}$ cm^{-3}; (b) $[B]=5\times10^{18}$ cm^{-3}.



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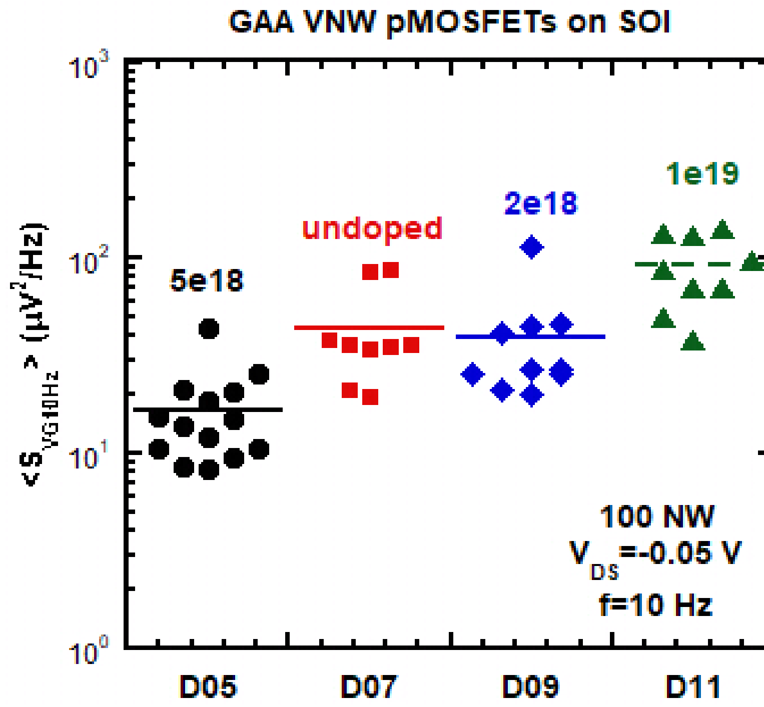

Figure 9: Average S_{VG} at 10 Hz and V_{DS}=-0.05 V for GAA VNW pFETs with different [B].

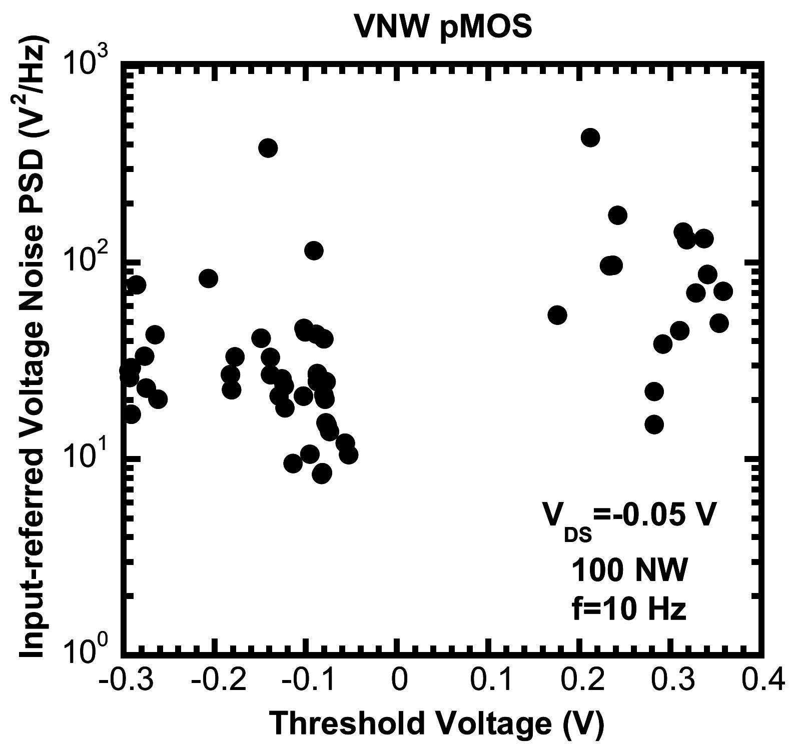

Figure 10: Average S_{VG} at 10 Hz and V_{DS}=-0.05 V versus threshold voltage for GAA VNW pFETs with different [B].

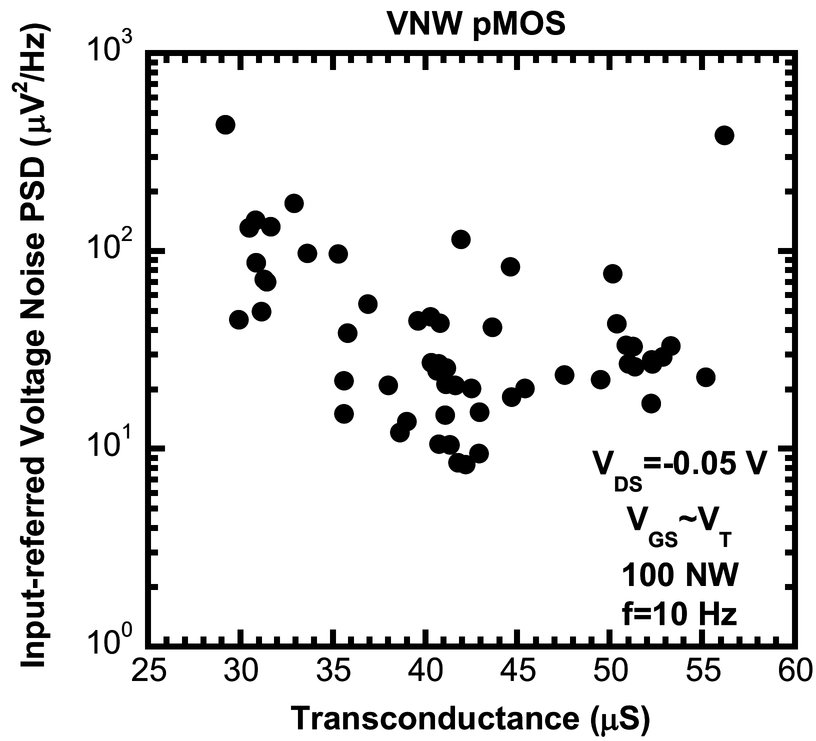

Figure 11: Average S_{VG} at 10 Hz and V_{DS}=-0.05 V versus maximum transconductance for GAA VNW pFETs with different [B].