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Distortion Cancellation in Asynchronous Sigma–Delta Modulators

Caro Meysmans, Achim Vandierendonck, *Graduate Student Member, IEEE*, Pieter Rombouts, *Senior Member, IEEE*, and Guy Torfs, *Senior Member, IEEE*

***Abstract*—This paper presents a design procedure for asynchronous sigma-delta modulators (ASDMs) that exploits distortion cancellation between the quantizer and the input path. By accurately matching the expansive nonlinearity of the quantizer to the compressive nonlinearity of the input path, the presented procedure relaxes input path linearity requirements, enabling power-efficient high-bandwidth designs. To support this procedure, a novel analytical model for first-order delay-based ASDMs is introduced that accurately characterizes the quantizer nonlinearity as a function of the loop filter corner frequency. Prior models assume a corner frequency much smaller than the self-oscillation frequency, limiting their applicability. The procedure is validated through the design of a 28 nm CMOS prototype. Operating at a self-oscillation frequency of 7.2 GHz, the prototype demonstrates distortion cancellation across a wide input amplitude range for frequencies within the loop filter bandwidth, while consuming only 3.1 mW from a 0.9 V supply.**

***Index Terms*—Inverter-based, CMOS, asynchronous sigma-delta modulator (ASDM), pulse-width modulator (PWM), distortion cancellation.**

I. Introduction

ASYNCHRONOUS sigma-delta modulators (ASDMs) do not introduce quantization noise when quantizing their input signal to a two-level output signal [1]. This makes them attractive for use at the input of analog-to-digital converters (ADCs) [2], [3], [4] and class-D power amplifiers [5], where they relax the input path linearity requirements. Additionally, when combined with a time-to-digital converter, ASDMs enable ADC architectures with most of their functionality in the digital domain [6], reducing area and power consumption.

A passive loop filter can be used to realize a highly linear input path [7]. As an alternative, we proposed to leverage the expansive nonlinearity of the quantizer to compensate for the compressive nonlinearity of the input path [8], relaxing input path linearity requirements. This approach requires an accurate match between the nonlinearity of the quantizer and the nonlinearity of the input path. However, existing analytical models [9], [10] fail to accurately predict the nonlinearity of this design due to the proximity of the required loop filter corner frequency to the oscillation frequency. To address this limitation, we present a novel analytical model that accurately predicts the nonlinearity of first-order delay-based ASDMs as a function of the corner frequency, after which we validate the model with the design of a prototype ASDM. Operating at a self-oscillation frequency of 7.2 GHz, the prototype demonstrates distortion cancellation across a wide input amplitude range for frequencies within the loop filter bandwidth, while consuming only 3.1 mW from a 0.9 V supply.

The remainder of this paper is organized as follows. Section II introduces asynchronous sigma-delta modulation and presents the proposed analytical model. Section III details the design of a prototype multi-GHz inverter-based ASDM based on this model. Experimental results from the fabricated prototype are presented in Section IV. Finally, Section V concludes the paper.

II. Asynchronous Sigma-Delta Modulation

The block diagram of a generic ASDM is shown in Fig. 1a. It is a closed-loop configuration with a continuous-time loop filter $G(j2\pi f)$, where the function g_u models the compressive nonlinear input path, and the gain g_v models the feedback path. The loop filter output is quantized by a quantizer (with hysteresis thresholds $\pm V_s$ and/or delay T_d) before being fed back to the loop filter input. Unlike synchronous sigma-delta modulators, the quantizer is not clocked. Instead, an ASDM exhibits a self-oscillation of which both the frequency and pulse width are modulated by the input signal, as shown in the time domain in Fig. 1b and in the frequency domain in Fig. 1. Consequently, the quantizer does not introduce quantization noise. Instead, the quantizer can be modeled as an odd, expansive nonlinear function q. Accordingly, the role of the loop filter shifts from shaping quantization noise to suppressing the nonlinearity of q.

Because of their possible simple circuit implementation, this paper focuses on delay-based ASDMs (i.e., $V_s = 0$) employing a first-order low-pass loop filter with frequency response

$$G(j2\pi f) = \frac{A}{1 + j\frac{f}{f_g}} \tag{1}$$

where A is the static gain and f_g is the corner frequency. The key parameter in their design is the ratio between the corner frequency and the self-oscillation frequency. Prior models [9], [10] assume that the corner frequency lies well below the

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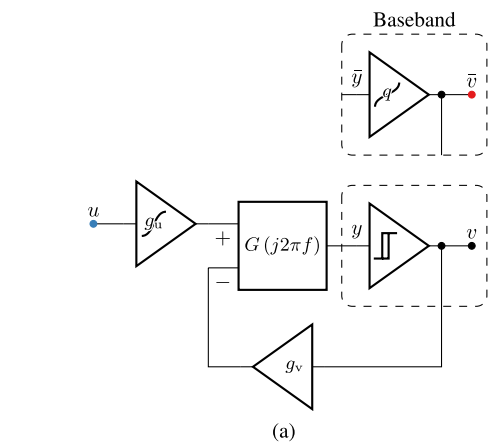
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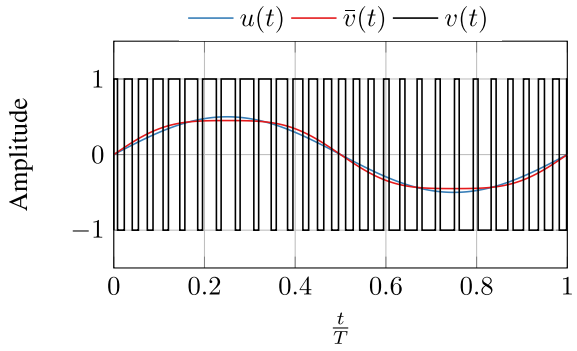
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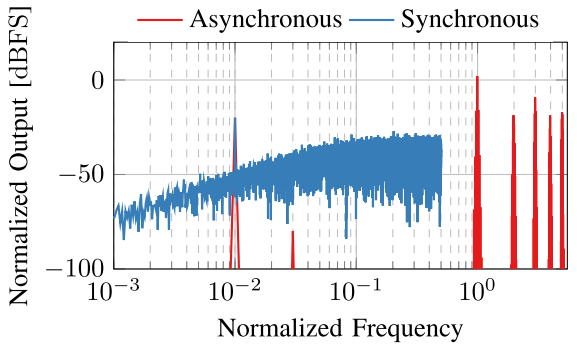
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(a)



(b)



(c)

Fig. 1. (a) Block diagram of a generic ASDM, and its baseband equivalent. (b) Time domain waveform of the normalized output signal v, and its baseband component $\bar{v}$ (no carrier and its sidebands), for a sinusoidal input signal u. (c) Comparison of the normalized output spectrum of an asynchronous sigma-delta modulator and a synchronous sigma-delta modulator, for a sinusoidal input signal.

self-oscillation frequency, limiting their validity when the ratio approaches one.

In this section, we derive novel expressions for first-order delay-based ASDMs, without making any assumptions on the corner frequency. Next, we evaluate the proposed model against simulation results and the prior work in [10]. Finally, we investigate the impact of input path nonlinearity and how to compensate it.

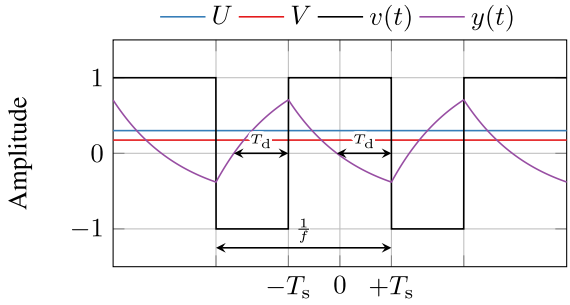


Fig. 2. Example waveforms of a first-order delay-based ASDM for a static input. Signal definitions follow Fig. 1a. The quantizer switches at $\pm T_s$. This example ASDM has a gain smaller than 1, i.e., $V < U$.

A. Analytical Model

As depicted in Fig. 1a, the loop filter output y for a static input is given by:

$$y = \left[g_u(U) - g_v v\right] * g \tag{2}$$

Here, U is the static input value, v is the normalized ASDM output, g is the loop filter impulse response, and $*$ denotes convolution.

The normalized ASDM output v is a square wave toggling between ± 1, with frequency f and average value V, where $|V| \leq 1$. It can be expressed as a Fourier series expansion:

$$v(t) = V + \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin\left(n\pi\frac{V+1}{2}\right)\cos\left(2\pi n f t\right) \tag{3}$$

Substituting Eq. 3 into Eq. 2 yields:

$$y(t) = \left[g_u(U) - g_v V\right]G(0) - g_v\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin\left(n\pi\frac{V+1}{2}\right)\cdot \Re\left\{G(j2\pi n f)\exp\left(j2\pi n f t\right)\right\} \tag{4}$$

From Fig. 2, we observe that $y(\mp T_s - T_d) = 0$, where $\mp T_s$ denotes the time at which the quantizer switches, leading to the following set of equations:

$$0 = \left[g_u(U) - g_v V\right]G(0) - g_v\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin\left(n\pi\frac{V+1}{2}\right) \cdot \Re\left\{G(j2\pi n f)\exp\left[j2\pi n f(-T_s - T_d)\right]\right\} \tag{5}$$

$$0 = \left[g_u(U) - g_v V\right]G(0) - g_v\frac{4}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin\left(n\pi\frac{V+1}{2}\right) \cdot \Re\left\{G(j2\pi n f)\exp\left[j2\pi n f(+T_s - T_d)\right]\right\} \tag{6}$$

Subtracting and adding Eqs. 5 and 6 results in the following new set of equations:

$$0 = p^{-1}(V, f) \tag{7}$$

$$\left[g_u(U) - g_v V\right]G(0) = q^{-1}(V, f) \tag{8}$$

with:

$$p^{-1}(V, f) = g_v\frac{2}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\left[(-1)^n\cos\left(n\pi V\right) - 1\right] \cdot \Im\left\{G(j2\pi n f)\exp\left(-j2\pi n f T_d\right)\right\} \tag{9}$$

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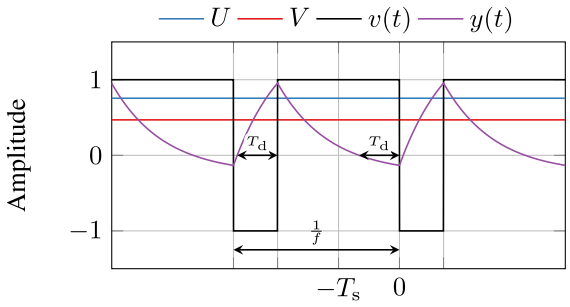


Fig. 3. Example waveforms of a first-order delay-based ASDM for a static input close to the maximum.

$$q^{-1}(V,f) = g_v \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{1}{n}(-1)^n \sin(n\pi V) \cdot \Re\left\{G(j2\pi nf)\exp(-j2\pi nfT_d)\right\} \quad (10)$$

The real and imaginary components of the frequency response, defined in Eq. 1, are given by:

$$\Re\{G(j2\pi f)\} = +\frac{A}{1+\left(\frac{f}{f_g}\right)^2} \quad (11)$$

$$\Im\{G(j2\pi f)\} = -\frac{A\left(\frac{f}{f_g}\right)}{1+\left(\frac{f}{f_g}\right)^2} \quad (12)$$

Substituting Eqs. 11 and 12 into Eqs. 9 and 10 yields the following expressions:

$$p^{-1}(V,f) = +g_v A \cdot \left[1 - \exp\left(2\pi f_g T_d\right)\frac{\cosh\left(\pi\frac{f_g}{f}V\right) - \exp\left(-\pi\frac{f_g}{f}\right)}{\sinh\left(\pi\frac{f_g}{f}\right)}\right] \quad (13)$$

$$q^{-1}(V,f) = -g_v A \cdot \left[V - \exp\left(2\pi f_g T_d\right)\frac{\sinh\left(\pi\frac{f_g}{f}V\right)}{\sinh\left(\pi\frac{f_g}{f}\right)}\right] \quad (14)$$

where we have used the trigonometric series listed in the appendix.

Convergence of the series requires

$$\frac{1}{f} \geq T_d \quad \text{and} \quad |V| \leq 1 - 2\,fT_d \quad (15)$$

As observed in Fig. 2, the first condition is always satisfied. The second condition demonstrates the limiting effect of the quantizer delay on the output swing. Using $V = 4\,fT_s - 1$, i.e., the average value, the second condition becomes:

$$T_d \leq 2T_s \leq \frac{1}{f} - T_d. \quad (16)$$

The upper bound of Eq. 16 is illustrated in Fig. 3, while the lower bound can be illustrated analogously.

Plugging Eq. 13 into Eq. 7 yields:

$$1 = \exp\left(2\pi f_g T_d\right)\frac{\cosh\left(\pi\frac{f_g}{f}V\right) - \exp\left(-\pi\frac{f_g}{f}\right)}{\sinh\left(\pi\frac{f_g}{f}\right)} \quad (17)$$

This implicit equation describes the relationship between the average output value V and the self-oscillation frequency f.

Although Eq. 17 does not admit a closed-form solution for f, the Taylor series coefficients $f_n = \frac{1}{n!}\frac{d^n f}{dV^n}\big|_{V=0}$ can be determined analytically via implicit differentiation. Due to the even symmetry of the system, all odd coefficients are zero. The first two non-zero coefficients are given by:

$$f_0 = +\pi f_g \frac{1}{\ln(1+\mu)} \quad (18)$$

$$f_2 = -\pi f_g \left(\frac{1}{2} + \mu^{-1}\right) \quad (19)$$

Here, the design parameter $\mu = 2\left[\exp\left(2\pi f_g T_d\right) - 1\right]$ is introduced to simplify the resulting expressions. Finally, the solution of Eq. 17 can be approximated by:

$$f \approx \pi f_g \frac{1}{\ln(1+\mu)}\left[1 - \left(\frac{1}{2} + \mu^{-1}\right)\ln(1+\mu)V^2\right] \quad (20)$$

These two Taylor series coefficients are sufficient to characterize the third-order nonlinearity, as demonstrated next.

Plugging Eq. 14 into Eq. 8 yields:

$$g_u(U) = g_v \exp\left(2\pi f_g T_d\right)\frac{\sinh\left(\pi\frac{f_g}{f}V\right)}{\sinh\left(\pi\frac{f_g}{f}\right)} \quad (21)$$

This implicit equation describes the static input value U as a function of the average output value V and the self-oscillation frequency f.

To evaluate the nonlinearity, we determine the Taylor series coefficients $V_n = \frac{1}{n!}\frac{d^n V}{dU^n}\big|_{U=0}$.

$$V_1 = \frac{g_{u1}}{g_v}\frac{1}{\left(1+\mu^{-1}\right)\ln(1+\mu)} \quad (22)$$

$$V_2 = \frac{g_{u2}}{g_{u1}}V_1 \quad (23)$$

$$V_3 = \frac{g_{u3}}{g_{u1}}V_1 + \left[\left(\frac{1}{3} + \mu^{-1} + \mu^{-2}\right)\ln(1+\mu)^2 - \left(\frac{1}{2} + \mu^{-1}\right)\ln(1+\mu)\right]V_1^3 \quad (24)$$

where $g_{un} = \frac{1}{n!}\frac{d^n g_u}{dU^n}\big|_{U=0}$ are the Taylor series coefficients of the input path nonlinearity.

Assuming no third-order input path nonlinearity, i.e., $g_{u3} = 0$, the RMS output-referred third-order intercept point $A_{oip3,q}$ is given by:

$$\frac{A_{oip3,q}^2}{2} = \left[\left(\frac{1}{3} + \mu^{-1} + \mu^{-2}\right)\ln(1+\mu)^2 - \left(\frac{1}{2} + \mu^{-1}\right)\ln(1+\mu)\right]^{-1} \quad (25)$$

Assuming no quantizer nonlinearity, i.e., $\mu = 0$, the RMS output-referred third-order intercept point A_{oip3,g_u} is given by:

$$\frac{A_{oip3,g_u}^2}{2} = \left|V_1^2\frac{g_{u1}}{g_{u3}}\right| \quad (26)$$

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Finally, assuming both nonlinearities are present, the overall RMS output-referred third-order intercept point A_{oip3} is given by:

$$\frac{1}{A_{\text{oip3}}^2} = \text{sgn}\left(\frac{g_{\text{u3}}}{g_{\text{u1}}}\right)\frac{1}{A_{\text{oip3},g_{\text{u}}}^2} + \frac{1}{A_{\text{oip3},q}^2} \tag{27}$$

B. Evaluation

To evaluate the proposed model, we simulate an ideal first-order delay-based ASDM for a range of frequency ratios $\frac{f_{\text{g}}}{f}$. First, the simulator[1] employed in this work is introduced. Next, we compare the simulation results with the proposed analytical expressions and the analytical expressions from [10], assuming no input path nonlinearity. Finally, we investigate the impact of input path nonlinearity.

1) Simulator: The goal of the simulator is to accurately determine the quantizer switching times T_{sn} for a general input signal of the form

$$u(t) = u_0 + \sum_{n=1}^{\infty} \Re\left\{u_n \exp\left(j2\pi n f_{\text{u}} t\right)\right\}, \tag{28}$$

where u_0 corresponds to the input static component and u_n denotes the phasor of the input sinusoidal component at frequency nf_{u}.

Between two switching times, i.e., $T_{sn} < t < T_{s(n+1)}$, the loop filter output is given by:

$$y(t) = y_{\text{u}}(t) + y_{\text{v}}(t) + y_{\text{y}}(t) \tag{29}$$

The first component is the steady-state response due to the input:

$$y_{\text{u}}(t) = Au_0 + \sum_{n=1}^{\infty} \Re\left\{\frac{A}{1 + j\frac{nf_{\text{u}}}{f_{\text{g}}}} u_n \exp\left(j2\pi n f_{\text{u}} t\right)\right\} \tag{30}$$

The second component is the step response due to the output switching at T_{sn}:

$$y_{\text{v}}(t) = -v(T_{sn}^{+})\left[1 - \exp\left(-\frac{t - T_{sn}}{\tau}\right)\right] \tag{31}$$

The third component is the natural response due to the initial conditions:

$$y_{\text{y}}(t) = \left[y_{\text{y}}(T_{sn}) + y_{\text{v}}(T_{sn})\right]\exp\left(-\frac{t - T_{sn}}{\tau}\right) \tag{32}$$

The next switching time $T_{s(n+1)}$ is found by numerically solving the transcendental equation $y(T_{s(n+1)} - T_{\text{d}}) = 0$ using a root-finding algorithm. This procedure is repeated to find all subsequent switching times.

With the switching times known, the baseband output $\bar{v}(t)$ can be obtained using:

$$\bar{v}(t) = 2\sum_{n=0}^{\infty}(-1)^n \cdot h_{\text{demod}}\left(t - T_{sn}\right) - 1 \tag{33}$$

where $h_{\text{demod}}(t)$ is the step response of a unity gain low-pass filter.

[1]The source code is available at https://github.com/cameysma/delta-sigma-simulator/

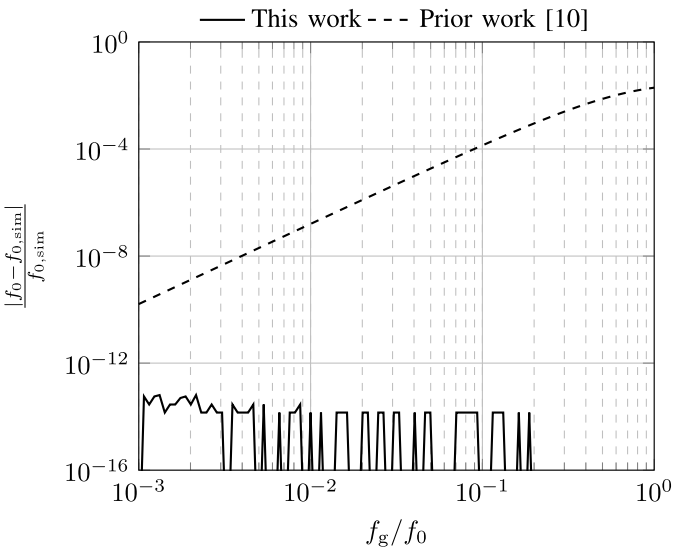


Fig. 4. Relative error between the estimated self-oscillation frequency f_0 = 1 Hz and the simulated value $f_{0,\text{sim}}$ as a function of the frequency ratio $\frac{f_{\text{g}}}{f_0}$ for the derived model (solid lines) and the prior work [10] (dashed lines).

Compared to traditional simulators, this approach avoids numerical errors due to finite time step sizes. Additionally, directly sampling the baseband output $\bar{v}(t)$ prevents aliasing of out-of-band components, which would otherwise occur when sampling $v(t)$ at a finite rate.

2) Simulation Results: For the next simulations, the parameters were set to $g_{\text{u1}} = g_{\text{v}} = 1$, $g_{\text{u2}} = g_{\text{u3}} = 0$ and $A = 1$, while T_{d} was selected to obtain an estimated self-oscillation frequency $f_0 = 1$ Hz, according to Eq. 18, for the specified f_{g}.

We first examine the relative error between the estimated self-oscillation frequency $f_0 = 1$ Hz and the simulated value $f_{0,\text{sim}}$ as a function of the frequency ratio $\frac{f_{\text{g}}}{f_0}$. As shown in Fig. 4, the proposed model accurately predicts f_0 over loop filter corner frequencies, while prior work [10] becomes inaccurate for corner frequencies close to the self-oscillation frequency.

Fig. 5 analyzes the self-oscillation frequency f as a function of the average output value V for a frequency ratio $\frac{f_{\text{g}}}{f_0} = 1$. At such a high frequency ratio, the response deviates significantly from the quadratic $1 - V^2$ relationship reported in [10].

Next, we compare the OIP3 as a function of the frequency ratio $\frac{f_{\text{g}}}{f_0}$. As shown in Fig. 6, the proposed model accurately predicts the OIP3 over loop filter corner frequencies, while prior work [10] overestimates the OIP3 for corner frequencies close to the self-oscillation frequency. Although not immediately clear from Eq. 25, the OIP3 exhibits an approximately linear dependence on the frequency ratio, with a slope of 20 dB/dec.

Finally, we investigate the impact of the input path nonlinearity. As shown in Eq. 27, when the input path nonlinearity is compressive, i.e., $\text{sgn}\left(\frac{g_{\text{u3}}}{g_{\text{u1}}}\right) < 0$, the nonlinearities of the quantizer and the input path (partially) cancel, thereby significantly improving the OIP3. This is illustrated in Fig. 7, where the OIP3 is plotted as a function of the frequency

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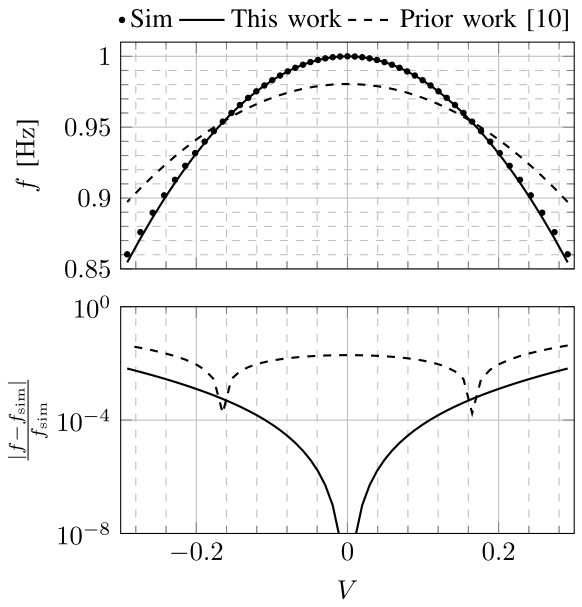


Fig. 5. Comparison of the self-oscillation frequency f as a function of the average output value V for a frequency ratio $\frac{f_g}{f_0} = 1$ for the derived model (solid lines) and the prior work [10] (dashed lines). The dots represent the simulation results.

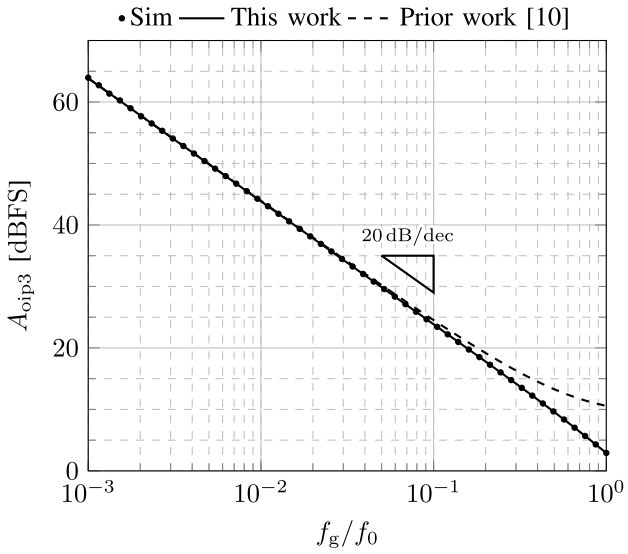


Fig. 6. Comparison of the OIP3 as a function of the frequency ratio $\frac{f_g}{f_0}$ for the derived model (solid lines) and the prior work [10] (dashed lines). The dots represent the simulation results.

ratio $\frac{f_g}{f_0}$. In this example, the third-order nonlinearity of the quantizer is completely compensated by that of the input path, resulting in an infinite OIP3, for a frequency ratio of $\frac{f_g}{f_0} = 10^{-2}$. At $\frac{f_g}{f_0} \ll 10^{-2}$, the OIP3 is dominated by the input path nonlinearity, while at $\frac{f_g}{f_0} \gg 10^{-2}$, the OIP3 is dominated by the quantizer nonlinearity. The dots represent the simulation results, which agree with Eq. 27.

The derivation leading to Eq. 27 assumes a static input signal, i.e., $f_u = 0$. In practice, however, the input signal has a non-zero frequency. We therefore investigate its impact by simulating the OIP3 as a function of the input frequency f_u for a frequency ratio $\frac{f_g}{f_0} = 10^{-2}$, as illustrated in Fig. 8. In addition,

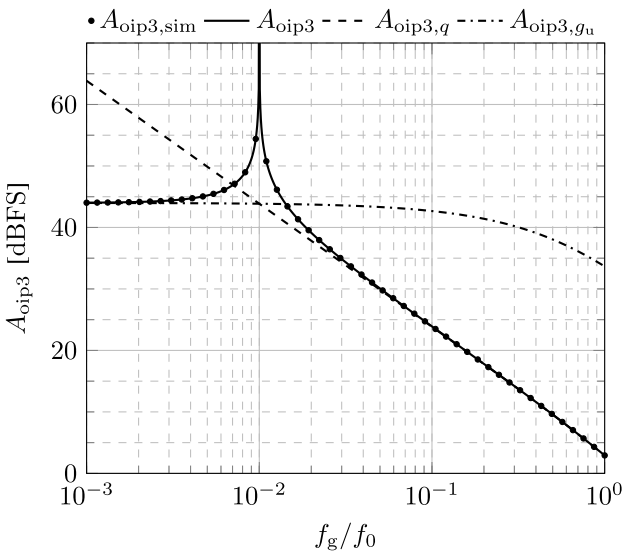


Fig. 7. Example of the quantizer nonlinearity and the input path nonlinearity compensating each other for a frequency ratio $\frac{f_g}{f_0} = 10^{-2}$. Signal definitions follow Eq. 27. The dots represent the simulation results.

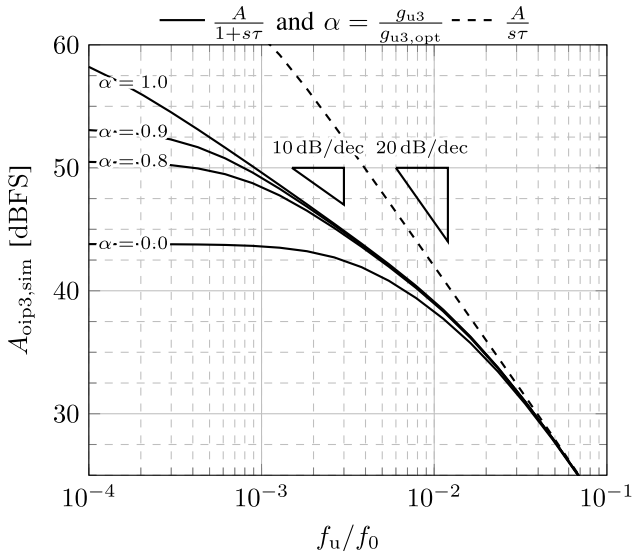


Fig. 8. Simulated OIP3 versus input frequency and $\alpha = \frac{g_{u3}}{g_{u3,opt}}$, for a frequency ratio $\frac{f_g}{f_0} = 10^{-2}$. At $\alpha = 1$, the quantizer nonlinearity compensates the input path nonlinearity for static inputs. The dashed line corresponds to an ASDM without input path nonlinearity and with an integrating loop filter with gain $2\pi f_g$.

we vary the input path nonlinearity by sweeping $\alpha = \frac{g_{u3}}{g_{u3,opt}}$, where $g_{u3,opt}$ is the value of g_{u3} that optimizes the OIP3 for a static input signal. For reference, we also include the case corresponding to an ASDM with an ideal integrating loop filter with gain $2\pi f_g$. At $\alpha = 0$, i.e., no input path nonlinearity, the OIP3 is approximately constant for $f_u \ll f_g$ and decreases with 20 dB/dec for $f_u \gg f_g$. At $\alpha = 1$, i.e., the input path nonlinearity completely compensates the quantizer nonlinearity for static inputs, the OIP3 is significantly improved for $f_u \ll f_g$ and decreases with [per-mode=symbol]10dB/. For $f_u \gg f_g$, the OIP3 is dominated by the quantizer nonlinearity and decreases with 20 dB/dec. For the ASDM with an ideal integrating loop filter and no input path nonlinearity, the OIP3 decreases with 20 dB/dec over the entire frequency range.

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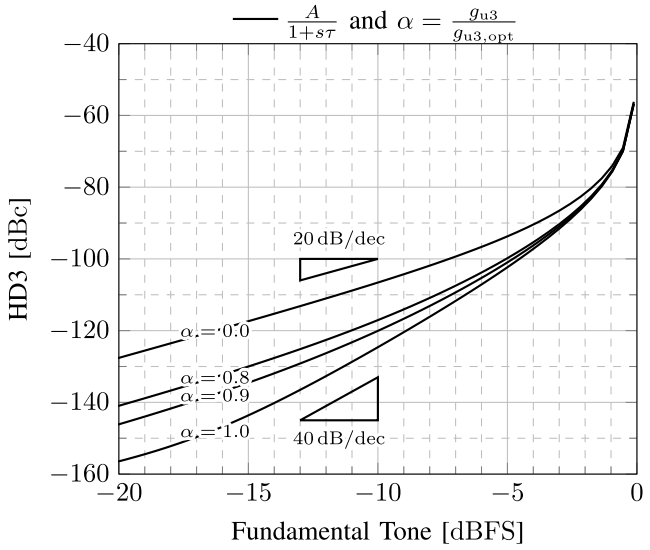


Fig. 9. Simulated HD3 as a function of the amplitude of the fundamental tone and $\alpha = \frac{g_{u3}}{g_{u3,opt}}$, for a frequency ratio $\frac{f_g}{f_0} = 10^{-2}$ and $\frac{f_u}{f_0} = 10^{-4}$. At $\alpha = 1$, the quantizer nonlinearity compensates the input path nonlinearity for static inputs.

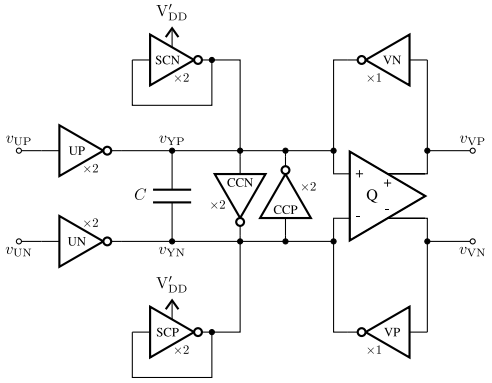


Fig. 10. Circuit diagram of the implementation.

Finally, we investigate the impact of the input signal amplitude. We therefore simulate the third-order harmonic distortion (HD3) as a function of the amplitude of the fundamental tone for a frequency ratio $\frac{f_g}{f_0} = 10^{-2}$ and $\frac{f_u}{f_0} = 10^{-4}$, as illustrated in Fig. 9. We again sweep the input path nonlinearity parameter α. At $\alpha = 0$, the HD3 is dominated by third-order terms and increases with 20 dB/dec. At $\alpha = 1$, the HD3 is significantly improved and becomes dominated by fifth-order terms, increasing with 40 dB/dec.

III. Implementation

The circuit diagram of the implementation is presented in Fig. 10. By using only inverters, the circuit is compatible with the decreasing supply voltage of aggressively scaled CMOS technologies, while it simultaneously benefits from the improvements in switching speed and power efficiency.

For high speed operation, a Gm-RC low-pass filter is used to implement the loop filter. Both the input and feedback transconductor are implemented using a Nauta transconductor [11]. A Nauta transconductor is a differential

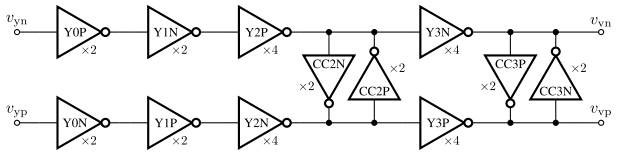


Fig. 11. Circuit diagram of the quantizer.

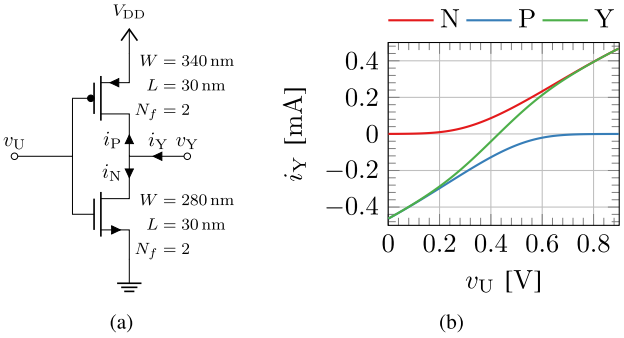


Fig. 12. (a) Circuit diagram of the unit inverter. W, L, and N_f denote the preshrink width, length, and number of fingers, respectively. (b) Simulated large-signal behavior of the unit inverter.

circuit comprising an input inverter pair (UP, UN) loaded by a cross-coupled inverter pair (CCP, CCN) and a self-coupled inverter pair (SCP, SCN). Since both the input and feedback transconductor share the same output, the cross-coupled and self-coupled inverter pair can be shared [12], saving both area and power. The output impedance of the Nauta transconductors is used to realize R, while the capacitance C is realized using a MOM-type capacitor and the parasitic capacitances of the inverters. Together they realize the desired corner frequency for optimal linearity. The separate supply voltage of the self-coupled inverter pair allows the loop filter corner frequency to be adjusted to guarantee distortion cancellation over process, voltage, and temperature variations.

The quantizer comprises a cascade of pseudo-differential inverters, as shown in Fig. 11. A total of four paths was selected to obtain a sufficiently large gain. The last path comprises four unit inverters to provide sufficient drive strength. The first path comprises only two unit inverters. For the intermediate paths, the number of unit inverters was chosen to minimize the overall propagation delay. Finally, a delay of 23 ps could be obtained.

In what follows, the unit inverter, serving as the fundamental building block, is introduced and characterized. After which the capacitance C required for optimal linearity is derived using the model presented in Section II.

A. Unit Inverter

The circuit diagram of the unit inverter is depicted in Fig. 12a. W, L, and N_f denote the preshrink width, length, and number of fingers, respectively. The unit inverter employs minimum length transistors with ultra-low threshold voltage to achieve high-speed operation. The lower mobility of the PMOS transistor is compensated by making its width 1.2 times that of the NMOS transistor.

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Deep submicron transistors deviate significantly from the square-law model due to second-order effects like mobility reduction and channel length modulation. These effects are difficult to capture in simple design equations. Hence, Taylor series expansions based on the simulated large-signal behavior, shown in Fig. 12b, are used to characterize the device behavior.

For small input voltage variations, the output current i_y is given by:

$$i_y = \sum_{n=0}^{\infty} g_{msn} v_u^n + \frac{v_y}{r_{os}} \tag{34}$$

with:

$$g_{msn} = \frac{1}{n!} \frac{d^n i_Y}{dv_U^n}\bigg|_{\substack{v_U=V_U \\ v_Y=V_Y}} \quad \text{and} \quad \frac{1}{r_{os}} = \frac{di_Y}{dv_Y}\bigg|_{\substack{v_U=V_U \\ v_Y=V_Y}} \tag{35}$$

Here, v_u, v_y, and i_y denote the input voltage, output voltage, and output current variations around the static values V_U, V_Y, and I_Y, respectively. The nonlinearity of the output resistance and the mixed terms $v_u^n v_y^m$ are omitted due to their negligible impact on the performance.

For a fullscale square wave input, e.g., the output of the ASDM, the output current i_y is perfectly linear and given by:

$$i_y = g_{ml} v_u + \frac{v_y}{r_{ol}} \tag{36}$$

with:

$$g_{ml} = \frac{i_Y(V_{DD}, V_Y) - i_Y(0, V_Y)}{V_{DD}} \tag{37}$$

and:

$$r_{ol} = \frac{r_{os}(V_{DD}, V_Y) + r_{os}(0, V_Y)}{2} \tag{38}$$

Fig. 13 summarizes the first three small-signal transconductance coefficients g_{msn}, and the output resistance r_{os} as a function of the static input voltage V_U. The supply voltage V_{DD} is 0.9 V, and the static output voltage V_Y is set to half the supply voltage. Although there are two static input voltages which provide optimal third-order linearity, a static input voltage of half the supply voltage is chosen, to minimize the static output current. This yields a small-signal transconductance g_{ms1} of 1.36 mS, g_{ms3} of -3.32 mS/A^2, and an output resistance r_{os} of 5.06 kΩ. For a fullscale square wave input, the transconductance g_{ml} is 1.04 mS, and the output resistance r_{ol} is 2.70 kΩ.

B. Optimal Linearity

Using the small-signal and square-wave descriptions of the unit inverter, the parameters of the model presented in Section II and the resulting nonlinearity can be calculated.

The input and feedback path are described by:

$$g_{u(2n+1)} = \frac{g_{ms(2n+1)}}{2^{2n}} \quad \text{and} \quad g_v = \frac{g_{ml}}{2} V_{DD} \tag{39}$$

Due to the differential operation, the even-order coefficients vanish.

The loop filter DC gain A and corner frequency f_g are given by:

$$A = R \quad \text{and} \quad f_g = \frac{1}{2\pi RC} \tag{40}$$

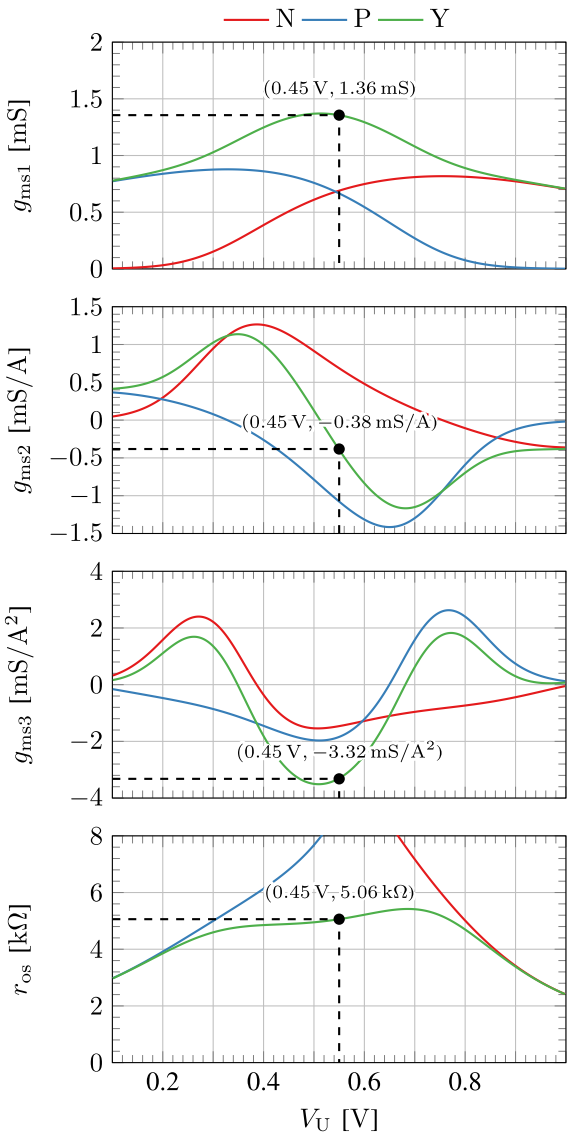


Fig. 13. The first three small-signal transconductance coefficients g_{msn}, and the output resistance r_{os} as a function of the static input voltage V_U. The supply voltage V_{DD} is 0.9 V, and the static output voltage V_Y is set to half the supply voltage.

TABLE I
CONTRIBUTION OF EACH INVERTER PAIR TO $1/R$

Inverter pair	Contribution to $1/R$
UP and UN	$\frac{1}{r_{os}}$
VP and VN	$\frac{1}{2r_{ol}}$
CCP and CCN	$\frac{1}{r_{os}} - g_{ms1}$
SCP and SCN	$\frac{1}{r'_{os}} + g'_{ms1}$

Table I summarizes the contribution of each inverter pair to the total conductance $\frac{1}{R}$. Here, g'_{ms1} and r'_{os} represent the modified small-signal transconductance and output resistance of a unit inverter operating at a different supply voltage V'_{DD}. The nominal value of R is 1.28 kΩ, and it can be adjusted from 2.35 kΩ to 1.00 kΩ by varying V'_{DD} from 0.8 V to 1.0 V. The

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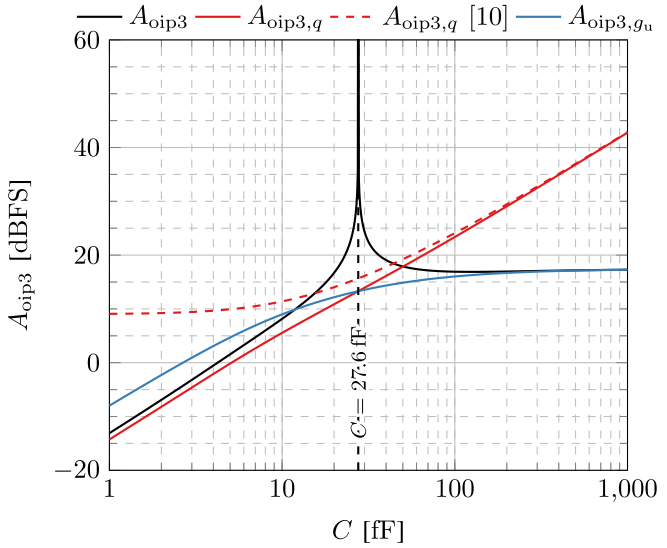


Fig. 14. Predicted A_{oip3,g_u}, $A_{\text{oip3},q}$, and the resulting A_{oip3} as a function of the loop filter capacitance C for a resistance R of 1.28 kΩ.

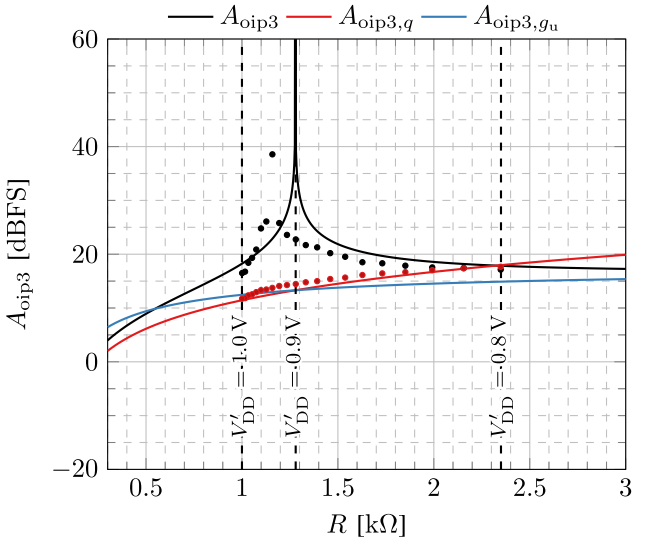


Fig. 15. Predicted A_{oip3,g_u}, $A_{\text{oip3},q}$, and the resulting A_{oip3} as a function of the loop filter resistance R for a capacitance C of 27.6 fF. The resistances R at a V'_{DD} of 0.8 V, 0.9 V, and 1.0 V are indicated with vertical dashed lines. The dots represent the schematic-level simulated OIP3s.

parasitic capacitances of the inverters contribute a parasitic capacitance C_i of 7.0 fF to the capacitance C.

The quantizer delay T_d was already determined to be 23 ps.

To determine the optimal loop filter capacitance C, we calculate A_{oip3,g_u}, $A_{\text{oip3},q}$, and the resulting A_{oip3} as a function of the loop filter capacitance C using Eqs. 26 and 25, respectively. As illustrated in Fig. 14, optimal linearity is achieved with a loop filter capacitance C of 27.6 fF. Given the parasitic capacitance C_i of 7.0 fF, an explicit capacitance C_e of 20.6 fF is required. For comparison, Fig. 14 also includes the predicted $A_{\text{oip3,q}}$ using the analytical model from [10], which becomes inaccurate for low OIP3s, i.e., high loop filter bandwidths with respect to the self-oscillation frequency. As a result, this prior model cannot correctly predict the required capacitance to compensate the nonlinearity.

To illustrate the effect of the tunable supply voltage V'_{DD} on the linearity, we also calculate A_{oip3,g_u}, $A_{\text{oip3},q}$, and the resulting A_{oip3} as a function of the loop filter resistance R for a capacitance C of 27.6 fF. The result is shown in Fig. 15, where the resistances R at a V'_{DD} of 0.8 V, 0.9 V, and 1.0 V are indicated with vertical dashed lines. The dots represent the schematic-level simulated OIP3s. The difference between the predicted and simulated OIP3s can be attributed to the nonlinearity of the output resistance, which is not captured in the model. Nonetheless, this only results in a small shift of the optimal resistance R and the corresponding supply voltage V'_{DD}, and can be compensated by adjusting C during the design.

IV. Experimental Results

A prototype is implemented using a commercially available 28 nm CMOS process. A die micrograph is presented in Fig. 16, showing the ASDM along with test structures outside the scope of this paper. The ASDM layout, which measures 27 μm × 18 μm, is also shown.

The measurement setup is illustrated in Fig. 17. The prototype is wire-bonded to a printed circuit board. A Keysight

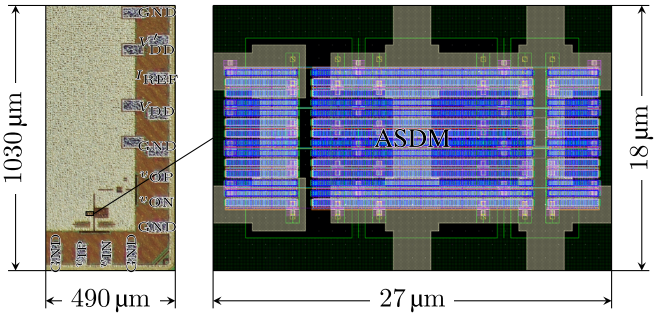


Fig. 16. Die micrograph and ASDM layout view.

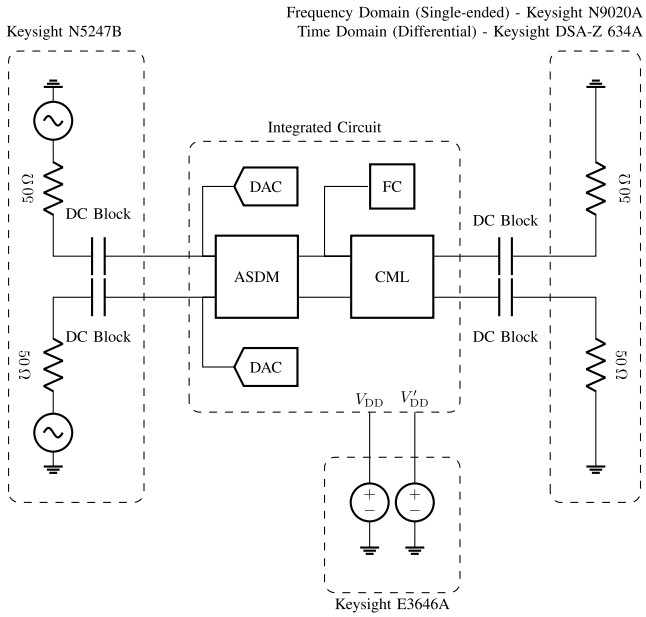


Fig. 17. Measurement setup.

E3646A power supply generates both the main supply voltage V_{DD} = 0.9 V and the tunable supply voltage V'_{DD}. The input is

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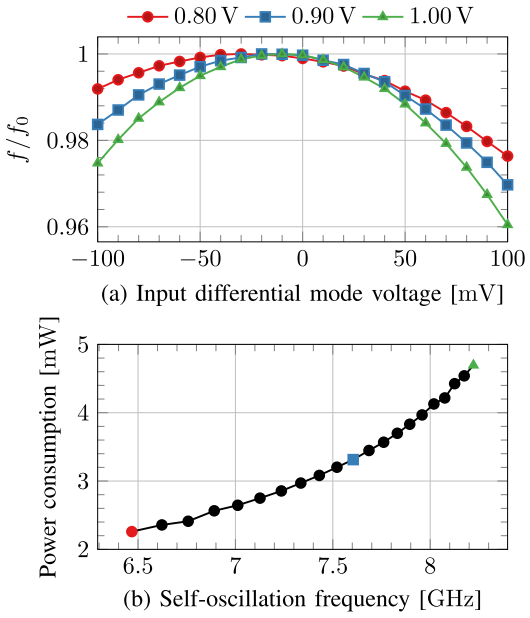


Fig. 18. (a) Ratio of the instantaneous frequency f to the self-oscillation frequency f_0 as a function of the input differential mode voltage. The result is shown for different supply voltages. (b) Power consumption and corresponding self-oscillation frequency as a function of the supply voltage (in steps of 10 mV).

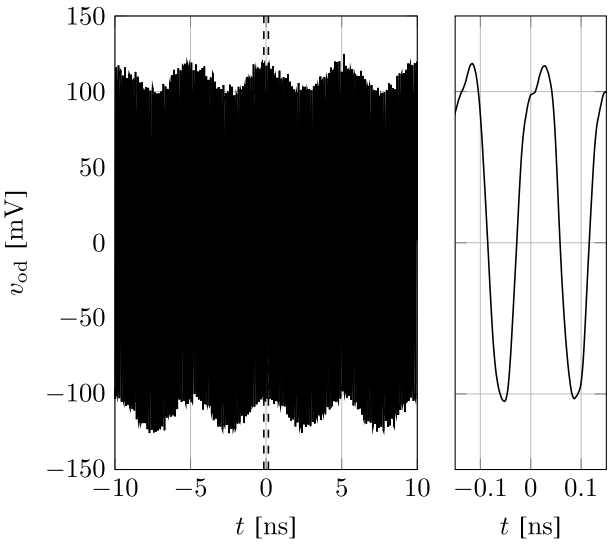


Fig. 19. Measured time domain waveform of the output signal for a 200 MHz input signal with a 100 mV amplitude.

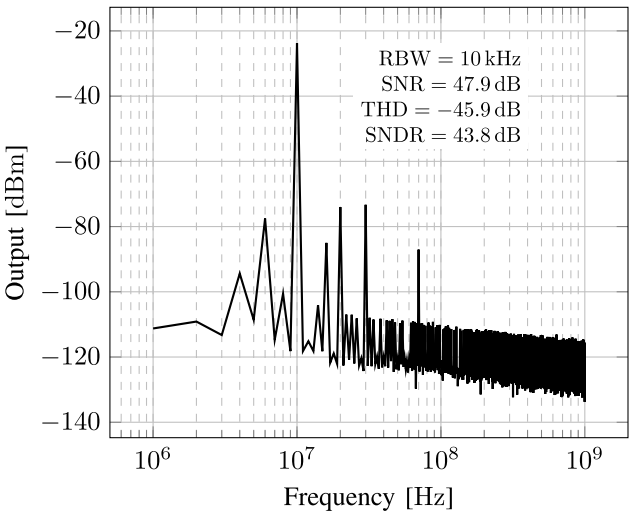


Fig. 20. Measured frequency domain waveform of the output signal at peak SNDR of 43.8 dB.

biased using two on-chip digital-to-analog converters (DACs), whereas the Keysight N5247B provides the differential input signal. To drive a 50 Ω load, the output is buffered by an on-chip current-mode logic (CML) driver. For time-domain measurements, the output is connected to a Keysight DSA-Z 634A oscilloscope, while frequency-domain measurements are performed using a Keysight N9020A spectrum analyzer. The oscillation frequency is measured using an on-chip frequency counter (FC).

Neglecting the static simulated power consumption of the DACs (94 μW) and the frequency counter (26 μW), the ASDM and the CML driver consume 3.1 mW and 6.9 mW, respectively. The power consumption is measured with a main supply voltage of V_{DD} = 0.9 V and an optimal tunable supply voltage of V'_{DD} = 0.826 V.

We measured the ratio of the instantaneous frequency f to the self-oscillation frequency f_0 as a function of the DC input voltage. The result is shown in Fig. 18a for different supply voltages. For the considered supply voltages, this sample has a 20 mV offset voltage. Figure 18b shows the power consumption and corresponding self-oscillation frequency as a function of the supply voltage.

A measured time domain waveform of the output signal for a 200 MHz input signal with a 100 mV amplitude is shown in Fig. 19. The right axis shows a magnified view of the region between the dashed lines. A measured frequency domain waveform of the output signal at peak SNDR of 43.8 dB is shown in Fig. 20. While the measurement is performed single-ended, the noise floor has been corrected by 3 dB to account for the differential operation of the ASDM.

To validate the proposed distortion cancellation technique, the third-order harmonic distortion is measured as a function of the tunable supply voltage V'_{DD} for input frequencies of 10 MHz, 20 MHz, and 50 MHz. As shown in Fig. 21, minimal third-order harmonic distortion is achieved at V'_{DD} = 0.826 V independent of the input frequency.

Next, the third-order harmonic distortion is measured as a function of the input amplitude for a 10 MHz input signal, for tunable supply voltages of 0.7 V, 0.9 V, and the optimal value of 0.826 V. As shown in Fig. 22, a wide range of input amplitudes achieves minimal distortion at the optimal tunable supply voltage. For comparison, the distortion is significantly higher for the 0.7 V where the distortion of the input path dominates, and for the 0.9 V where the distortion of the quantizer dominates. This demonstrates the effectiveness of the proposed distortion cancellation technique.

The measured performance, along with a post-layout simulation over corners, is summarized in Table II. The measured SNDR is 43.8 dB at a 500 MHz bandwidth, which is lower than the simulated SNDR of 48.1 dB. This difference is

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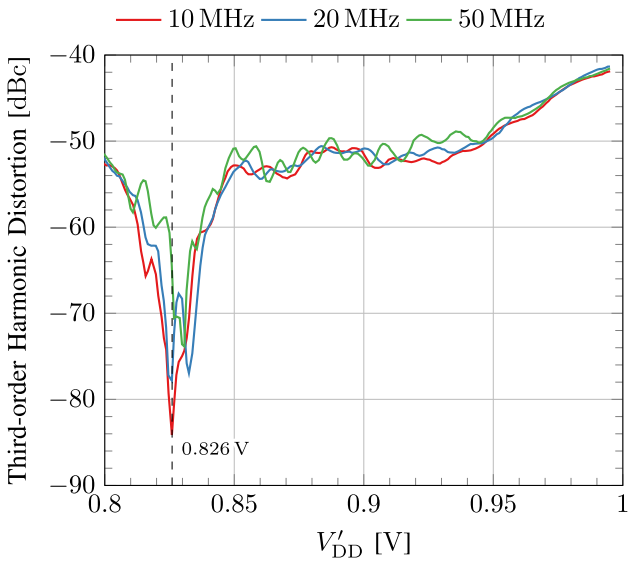


Fig. 21. Measured third-order harmonic distortion as a function of the tunable supply voltage V'_{DD} for input frequencies of 10 MHz, 20 MHz, and 50 MHz.

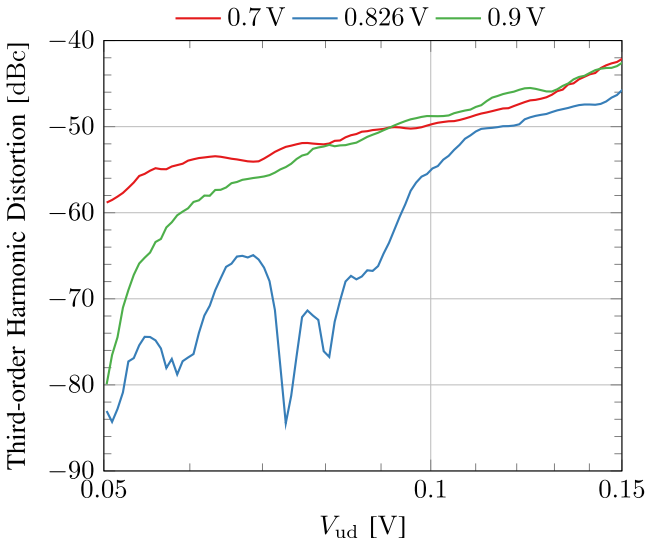


Fig. 22. Measured third-order harmonic distortion as a function of the input amplitude for a 10 MHz input signal for tunable supply voltages of 0.7 V, 0.9 V, and the optimal value of 0.826 V.

TABLE II
PERFORMANCE OVER A 500 MHZ BANDWIDTH

	Post-layout Simulation			Measurement
Corner	SS	TT	FF	
Temperature [°C]	100	70	0	
V_{DD} [mV]	900	900	900	900
V'_{DD} [mV]	936	903	821	826
P [mW]	2.6	3.3	4.1	3.1
f_0 [GHz]	8.1	9.7	11.7	7.2
Noise [dBFS]	−58.8	−58.7	−58.9	-
SNDR [dB]	48.1	48.1	48.3	43.8[a]
Offset [mV]	2	2	2	20

[a] Single-ended measurement + 3 dB SNR correction for differential operation.

mainly attributed to the inability to perform proper differential measurements during testing

TABLE III
COMPARISON WITH STATE OF THE ART

	This work	[13][a]	[14]	[1]	[15]	[16]
V_{DD} [V]	0.9	1	1.8	1.8	0.25	0.3
Tech [nm]	28	65	180	180	130	180
Area [mm^2]	486 µ	6.5 m	0.026	0.04	0.141[b]	0.059
Order	1	1	1	2	1	1
P [W]	3.1 m	240 µ	1.5 m	2.2 m	28 n	34 n
f [Hz]	7.2 G	300 M	140 M	120 M	630	3 k
BW [Hz]	500 M	2 M	8 M	12 M	30	81
SNDR [dB]	43.8	-	-	-	58	57.1

[a] Used in cascade with a VCO-ADC. Separate performance of ASDM not reported.
[b] Without passive components (external).

Finally, the performance of this work is compared with the state of the art in Table III.

V. CONCLUSION

This paper presented a design procedure for asynchronous sigma-delta modulators that exploits distortion cancellation between the quantizer and the input path. By accurately matching the expansive nonlinearity of the quantizer to the compressive nonlinearity of the input path, the proposed approach relaxes input path linearity requirements, enabling power-efficient high-bandwidth designs.

To support this procedure, we introduced a novel analytical model for first-order delay-based ASDMs that accurately characterizes the quantizer nonlinearity as a function of loop filter bandwidth. Prior models assume a loop filter bandwidth much smaller than the self-oscillation frequency, limiting their applicability. This model was shown to provide significantly improved predictions of the self-oscillation frequency and nonlinearity, particularly for high loop filter bandwidths.

The model was validated through the design of a 28 nm CMOS prototype. Operating at a self-oscillation frequency of 7.2 GHz, the prototype demonstrates distortion cancellation across a wide input amplitude range for frequencies within the loop filter bandwidth, while consuming only 3.1 mW from a 0.9 V supply. These results validate both the effectiveness of the proposed distortion cancellation technique and the accuracy of the analytical model.

APPENDIX

A. Trigonometric Series

During the derivation of the analytical model, several trigonometric series are used, which for completeness are listed below.

The following two series correspond to Eqs. 1.445.2 and 1.445.3 in [16]:

$$p(x,\alpha) = \sum_{k=1}^{\infty} \frac{\cos(kx)}{k^2+\alpha^2} \quad [0 \le x \le 2\pi]$$
$$= \frac{\pi}{2\alpha}\frac{\cosh(\alpha\pi - \alpha x)}{\sinh(\alpha\pi)} - \frac{1}{2\alpha^2} \tag{41}$$
$$q(x,\alpha) = \sum_{k=1}^{\infty} \frac{(-1)^k \cos(kx)}{k^2+\alpha^2} \quad [-\pi \le x \le \pi]$$
$$= \frac{\pi}{2\alpha}\frac{\cosh(\alpha x)}{\sinh(\alpha\pi)} - \frac{1}{2\alpha^2} \tag{42}$$

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Integrating Eqs. 41 and 42 with respect to x yields, respectively:

$$r(x,\alpha) = \sum_{k=1}^{\infty} \frac{\sin(kx)}{k\left(k^2+\alpha^2\right)} \quad [0 \le x \le 2\pi]$$
$$= -\frac{\pi}{2\alpha^2}\frac{\sinh(\alpha\pi - \alpha x)}{\sinh(\alpha\pi)} - \frac{x}{2\alpha^2} + \frac{\pi}{2\alpha^2} \tag{43}$$
$$s(x,\alpha) = \sum_{k=1}^{\infty} \frac{(-1)^k \sin(kx)}{k\left(k^2+\alpha^2\right)} \quad [-\pi \le x \le \pi]$$
$$= \frac{\pi}{2\alpha}\frac{\sinh(\alpha x)}{\sinh(\alpha\pi)} - \frac{x}{2\alpha^2} \tag{44}$$

The constants of integration are determined by evaluating the series at $x = 0$.

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