Random Telegraph Noise and Radiation Response of 80 nm Vertical Charge-Trapping NAND Flash Memory Devices With SiON Tunneling Oxide

Isabella R. Wynocker, *Member, IEEE*, En Xia Zhang, *Senior Member, IEEE*, Robert A. Reed, *Fellow, IEEE*, Ronald D. Schrimpf, *Fellow, IEEE*, Antonio Arreghini, João P. Bastos, Geert Van den Bosch, Dimitri Linten, *Senior Member, IEEE*, and Daniel M. Fleetwood, *Life Fellow, IEEE*

***Abstract*— Random telegraph noise (RTN) measurements are performed on as-processed, programmed, erased, and irradiated 80 nm vertical charge-trapping nand memory transistors. Variations in current with time of up to ±20% are observed during the RTN testing interval. The RTN of these devices is relatively unaffected by irradiation of devices to 500 krad(SiO_2). Root-mean-square (rms) magnitudes of measured RTN exceed predictions of number-fluctuation models (NFMs) by up to six-times. This result demonstrates that fluctuations in carrier scattering rates caused by motion and/or reconfiguration of traps at grain boundaries likely lead to a significant fraction of the low-frequency noise and/or RTN in poly-crystalline Si channel, charge-trapping memory devices. The magnitudes of these fluctuations may present significant challenges to the resolution of highly scaled 3-D memory devices.**

***Index Terms*— 3-D NAND, random telegraph noise (RTN), SiON tunneling layer, total dose effects.**

I. Introduction

THE prevalence of vertical charge-trapping NAND flash memory devices is increasing in space environments due to their nonvolatility and high-density storage characteristics [1], [2], [3]. Demand for scaled-down electronics working in low-noise and space applications has increased interest in three-gate vertical charge-trapping NAND Flash memory devices [4], [5]. The read process in vertical charge-trapping NAND flash memory devices is extremely sensitive to current levels.

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Isabella R. Wynocker, Robert A. Reed, Ronald D. Schrimpf, and Daniel M. Fleetwood are with the Department of Electrical and Computer Engineering (ECE), Vanderbilt University, Nashville, TN 37235 USA (e-mail: isabella.r.wynocker@vanderbilt.edu; robert.reed@vanderbilt.edu; ron.schrimpf@vanderbilt.edu; dan.fleetwood@vanderbilt.edu).

En Xia Zhang is with the Department ECE, University of Central Florida, Orlando, FL 32826 USA (e-mail: enxia.zhang@ucf.edu).

Antonio Arreghini, João P. Bastos, Geert Van den Bosch, and Dimitri Linten are with imec, 3001 Leuven, Belgium (e-mail: Antonio.Arreghini@imec.be; Joao.Bastos@imec.be; Geert.VandenBosch@imec.be; dimitri.linten@imec.be).

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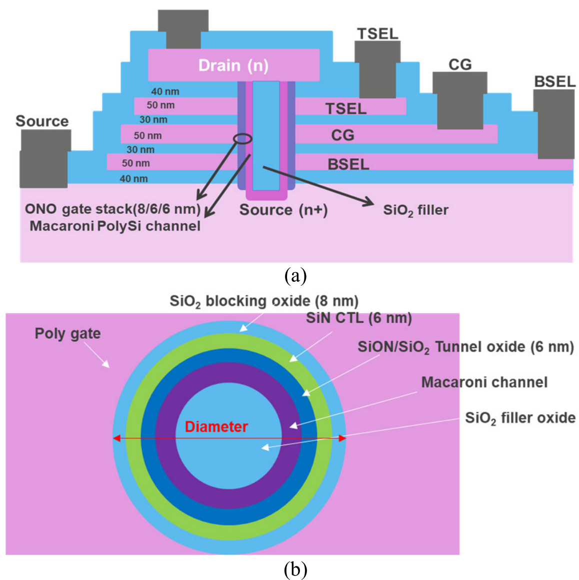

Fig. 1. (a) Lateral and (b) top-view cross-sections of charge-trapping 3-D NAND memory devices. After [5].

The random telegraph noise (RTN) in MOS transistor drain current results from random, discrete resistance switching events. Underlying fluctuations are due to charge trapping and emission from border traps in the gate dielectrics and/or time-dependent changes in scattering rates due to reconfiguration of intrinsic defects in the device channel [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16]. Hence, RTN measurements can provide significant insight into defects in MOS transistors and significant insights into device performance and reliability.

Cylindrical vertical 3-D NAND structures with poly-crystalline Si channels are commonly used for high-density storage [1], [4]. The development stage devices evaluated in this work (see Fig. 1) are fabricated by imec [4], [5]. The tunneling layer for these devices is SiON. The ONO thickness is fixed in the manufacturing process; the SiO_2 filler thickness is adjusted to modify the channel size. Devices with channel diameter of 80 nm are the focus of this work due to their relatively high radiation tolerance and scaled dimensions [5], [17], [18].

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The macaroni structure of the device channel improves the control of the gate over the channel [17]. For these devices, the macaroni channel is p-doped poly-crystalline Si at a concentration of 8 × 10^{18} cm^{-3} [17]. Previous studies of the radiation response and reliability of the vertical charge-trapping 3-D NAND flash memory devices of Fig. 1 have investigated the effects of geometry and cycling on the radiation response, showing that smaller devices have enhanced total-ionizing-dose (TID) tolerance and enhanced programmability, as demonstrated by enhanced threshold voltage shifts, as compared with otherwise similar larger devices [5], [18]. Charge-trapping NAND flash devices built in this technology show satisfactory endurance in cycling tests and radiation tolerance up to 500 krad(SiO_2) [18].

In this work, RTN measurements are performed on as-processed, programmed, erased, and irradiated vertical charge-trapping 3-D NAND memory transistors. Comparing the magnitudes of fluctuations with predictions of the number-fluctuation model (NFM) of low-frequency noise provides insight into the nature of the defects responsible for the observed fluctuations. Measured RTN magnitudes fluctuate by as much as ∼40%. Root-mean-square (rms) averages of RTN magnitudes exceed those predicted by number fluctuation models by up to six-times. These results strongly suggest that the motion and/or reconfiguration of traps at grain boundaries of the poly-crystalline macaroni channels adds significantly to the observed low-frequency noise and/or RTN of these devices.

II. Experimental Details

Drain current-gate voltage (I_{DS}–V_{GS}) characterization, program and erase processes, and RTN tests at gate overdrive voltages ($V_{GT} = V_{GS} - V_{TH}$, where V_{GS} is the gate-to-source voltage and V_{TH} is the threshold voltage) of 0.1–0.6 V were performed using a Keithley 4200A-SCS semiconductor parameter analyzer. Unless otherwise specified, the RTN testing consists of recording approximately 3000 equally spaced drain current I_{DS} measurements at fixed V_{GS} for 240 s, which is an equivalent sampling rate of 12.5 Hz. RTN testing was conducted for 39 trials on more than 15 devices with qualitatively comparable results. Results from representative devices are shown.

During device parametric characterization, the top-select (TSEL) gate and bottom select (BSEL) gate are biased at 7 V, the drain is biased at 0.5 V, and the control gate (CG) is pulsed from 0 to 12 V [5]. The threshold voltage, V_{TH}, is extracted through the maximum transconductance g_m method [5], [18]. Devices are programmed by applying incremental 100 μs step pulses of amplitudes of 12–24 V to the CG; BSEL and TSEL are biased at 7 V with the source and drain grounded [18]. Devices are erased by applying incremental 1 ms step pulses to the CG with amplitudes of −12 to −20 V; BSEL and TSEL are biased at −10 V with the source and drain grounded [18].

After devices undergo RTN testing in as-processed, programmed, and erased states, they are irradiated in either the programmed or erased state up to 500 krad(SiO_2) with ∼10-keV X-rays at a dose rate of 30.3 krad(SiO_2)/min with all terminals grounded [18], [19]. Post-irradiation I_{DS}–V_{GS} characterization typically is conducted 1 and 10 min after the end of the exposure to measure short-term annealing response. Most devices are then annealed for 24 h or longer to allow defects to equilibrate. I_{DS}–V_{GS} characterization is conducted immediately after the recovery period and before and after each RTN test. Devices exhibit significant changes in threshold voltage at 500 krad(SiO_2) but retain sufficient memory windows for successful operation in practical space radiation environments [5], [18].

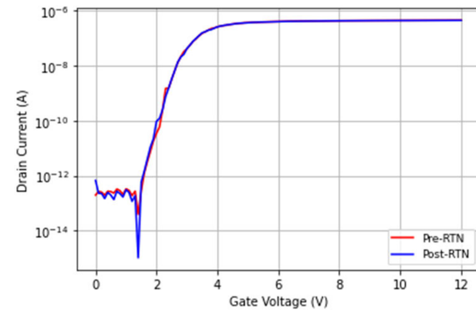

Fig. 2. I_{DS}–V_{GS} characteristics before and after RTN testing of a representative as-processed device.

III. RTN: As-Processed Devices

Figs. 2–4 display results from RTN testing of a representative as-processed device, which establishes a baseline for comparison with later results on programmed, erased, and/or irradiated devices. In Fig. 2, I_{DS}–V_{GS} characteristics are shown before and after the RTN measurement sequence of Fig. 3. Results were similar from run to run in all cases, and the order in which voltages were applied (small to large, large to small, or random) did not significantly affect the results. No detectable V_{TH} shift is observed as a result of RTN testing, verifying that any changes in defect density that occurs during device tests is insufficient to modify device electrical parameters.

Fig. 3 shows RTN results for the as-processed device of Fig. 2 versus V_{GT} and time, t. Variations in current with time of up to approximately ±20% are observed during the RTN testing interval. Visually apparent "steps" are observed for V_{GT} = 0.2 and 0.3 V, corresponding to persistent increases in current at times greater than ∼100 s. Rapid fluctuations of similar size are observed in several of the other I_{DS}–t traces in Fig. 3. Potential reasons for the observed RTN are discussed below.

The results of the RTN testing in Fig. 3 are visualized in the weighted time lag plots of Fig. 4. Delay of 1 s is imposed between the data on the y- and x-axes for the central display, and histograms of the I_{DS}–t distributions are shown on the right-hand and top edges of the figure [16], [20], [21], [22]. Stable current with Gaussian noise shows up in weighted time lag plots as a symmetrical round ball in the center of the plot and normal distributions along the edges [16], [20], [21], [22], [23]. The results of Fig. 4 clearly show that *none* of the I_{DS}–t distributions are Gaussian. All are bimodal, with the current fluctuating between higher and lower resistance levels, which is typical of devices showing significant RTN [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [20], [21], [22], [23].

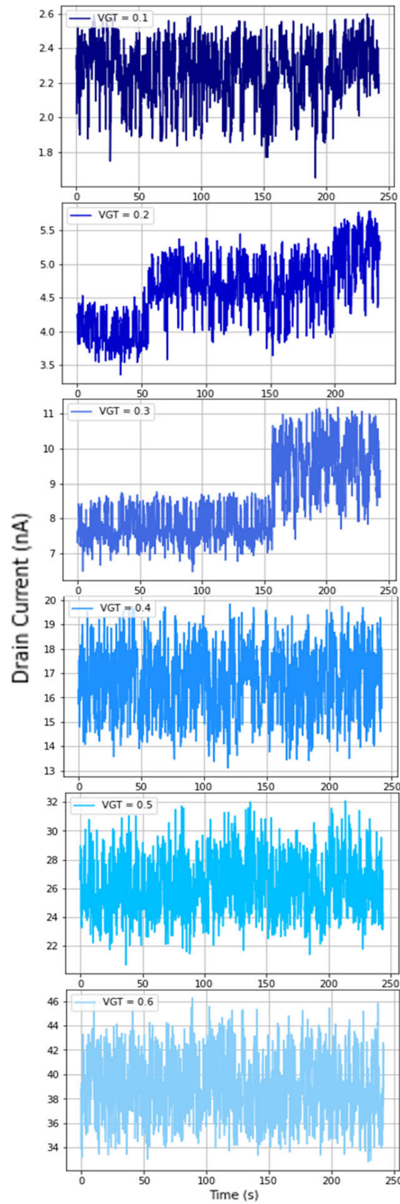

Fig. 3. I_{DS} versus time for the as-processed device of Fig. 2 as a function of V_{GT}. Values of V_{GT} range from 0.1 V (top) to 0.6 V (bottom). Devices equilibrated under bias for 60 s at each value of I_{DS} and V_{GT} before data recording began.

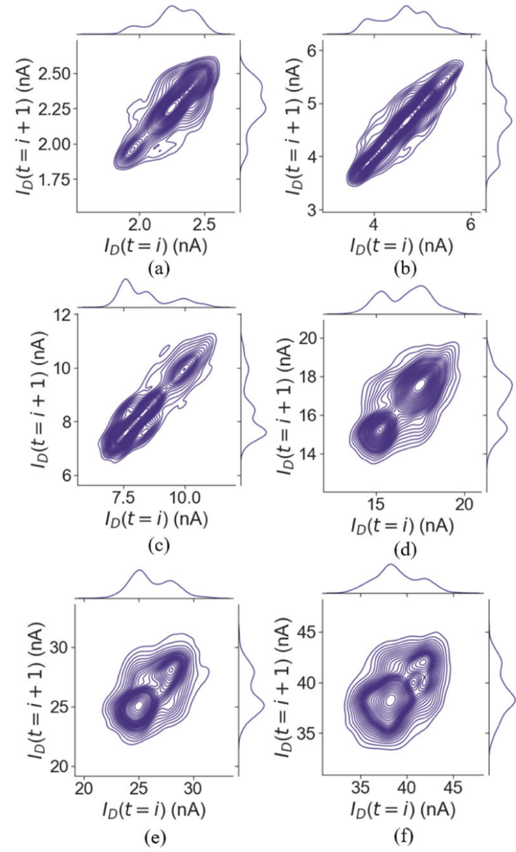

Fig. 4. Weighted time lag plots for the as-processed device of Figs. 2 and 3 at V_{GT} values ranging from (a) 0.1 V to (f) 0.6 V in 0.1 V intervals. Amplitude histograms that display relative distributions of drain current values are displayed on the top and right axes.

We now consider the potential origins of the measured fluctuations in drain current. RTN in MOS transistors is often considered to be due primarily to the exchange of charge between the device channel and prominent border traps in adjacent dielectric layers [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16]. However, it has been shown that RTN can also be caused by changes in the charge state of random dopant atoms in the device channel [24], [25], reconfiguration of bulk defects in the channel or in the source/drain depletion regions [15], [26], [27], and/or hydrogen-mediated passivation and depassivation of interface traps [13], [15], [28].

Comparing magnitudes of the fluctuations in Figs. 3 and 4 with the predictions of the NFM of low-frequency noise/RTN provides insight into the nature of the defects responsible for the observed fluctuations [7], [8], [9], [10], [12], [13], [14], [15], [16], [28]. When the amplitudes of the observed fluctuations are consistent with NFM predictions, the noise is due primarily to the exchange of single carriers with border traps without significant contributions from mobility fluctuation noise [12], [13], [14], [15]. For these devices, the border traps of most interest are in the tunnel oxide that separates the polycrystalline Si channel from the Si_3N_4 charge-trapping layer [5], [18]. When the noise significantly exceeds the predictions of the NFM, other defects that are much more efficient than border traps in scattering channel carriers most likely contribute significantly to the RTN, that is, random dopant atoms, bulk Si defects in the channel and/or near junctions, and/or interface traps [11], [13], [15], [16], [24], [25], [26], [27], [28].

In a first-order NFM, the magnitudes of the relative rms current fluctuations observed in RTN measurements, $\Delta I_D/I_D$, are related to the fluctuations in carrier number density, $\Delta N/N$, associated with the capture or emission of a single electron via [8], [9], [13], [14], [15], [16]

$$\Delta I_D/I_D \approx \Delta N/N = (NA)^{-1} \approx (qt_{\rm ox})/(A\varepsilon_{\rm ox}V_{\rm GT}). \quad (1)$$

Here, q is the magnitude of the electron charge, t_{ox} is the tunnel oxide thickness (~6 nm), ε_{ox} is the oxide dielectric constant, and $A = 2\pi Lt_{MC}$, where L is the channel length (~50 nm), and t_{MC} is the thickness of the macaroni channel (~15 nm) [5], [18].

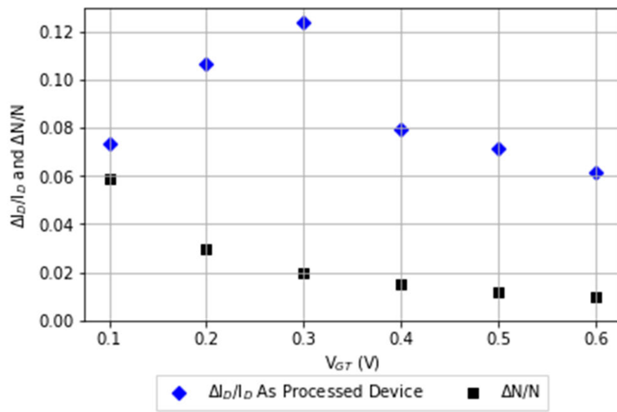

Fig. 5. Comparison of observed, $\Delta I_D/I_D$, and expected, $\Delta N/N$, rms magnitudes of current fluctuations leading to low-frequency noise and/or RTN for an as processed device. I_D is the average of the current values for each I_{DS}–t trace in Fig. 3; ΔI_D is the respective standard deviation in measured current for each trace; and $\Delta N/N$ is calculated using (1) of the text.

Fig. 5 compares experimental measurements of $\Delta I_D/I_D$ for the as-processed device of Figs. 3 and 4 with NFM estimates of $\Delta N/N$ from (1). For these devices, the measured rms current fluctuations exceed those expected from simple NFM predictions by up to a factor of 6 (at $V_{\mathrm{GT}} = 0.3$ V). Hence, except at the lowest value of V_{GT}, the dominant sources of RTN in as-processed devices is most likely the motion or reconfiguration of prominent defects in the macaroni channel of the transistor or at the channel/SiO_2 interface, and/or hydrogen-mediated activation and passivation of interface traps [13], [15], [24], [25], [26], [27], [28].

IV. Programming, Erasure, and Irradiation

Programming charge-trapping memory transistors leads to significant electron trapping in the Si_3N_4 layer [5], [18], [29]; the erasure sequence neutralizes negative trapped charge due to hole capture or electron emission; and irradiation leads to hole trapping [5], [18], [29]. We now illustrate how these changes in trapped charge densities may affect the RTN of these devices.

Fig. 6 shows I_{DS}–V_{GS} characteristics before and after RTN testing for a second device after programming and irradiation. Comparing Figs. 2 and 6(a), programming leads to about a +5 V shift due to electron trapping in Si_3N_4 [5], [18]. Negative V_{TH} shifts occur during irradiation due to hole trapping in SiO_2 and/or Si_3N_4, as shown in Fig. 6(b) [5], [7], [18], [19], [29], [30]. The I_{DS}–V_{GS} curves show small negative shifts during RTN testing in Fig. 6(a) and (b), due primarily to trapped-electron emission during the RTN testing interval [5], [7].

Fig. 7(a) shows I_{DS} versus time plots for the device of Fig. 6 as a function of V_{GT} (a) after programming but before irradiation, and Fig. 7(b) shows similar results after the device is irradiated to 500 krad(SiO_2) and annealed at room temperature with all pins grounded. Again, variations in current with time of up to ±20% are observed. In Fig. 7(a) and (b), the observed increases in resistance with time are due primarily to annealing of negative trapped charge in the Si_3N_4 layer of the programmed

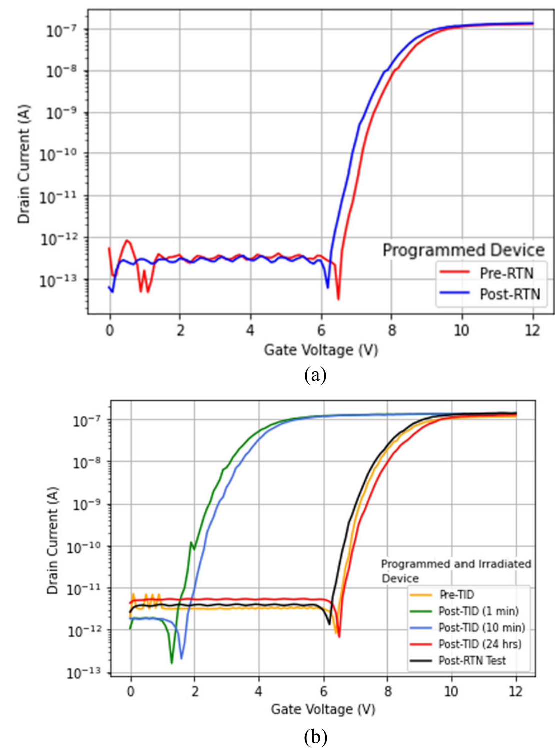

Fig. 6. I_{DS}–V_{GS} characteristics before and after RTN testing of a second representative device (a) after being programmed and (b) after irradiation to 500 krad(SiO_2) and room temperature annealing with all pins grounded.

device [5], [18], [29]. Observed and expected estimates of the magnitudes of the current fluctuations are compared in Fig. 8. Except at $V_{\mathrm{GT}} = 0.1$ V, the observed rms fluctuations again exceed the values predicted by a simple NFM. Hence, the current fluctuations that exceed 10%, observed between 0 and 50 s for $V_{\mathrm{GT}} = 0.5$ V in both Fig. 7(a) and (b), for example, are due most likely to resistance fluctuations associated with significant reconfigurations of defect complexes in the poly-crystalline macaroni channel [7], [13], [15], [17], [24], [25], [26], [27], [28], [31], [32], [33], [34]. Similarly, large fluctuations are not observed in charge-trapping transistor memory devices fabricated in bulk 14-nm FinFET technology, in which RTN was found to be entirely consistent with charge exchange with border traps [14]. RTN associated with border traps also likely contribute to the more common, but much smaller fluctuations in these devices [9], [10], [11], [12], [13], [14], [15]. The similarity of the RTN before and after irradiation is consistent with recent studies that often find stable RTN up to TID levels greater than 100 Mrad(SiO_2) [6].

Selected results of the RTN testing in Fig. 7 are visualized in the weighted time lag plots of Fig. 9. These plots correspond to a device that was (a) programmed but not irradiated, and then (b) irradiated to 500 krad(SiO_2) and annealed at room temperature. Prominent two-level fluctuators are resolvable in Fig. 9(a.ii)–9(b.i). In Fig. 9(a.i), the observed distribution is consistent with longer dwell times for the device in its lower resistance state. Higher and lower resistance states are more uniformly represented in most of the other figures. A diagonally elongated distribution is evidence of resistance drift during measurement, as seen most clearly in Fig. 9(b.i).

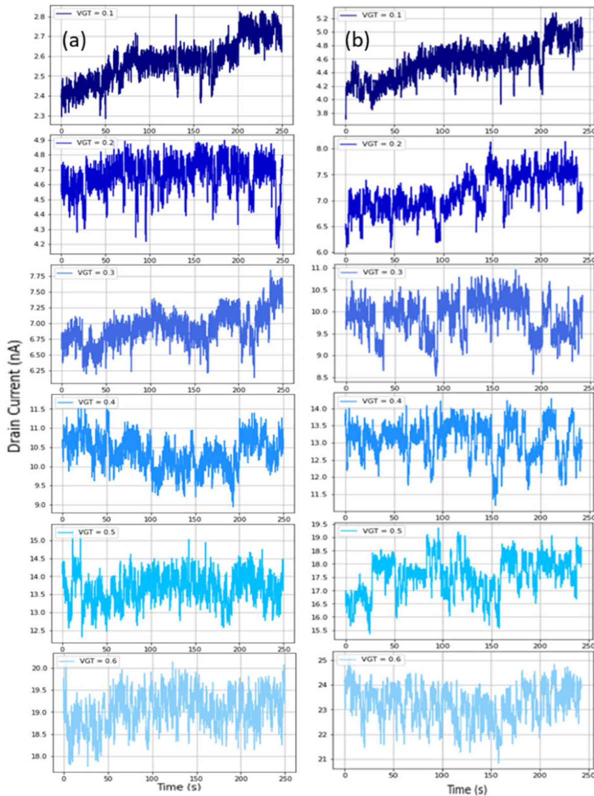

Fig. 7. I_{DS} versus time and V_{GT} for the device of Fig. 6 (a) after programming and (b) after irradiation to 500 krad(SiO_2) with all pins grounded. Values of V_{GT} range from 0.1 V (top) to 0.6 V (bottom). Devices were allowed to equilibrate under bias at least 60 s at each value of I_{DS} and V_{GT} before data recording began.

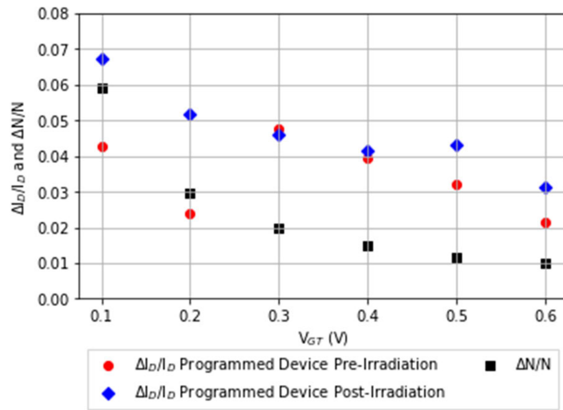

Fig. 8. Comparison of observed, $\Delta I_D/I_D$, and NFM estimates, $\Delta N/N$, of rms magnitudes of current fluctuations leading to low-frequency noise and RTN for the programmed devices of Figs. 6 and 7, before and after irradiation. ΔI_D is the respective standard deviation in measured current for each trace; $\Delta N/N$ is calculated using (1) of the text.

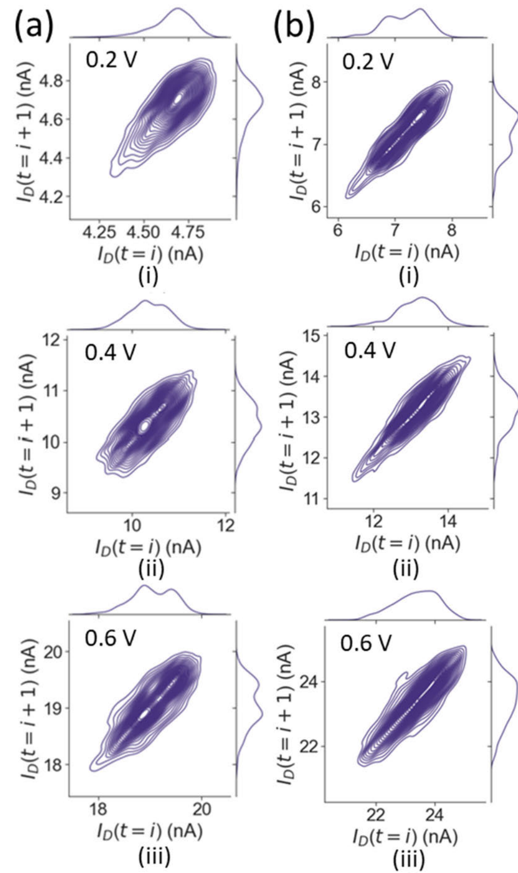

Fig. 9. Weighted time lag plots for (a) programmed device and (b) irradiated device of Figs. 6–8 at V_{GT} values ranging from (i) 0.2 V to (iii) 0.6 V in 0.2 V intervals. Amplitude histograms that display relative distributions of drain current values are displayed on the top and right axes.

The $V_{GT} = 0.1$ V cases in Fig. 7 are not only pictured in Fig. 9 but also represent examples of resistance drift during measurement. At this lowest value of V_{GT}, individual carrier trapping or emission leads to more significant relative changes in V_{TH} than do similar events at higher gate overdrive voltages. Thus, RTN data are typically less stable at smaller values of V_{GT}. As a result, we often focus mostly on larger values of V_{GT} in the RTN analysis.

Fig. 10 shows I_{DS}–V_{GS} characteristics for a third device that was put through programming and erasure, before it was irradiated to 500 krad(SiO_2). Comparison of Figs. 2 and 10(a) shows that V_{TH} is similar after erasure to that of the as-processed devices, as desired [5], [18]. Fig. 10(b) shows negative radiation-induced V_{TH} shifts, followed by trapped-charge neutralization during room temperature annealing [5], [7]. Minimal changes in V_{TH} occur during RTN tests in Fig. 10(a) and (b).

Fig. 11(a) and (b) shows I_{DS} versus time plots for the programmed and erased devices of Fig. 10(a) and (b), respectively. Again, currents vary by up to about ±20% during RTN evaluation. With the exception of the $V_{GT} = 0.1$ V trace in Fig. 11(a), there is generally less "drift" of device characteristics for the erased devices, before and after programming, than for the programmed devices of Fig. 7. This emphasizes the significance of trapped negative charge loss from the Si_3N_4 to the observed resistance drift in programmed devices.

Fig. 12 compares measured and expected magnitudes of the rms current fluctuations for devices of Figs. 10 and 11. Except at $V_{GT} = 0.1$ V, observed rms fluctuations exceed values predicted by a simple NFM by factors of 2–4. These results are similar to those of programmed devices in Fig. 8, reinforcing the significance of mobility fluctuations to RTN in these charge-trapping memory devices [7], [13], [15], [35], [36], [37].

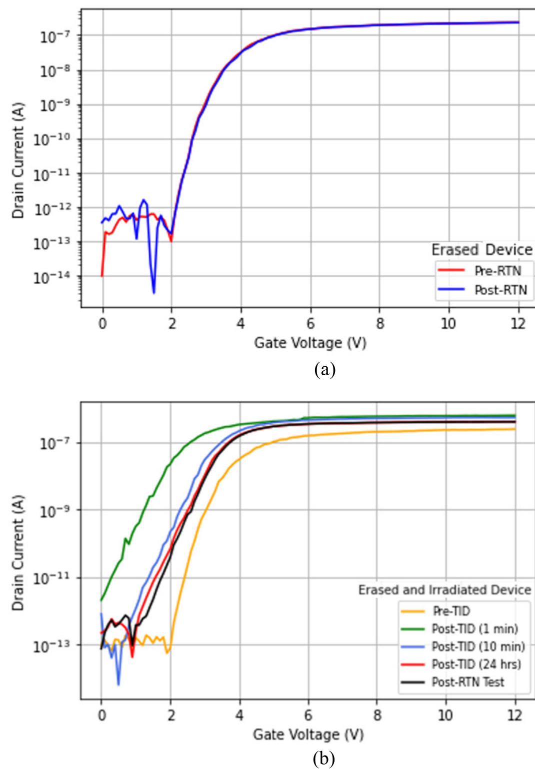

Fig. 10. I_{DS}–V_{GS} characteristics before and after RTN testing of a third representative device (a) after a full programming and erasure sequence and (b) after erasure and irradiation of the device to 500 krad(SiO_2) at room temperature, followed by annealing with all pins grounded.

The results of RTN testing in Fig. 11 are again visualized in the weighted time lag plots of Fig. 13 [16], [20], [21], [22]. Fig. 13(a) shows a device that was erased but not irradiated, and Fig. 13(b) shows results for a device that was irradiated to 500 krad(SiO_2) and annealed at room temperature. These distributions are generally more Gaussian than for the as-processed device of Fig. 4 or the programmed device of Fig. 9. Nearly symmetric distributions are seen in Fig. 13(a.iii), (b.i), and (b.iii), for example. Fewer slow, two-state fluctuators are visible in erased devices, most likely as a result of defect reconfiguration that typically accompanies charge neutralization processes [18], [19], [38], [39]. The diagonally elongated distribution observed in Fig. 13(a.i) is again due to resistance drift during measurement. Similar RTN is again observed before and after irradiation [6].

Probabilities of observing larger fluctuations increase at rates of $1/f$ to $1/f^2$ for systems exhibiting $1/f$ noise and/or prominent two-level fluctuations [10], [35], [36], and even more strongly than $1/f^2$ for systems exhibiting percolative transport [40], [41], as expected for conduction in the poly-crystalline Si channels of these devices [31], [32], [33], [34], [42]. Hence, one might expect larger fluctuations if data are collected over much longer sampling times. Accordingly, Figs. 14–16 show I_{DS}–V_{GS} characteristics before and after RTN measurements for typical and extended time-series data for a device that underwent programming and irradiation sequences similar to those of Figs. 6–9, except that the waiting time between the 10 min post-TID irradiation-annealing curve and pre-RTN measurement time in Fig. 14 is 11 months

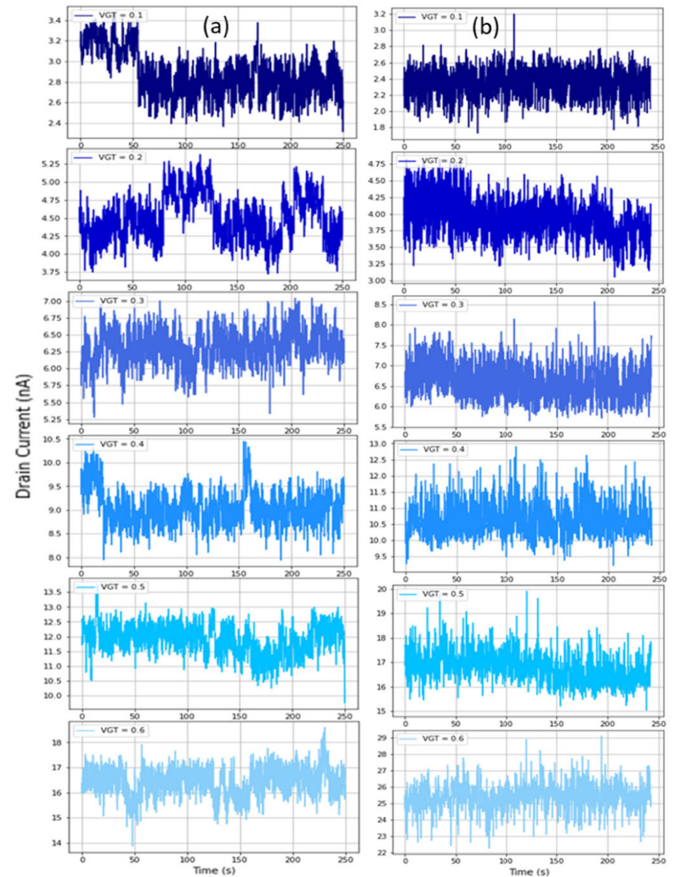

Fig. 11. I_{DS} versus time and V_{GT} for (a) programmed and erased device of Fig. 10(a), and (b) device of Fig. 10(b) after irradiation to 500 krad(SiO_2) and 30 min of post-irradiation annealing at room temperature. Values of V_{GT} range from 0.1 V (top) to 0.6 V (bottom). Devices equilibrated under bias for at least 60 s at each value of I_{DS} and V_{GT} before data recording began.

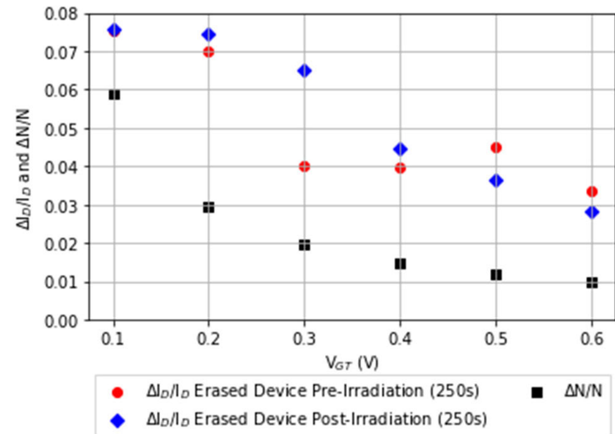

Fig. 12. Comparisons of observed, $\Delta I_D/I_D$, and expected, $\Delta N/N$, rms magnitudes of current fluctuations leading to low-frequency noise and/or RTN before and after irradiation for an erased device. ΔI_D is the respective standard deviation in measured current; and $\Delta N/N$ is calculated using (1) of the text.

before RTN measurements. This longer waiting time leads to additional trapped-electron charge loss, as noted by the negative shift of the I_{DS}–V_{GS} curve between the post-TID 10-min and 11-month curves in Fig. 14. Small changes are also observed as a result of the annealing of trapped positive charge during RTN measurement.

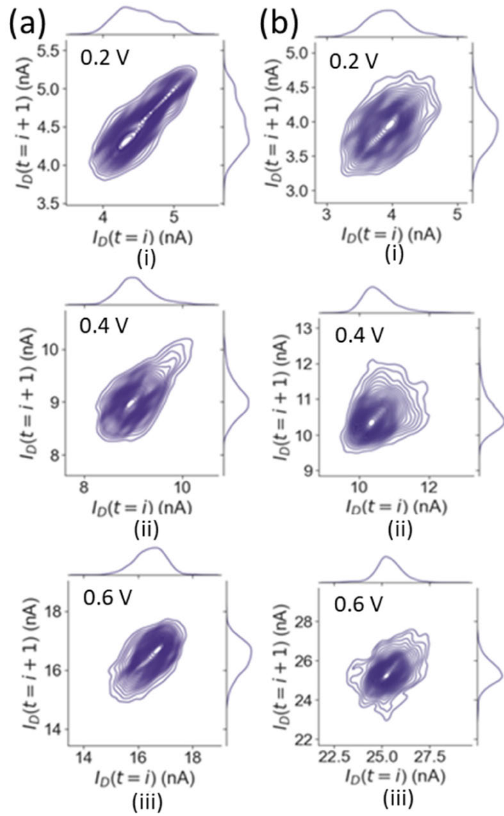

Fig. 13. Weighted time lag plots for (a) programmed and erased device of Figs. 10(a) and 11(a), and (b) device of Figs. 10(b) and 11(b) after irradiation to 500 krad(SiO_2) and 30 min of post-irradiation annealing at room temperature. Values of V_{GT} range from (i) 0.2 V to (iii) 0.6 V in 0.2 V intervals. Amplitude histograms that display relative distributions of drain current values are displayed on the top and right axes.

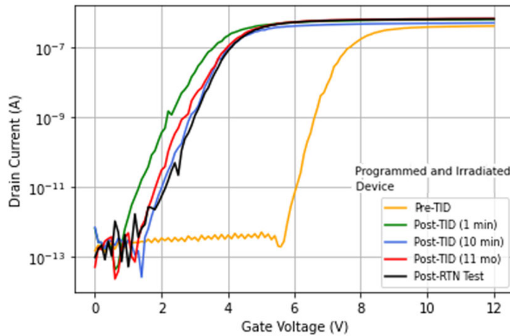

Fig. 14. I_{DS}–V_{GS} characteristics before and after RTN testing for a fourth device that was programmed and irradiated to 500 krad(SiO_2), followed by room temperature annealing with all pins grounded.

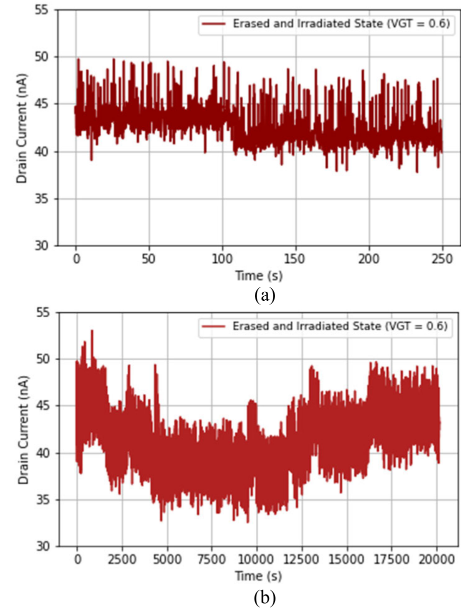

Fig. 15. Analysis of RTN the programmed and irradiated device of Fig. 14 at $V_{GT} = 0.6$ V for (a) normal and (b) extended measuring series.

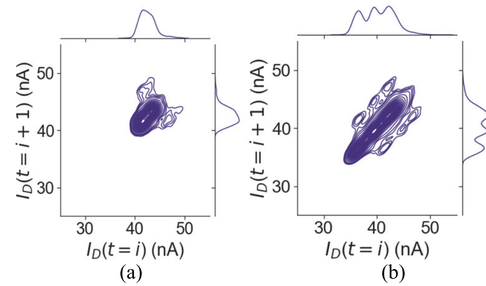

Fig. 16. Weighted time lag plots at $V_{GT} = 0.6$ V for the programmed and irradiated device of Fig. 14 for (a) time series of Fig. 15(a), and (b) extended time series of Fig. 15(b). Amplitude histograms that display relative distributions of drain current values are displayed on the top and right axes.

Fig. 15(a) and (b) shows RTN measurements at $V_{GT} = 0.6$ V for the device of Fig. 14 at a typical 250 s sampling time and an 80× longer sampling time, respectively. Observed differences in I_{DS} during these RTN measurements are within the range of sample-to-sample variations in initial drive current for these development-stage, poly-crystalline Si channel devices, as illustrated in Figs. 2, 6, 10, and 14. Note that the RTS trace in Fig. 15(a) has higher drain current than the previous programmed and irradiated device of Fig. 7(b), but otherwise shows a similar Gaussian current distribution. Such large variations are typical of percolative current transport [41], [42], [43], [44].

Extended testing RTN data of the device of Fig. 15(b) starts similar to that of the shorter time series data in Fig. 15(a), but then shows a large slow drift to currents up to 40% lower than initial values, followed by recovery to levels similar to starting values. This is evidence of extremely slow, reversible defect reconfiguration processes that can lead to changes in current that are large enough to potentially affect successful device operation. Weighted time lag plots show an approximate Gaussian distribution for shorter time series in Fig. 16(a) and a clear *trimodal* distribution in longer time series in Fig. 16(b).

Overall, variations in current with time of up to ±10% are observed during the shorter RTN measuring interval in Fig. 15(a), with up to ±20% variation observed in the longer measuring interval of Fig. 15(b). Each of these lies within the range of relative variations (normalized to drive current) of devices in Figs. 2–13, affirming that similar mechanisms contribute to RTN in all cases considered in this work.

Finally, we note that large $1/f$ noise and significant random-telegraph noise also has been observed in floating-gate Flash memory devices, as a result of similar fluctuation processes to the ones considered in this work [41], [43], [44].

Therefore, the significant current variations illustrated in this work are not unique to these charge-trapping 3-D NAND-Flash device architectures. In any poly-crystalline Si macaroni channel device, it is likely that current fluctuations will become increasingly significant to device operation as nonvolatile memory dimensions continue to scale [30], [41], particularly for multistate memory devices where increased resolution is required to avoid read-out errors.

V. Summary and Conclusion

RTN has been characterized in as-processed, programmed, erased, and irradiated 80 nm vertical charge-trapping 3-D NAND Flash memory transistors with poly-crystalline Si channels. Current variations in time of up to ±20% are observed on time scales up to several hours in these devices. Irradiation does not significantly affect the magnitudes of the observed RTN for these devices, consistent with the conclusions of [6] for a variety of other MOS devices. RTN magnitudes exceed those expected from border-trap NFMs of low-frequency noise/RTN by up to six-times for devices that are programmed, erased, and/or irradiated. This contrasts with previous work on charge-trapping transistor memory devices fabricated in bulk 14-nm FinFET technology, in which RTN was found to be caused almost entirely by charge exchange with border traps [14].

Based on the results of this study, the most likely origin of the largest RTN in these 3-D NAND Flash memory transistors with poly-crystalline Si channels is fluctuations in carrier scattering rates caused by motion and/or reconfiguration of defect complexes at grain boundaries of the poly-crystalline macaroni channels, which exhibit percolative current transport. The relative significance of these large-scale fluctuations will most likely become increasingly significant as nonvolatile memory dimensions continue to shrink, particularly for multistate memory devices that require increased current resolution to avoid read-out errors. This will be an important issue to investigate in future work.

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