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Exploring GAA-Nanosheet, Forksheet and GAA–Forksheet Architectures: A TCAD-DTCO Study at 90 nm and 120-nm Cell Height

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ABSTRACT This study presents a Technology Computer Aided Design (TCAD) and comprehensive Design-Technology Co-Optimization (DTCO) approach to evaluate and enhance power and performance in Gate-All-Around Nanosheet (GAA-Nsh) and Forksheet (Fsh) architectures. The analysis focuses on the impact of active widths, sheet count, wall properties, and power delivery methods on the effective resistance (R_{eff}) and capacitance (C_{eff}) of these devices. The research employs simulations of five-stage INVD1 ring oscillators (RO) at various metal pitches (Mx) to extract frequency and power data. Notably, a novel Gate-All-Around Forksheet (GAA-Fsh) structure is introduced, offering enhanced gate control while retaining the advantages of Fsh. The study also explores asymmetric N/PFETs within the Fsh technology, and innovative contacting approaches such as Buried Power Rail (BPR) and Backside Power Rail (BS-PR) with Backside Contact (BSC) to reduce access resistance. Results indicate that GAA-Fsh outperforms traditional GAA-Nsh and Fsh due to reduced R_{eff} and C_{eff}, although it is process feasible only at larger Mx. At smaller Mx, GAA-Nsh demonstrates higher performance than Fsh at a given sheet width (W_{sh}), but Fsh, with the advantage of additional W_{sh}, can match GAA-Nsh performance at larger W_{sh}. Furthermore, the BPR and BS-PR contacting schemes are found to provide similar performance. This research provides valuable insights into future semiconductor device designs, emphasizing higher performance and efficient scaling.

INDEX TERMS DTCO, nanosheet, Forksheet, buried power rail, backside power delivery, PPA, process integration, design rules.

I. INTRODUCTION

The continuous advancement in semiconductor technology demands innovative device architectures that can sustain the trend of scaling while enhancing performance. The Gate-All-Around Nanosheet (GAA-Nsh) device architecture (Fig. 1a) emerges as a promising solution, enabling aggressive scaling of the contacted gate pitch (CGP) and offering a substantial drive current per footprint advantage [1] [2]. Despite these benefits, the potential for scaling the standard cell height (CH) is constrained by the process-limited minimum separation between N-type and P-type field-effect transistors (N/PFETs). This N-P separation restricts the scaling of parasitic capacitance, thereby impacting the overall circuit speed.

To address this limitation, the Forksheet (Fsh) architecture (Fig. 1b) introduces a dielectric wall between N- and P-FET [3], [4]. This design modification significantly reduces gate parasitic capacitance and allows an increase in the

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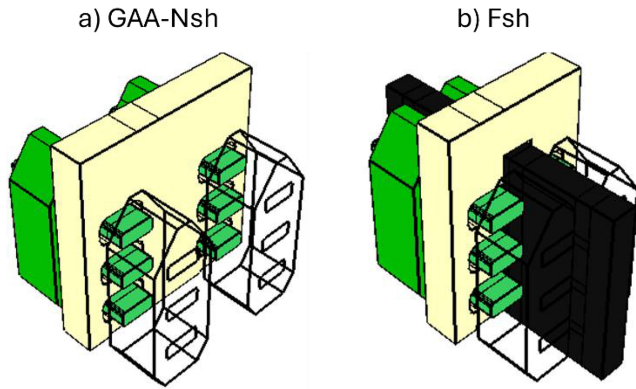

FIGURE 1. **3D bird's eye view of a) GAA-Nsh and b) Fsh. Notice how the Fsh wall (black) runs through the gate (yellow), semiconductor (green) & S/D contact metal (not shown).**

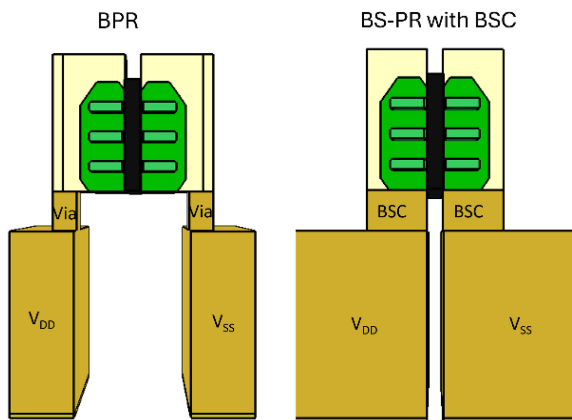

FIGURE 2. **Cross section of a) BPR and b) BS-PR with BSC contact. Due to its frontside process, BPR & its via cannot extend underneath active. Backside processed BS-PR & BSC can go underneath active**

active width while maintaining a fixed CH. However, the Fsh architecture's tri-gate configuration can lead to diminished gate control, presenting another challenge to overcome.

This study aims to tackle these challenges through a comprehensive Technology Computer Aided Design (TCAD) and Design-Technology Co-Optimization (DTCO) approach. GAA-Nsh and Fsh devices are compared across parameters such as active width (W_{sh}), sheet count (N), Fsh dielectric wall thickness (T_{wall}) and permittivity (k), contact resistance (CR), and metal pitch (Mx). These comparisons are conducted through simulations of device characteristics and five-stage INVD1 ring oscillators (RO). Additionally, two new contacting approaches like the buried power rail (BPR) and backside power rail (BS-PR) with backside contact (BSC) are investigated (Fig. 2) [6], [7]. Moreover, two new Fsh variants are explored: 1) a novel GAA-Fsh structure, where the Fsh wall is etched along the width of the device and filled with a gate stack to form a GAA configuration (Fig. 3a) [5], and 2) the impact of asymmetric N/PFETs to optimize performance (Fig. 3b). This work extends the findings presented in our previous study in [8], offering a more detailed and comprehensive analysis.

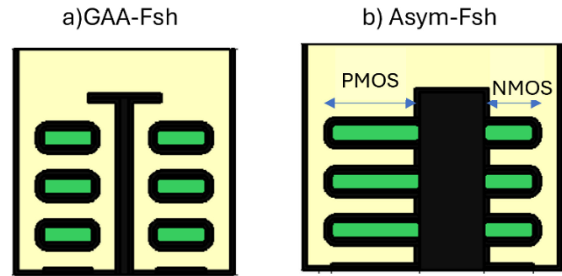

FIGURE 3. **2D view of a) GAA-Fsh and b) Asymmetric-Fsh. A lateral etch into the Fsh wall allows for gate formation all around the sheets (GAA-Fsh). Weaker PMOS (due to possible stress loss) could be counteracted by exchanging NMOS for PMOS active.**

In Section II, the process flow and layout-design rules essential for the implementation of these architectures are discussed. Section III provides a brief discussion on the TCAD and DTCO framework followed by a detailed presentation of the simulation results in Section IV. Finally, in Section V, the study is concluded by summarizing the key findings and their implications for future semiconductor device designs.

II. PROCESS AND DESIGN RULES

In this section, the integration flow of Buried Power Rail (BPR) (Fig. 4) and Backside Power Rail (BS-PR) with Backside Contact (BSC) (Fig. 5) are discussed. The flows presented are for Fsh, but they are similar for GAA-Nsh, with the step involving wall formation excluded. This is followed by an elaboration on layout design rules for GAA-Nsh and Fsh.

A. INTEGRATION FLOW OF BURIED POWER RAIL (BPR)

The area and routing benefits of the buried power rail (BPR) have been studied at a full block level in previous works [9], [10], [11]. While BPR can be accessed from the backside (BS), its integration occurs entirely from the frontside (FS) [12], [13] (See Fig. 4). For sheet-based devices, the process begins with a Si substrate containing an epitaxial Si/SiGe superlattice. After etching the active pillars, the N-P separation trench is filled with dielectric material, forming the Fsh wall. This is followed by shallow trench isolation (STI), which is created by filling and planarizing silicon dioxide (oxide).

Next, the BPR trenches are patterned, lined with an insulating dielectric, and metallized. The BPR trench may be partially embedded into the Si substrate. The BPR metal is then recessed to a specific depth and a BPR cap is formed by depositing a thin conformal silicon nitride layer; to ensure adequate dielectric isolation on top of the recessed BPR metal, which helps avoid metal cross-contamination during critical front-end-of-line (FEOL) processing. This is followed by fill and planarization of oxide. Dummy gate line formation then takes place using dummy gate oxide and poly-Si.

The gate sidewall outer spacer is deposited next. Subsequently, the original Si/SiGe stack is etched away in the source/drain (S/D) regions. A lateral etch trims the

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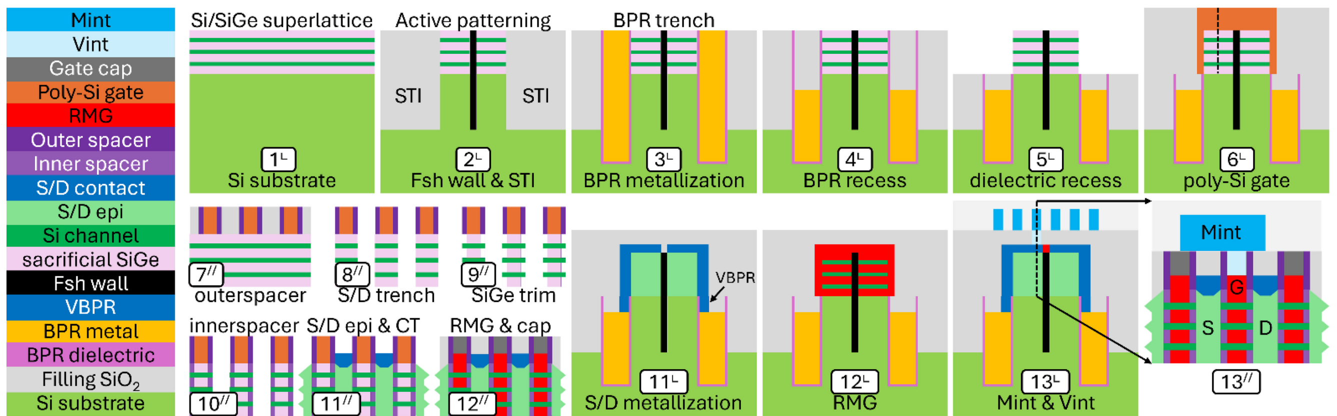

FIGURE 4. BPR process flow for Fsh. Top row shows formation of STI, Fsh wall, BPR and poly-Si gate. Bottom left shows outer & inner spacer formation, S/D epi, S/D metallization and RMG. Bottom right includes first routing layer (Mint). {Process order is indicated by numbers 1-13. Views perpendicular (⌞) and parallel (//) to channel orientation.}

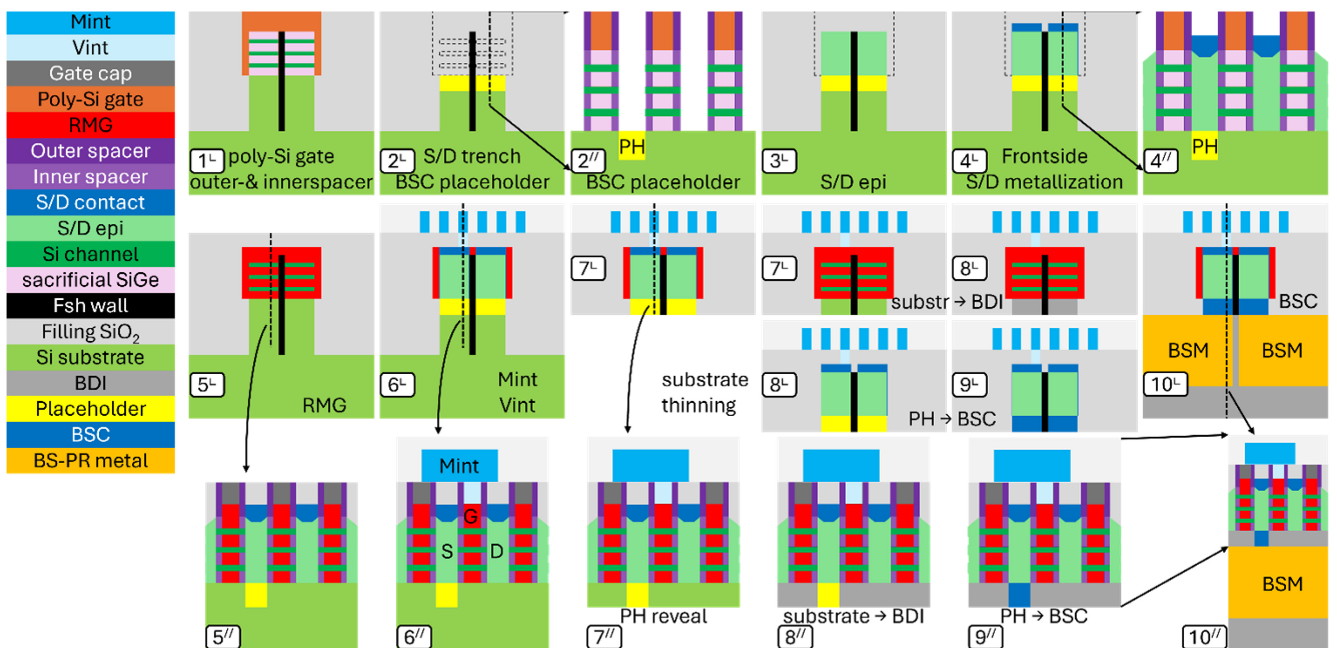

FIGURE 5. BS-PR process flow for Fsh with placeholder (yellow), BSC (dark blue), BDI (dark grey) and first BS metal (orange). {Process order is indicated by numbers 1-10. Views perpendicular (⌞) and parallel (//) to channel orientation.}

sacrificial SiGe beneath the outer spacer. S/D trenches are lined with a spacer dielectric, and a subsequent dry etch provides access to the remaining Si underneath the outer spacer while maintaining the newly formed inner spacer. From the exposed Si channel cross-section at the edges of the S/D trenches, S/D epitaxial growth can occur. Following this, S/D epitaxial silicidation and metallization of the contact and via to the BPR are performed using a dual damascene process.

After contact formation, the poly-Si gate and dummy gate oxide are removed, and the sacrificial SiGe is etched away to reveal the Si channels. Gate dielectrics (SiO_2 and HfO_2) and the full gate metal stack, including work function metals, are deposited using the replacement metal gate (RMG) process. A capping dielectric is then deposited before implementing the full back-end-of-line (BEOL) interconnect stack. Fig. 4 illustrates the first horizontal metal layer (Mint) with its corresponding vias to the gate or contact (Vint).

B. INTEGRATION FLOW OF BACKSIDE POWER RAIL (BS-PR) WITH BACKSIDE CONTACT (BSC)

The process flow for circuits using BS-PR (with BSC) follows similar steps to the BPR flow up until the formation of the poly-Si gate and the outer- and inner-spacers. At the stage where the S/D trenches are opened (by removing the Si/SiGe stack in the S/D regions), an additional etch into the substrate pillar is performed and filled with a placeholder dielectric for the BSC. The subsequent steps—S/D epitaxial regrowth, contact metallization, RMG, and BEOL—remain the same as in the BPR flow [14]. See Fig. 5.

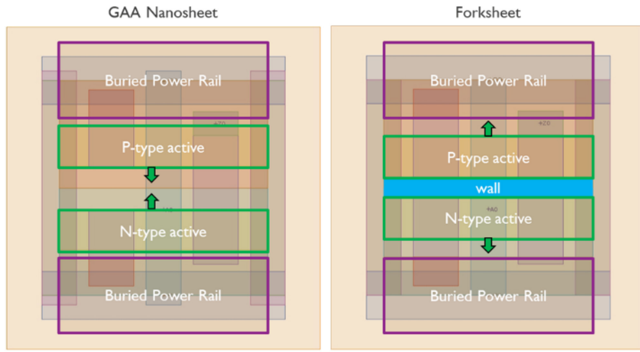

FIGURE 6. Design rules for varying W_{sh} in GAA-Nsh and Fsh. Nsh position is anchored by its minimal distance towards BPR. Fsh position is anchored by the Fsh wall.

To access the placeholder dielectric, the wafer is flipped upside down, and the substrate is thinned. The remaining substrate pillars beneath the RMG are then replaced with bottom dielectric isolation (BDI). In the S/D trenches, the placeholder dielectric is replaced with backside contact metallization (BSC). Following this, the first backside interconnect layer (BSM) is formed, allowing for the construction of a full backside BEOL interconnect stack [6], [15], [16].

C. DESIGN RULES FOR NANOSHEET AND FORKSHEET ARCHITECTURES

Starting from a Si/SiGe superlattice, the sacrificial SiGe layers can be etched away to release the Si sheets. In order to perform this SiGe etch efficiently, sufficient space next to the active region is required. In case of Nsh devices, the SiGe etch happens from both sides of the active. In case of Fsh devices, the removal of the sacrificial SiGe can only happen from the cell boundary side. Similar constraints must be considered for proper RMG. In either case (Nsh or Fsh), when performing the RMG for PMOS, the NMOS device must be protected by a dielectric deposition; and vice-versa. In case of Nsh devices, the boundary of N/P RMG is in the middle of the N-P separation. Considering RMG misalignment and overlay errors, the N-P distance should be sufficiently large ($\geq$18 nm). Due to the presence of a dielectric wall in Fsh, these RMG-related issues are less of a concern. Thus, Fsh wall can be narrower than Nsh N-P separation [4].

Given the FS processing of BPR with a typical width of ~30 nm and a minimal distance of active-to-BPR of 3 nm (Dabpr), sufficient room is provided at the cell boundary for successful SiGe etch and RMG. Keeping CH constant at 5 pitches of the first horizontal metal track (5T = 5×Mx), we notice that the design rules are somewhat different for Nsh and Fsh devices (See Fig. 6).

Assuming BPR and a minimal active-to-BPR distance, from an RMG processing point-of-view, it is preferable to maximize the N-P distance in case of Nsh devices. This immediately leads to the Nsh-specific design rule that active

TABLE 1. Design rules and assumed dimensions.

Min N-P separation	18 nm	Cell height (CH)	5 Mx	Channel length (Lg)	14 nm
Min Fsh wall thickness	8 nm	Mint pitch (Mx)	24/18 nm	Gate spacer thickness	5 nm
Min BPR width (WBPR)	30 nm	BPR width (WBPR)	32 nm	Gate cap diel. height	15 nm
Min active-BPR dist. (Dabpr)	3 nm	Gate pitch (CGP)	42 nm	Vint height	18 nm
Min CT tip-to-tip (T2TM0)	18 nm	#sheets / device (NNS)	3	Mint height	27 nm
Min VBPR size (YVBPR)	12 nm	Sheet offset (ONS)	10 nm	VBPR or BSC height	20 nm
Min gate cut (GC)	16 nm	Sheet pitch (PNS)	15 nm	Power Rail height	90 nm
Min gate extension (GE)	9 nm	Gate SiO_2/HfO_2	1/1.3 nm	STI depth	70 nm

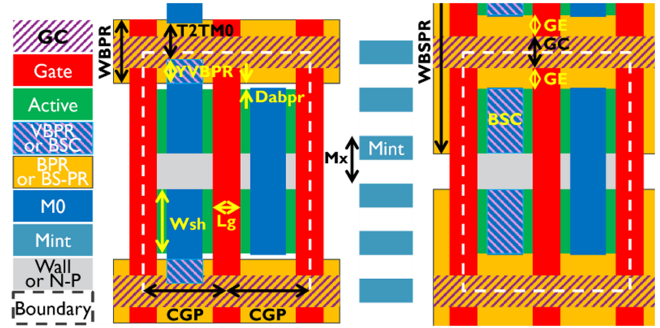

FIGURE 7. Inverter INVD1 layout with BPR (left) & BS-PR (right).

is anchored with respect to its minimal distance to BPR. As a result, further W_{sh} increase will reduce the N-P separation ($\geq$18 nm). In contrast, Fsh devices are anchored by the Fsh dielectric wall in the centre of the cell. Hence, further Fsh active width enlargement shrinks the distance between active and BPR ($\geq$3 nm). See Table 1 for extra dimensions.

Figure 7 shows that minimal BPR width is determined by the minimal tip-to-tip distance (T2T) of the contact metallization (M0) and the size of the via connecting M0 to BPR (VBPR): $\min(WBPR) = \min(T2TM0) + \min(YVBPR) = 30\ nm$ The largest active region is hence determined by its minimal distance to BPR (3 nm):

$$\begin{aligned} &\max(active\ for\ BPR,\ \ incl\ N-P) \\ &\quad = CH - \left[\min(WBPR) + 2 \times \min(Dabpr)\right] \\ &\quad = CH - 36\ nm \end{aligned} \tag{1}$$

On the contrary, BS-PR must extend underneath the active region to ensure sufficient width for the BSC to the bottom of the S/D epi. In this case, the maximum active region is determined by the gate cut (GC) and gate extensions (GE) at the cell boundary:

$$\begin{aligned} &\max(active\ for\ BS-PR,\ \ incl\ N-P) \\ &\quad = CH - [\min(GC) + 2 \times \min(\mathrm{GE})] \\ &\quad = CH - 34\ nm \end{aligned} \tag{2}$$

Notice that the maximum active region can be 2 nm larger in case of BS-PR vs BPR. This would only result in 1 extra nm per device type (NMOS, PMOS).

Contact metallization (M0) extensions with respect to active are determined by: (1) the connections to BPR (Dabpr + YVBPR), (2) the full interception with overhanging horizontal metal lines (Mint) and (3) the M0 tip-to-tip design rule [6], [17], [18].

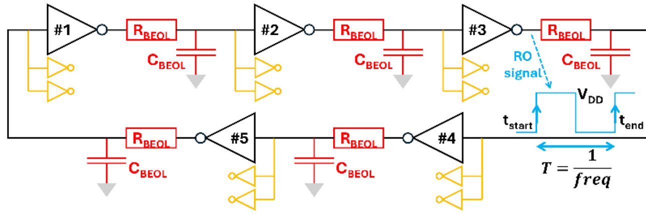

FIGURE 8. Inverter INVD1 based ring oscillator (RO) setup with BEOL load and 3-fold fanout.

III. TCAD AND DTCO FRAMEWORK

All simulations conducted in this study employed a TCAD framework for DTCO analysis, as described in [19]. The simulations for both NFET and PFET TCAD devices utilized the drift-diffusion/density gradient (DD/DG) equations, in conjunction with the Poisson equation and current continuity equations. The DG models incorporate quantum correction potentials. The mobility models employed in the simulations include the Lombardi, Philips, and ballistic models. Mobility parameters were calibrated using imec hardware data [20], [21]. Epi-induced stress of 0.6 GPa and −1.6 GPa were considered for NFET and PFET, respectively [22], [23]. The five-stage INVD1 RO simulations were performed using the SPICE-based DTCO flow incorporating back-end-of-line (BEOL) load parameters (R_{BEOL} = 748 Ω and C_{BEOL} = 560 aF) and a fanout of three (Fig. 8). To isolate the front-end-of-line (FEOL) impact, the BEOL wiring load was assumed to be independent of the metal pitch Mx. Power and frequency data were extracted from these circuits, along with intermediate values such as effective resistance (R_{eff}) and effective capacitance (C_{eff}). The specific device dimensions are presented in Table 1. For a comprehensive description of the models and parameters used, refer to [19], [20]. The procedure for extracting ring oscillator circuit figures of merit is outlined below for completeness.

To distinguish power consumption of the cells-under-test (here: INVD1 #1-5) from their fan-out neighbors (here: indicated in orange), two separate supply voltage (V_{DD}) networks are assumed. When referring to V_{DD}, we specifically mean the power source of the cells-under-test. If the RO loop is opened, the circuit becomes a chain and all signals find a stable bias point. In this case, the average quiescent current per stage can be measured:

$$I_{DDQ} = \frac{\langle I_{DD}^{chain} \rangle}{N_{stages}} \tag{3}$$

Given that all stages leak simultaneously, division by the number of stages N_{stages} is required. Closing the RO loop, we can also measure the average active current per stage:

$$I_{DDA} = \frac{1}{T} \int_{t_{start}}^{t_{end}} I_{DD}(t)\ dt \tag{4}$$

This is the average current delivered by the V_{DD} power rail. Given that only one stage is switching at any given time, division by N_{stages} is unnecessary. Active power consumption is given by:

$$P_{avg} = V_{DD} \times I_{DDA} \tag{5}$$

Knowing that one full period T of the RO signal corresponds to 2 full roundtrips (rising edge and falling edge), the delay per stage can be determined by:

$$delay_{stage} = \frac{T}{2 \times N_{stages}} = \frac{1}{2 \times N_{stages} \times freq} \tag{6}$$

The stage delay can also be mapped unto an equivalent RC network:

$$delay_{stage} = \ln(2) \times R_{eff} \times C_{eff} \tag{7}$$

Matching the stage delay to the time needed to charge C_{eff} up to $V_{DD}/2$ results in the factor ln(2).

The effective resistance relates to the average current delivered by the V_{DD} power rail:

$$R_{eff} = \frac{V_{DD}}{I_{DDA} - I_{DDQ}} \tag{8}$$

The corresponding effective capacitance is then given by:

$$C_{eff} = \frac{delay_{stage}}{\ln(2) \times R_{eff}} \tag{9}$$

These effective resistance and capacitance are more intuitive to interpret. Mind that mapping a multi-pole system unto a single-pole system means that R_{eff} is also influenced by capacitive components and that C_{eff} is also influenced by resistive components.

IV. RESULTS

A comprehensive DTCO study was carried out to compare GAA-Nsh and Fsh devices for two Mx—18 nm and 24 nm—across a range of N and W_{sh}. The study evaluated two contact schemes: BPR and BS-PR with BSC. For Fsh, the impact of T_{wall}, k, and CR are also investigated, on both transistor and RO level. Wide ranges are applied to the nominal values of T_{wall} = 8 nm, k = 7 (SiN) and CR = 10^{-9} Ω.cm^2. Additionally, two new Fsh variants—GAA-Fsh and asymmetric Fsh—were explored, focusing specifically on the 24 nm metal pitch.

As mentioned in the design rules, for GAA-Nsh devices, increasing W_{sh} impacts the N-P separation, whereas for Fsh devices, it affects the distance to the buried power rail (BPR) (Fig. 6). The gate extension (beyond the active region) remains constant, resulting in a W_{sh}-dependent gate width (W_G) for Fsh and a fixed W_G for Nsh devices (Fig. 9).

A. DEVICE ANALYSIS OF GAA-NSH AND FSH ARCHITECTURES AT MX = 18 NM

The GAA-Nsh and Fsh devices were benchmarked at Mx = 18 nm, in line with the A14 technology node design rules, which specify a CH = 90 nm with 5 metal tracks. According to these design rules, the maximum nanosheet W_{sh} for

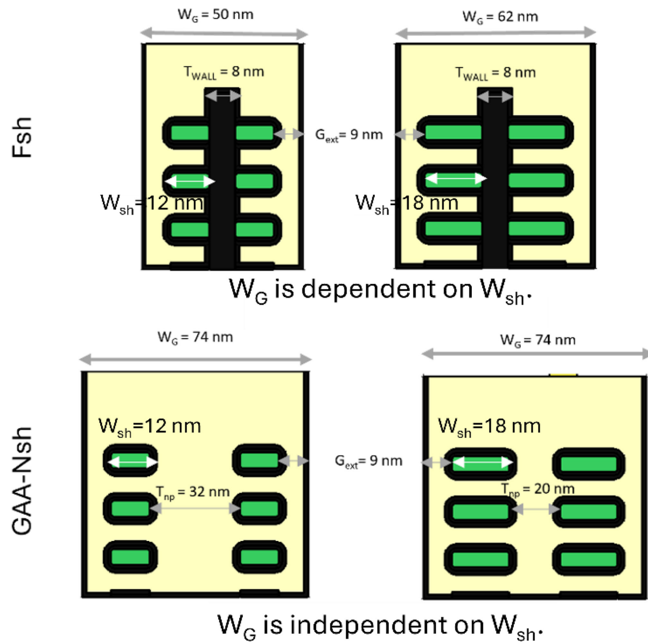

FIGURE 9. 2D cross section of Fsh and GAA-Nsh showing the variation of W_G with change in W_{sh}; example for Mx 24 nm

GAA-Nsh is restricted to 17 nm to maintain a minimum N-P separation of 18 nm. In contrast, Fsh devices can extend this maximum W_{sh} to 22 nm when a thin wall (T_{wall} = 8 nm) is utilized, providing Fsh with a potential performance advantage over Nsh. However, increasing the T_{wall} results in a reduced maximum W_{sh} for a fixed CH. Additionally, the application of a BS-PR with a BSC contacting scheme permits an additional 2 nm extension in W_{sh} for both GAA-Nsh and Fsh devices.

This study benchmarks these devices across varying W_{sh} (from 10 nm to $W_{sh,max}$) and N (2 to 5), evaluated at BPR and BSPR with BSC contacting scheme.

Figure 10 presents the sub-threshold swing (SS) and on-current (I_{ON}) characteristics for GAA-Nsh and Fsh NFET devices as a function of W_{sh} and varying N, based on TCAD simulations. Similar trends were observed in PFET simulations, although those results are not shown for brevity. I_{ON} is extracted at a fixed I_{OFF} = 1 nA and V_{DD} = 0.7 V, and the values are expressed as a percentage, using the GAA-Nsh device with W_{sh} = 19 nm and N = 3 as the reference.

In Fig. 10a and 10b, we can see that GAA-Nsh achieves better SS than Fsh at smaller W_{sh}. This is due to the superior electrostatic control provided by the GAA architecture, which fully surrounds the channel, offering more precise control over the charge carriers. As W_{sh} increases, SS worsens for both devices, primarily due to weaker gate control and increased parasitic capacitance. For GAA-Nsh, SS rises sharply, going from 68 to 73 mV/decade, whereas Fsh shows a more gradual increase from 74 to 75 mV/decade. The faster degradation in GAA-Nsh is likely due to the diminishing effect of full gate control over larger channels, whereas Fsh is less dependent on complete gate coverage. Despite this, GAA-Nsh maintains a better SS across the entire width range thanks to its stronger initial electrostatic control.

SS also shows slight improvement with an increase in N for both architectures. This is due to the non-uniform potential distribution across the sheets, where the lower sheet experiences a lower source resistance, effectively turning on earlier than the higher sheets, which marginally improves SS [20].

In Fig. 10c and 10d, we see a clear linear relationship between I_{ON} and W_{sh} for both GAA-Nsh and Fsh devices. GAA-Nsh has a higher y-intercept, indicating better drive current at smaller W_{sh}, thanks to its stronger gate control. However, as W_{sh} increases, Fsh devices show a steeper slope, meaning I_{ON} improves more rapidly with W_{sh} compared to GAA-Nsh. This suggests that Fsh benefits more from increased W_{sh}, likely due to better scalability in gate control at larger dimensions. The performance of Fsh matches that of GAA-Nsh at a W_{sh} of 23 nm for Fsh and 19 nm for GAA-Nsh. However, since Fsh can scale up to W_{sh} = 24 nm, it provides an additional I_{ON} gain of up to 7-8%, which holds true for all N. The slope of I_{ON} vs. W_{sh} also increases with N for both architectures. As more sheets are added, the effective channel area increases, allowing for greater current drive. The combined effect of expanded channel area and enhanced gate control results in steeper I_{ON} slopes at higher N values. Furthermore, the percentage increase in I_{ON} across different N for both GAA-Nsh and Fsh follows a clear trend: a 41-44% rise from N = 2 to N = 3, 27-29% from N = 3 to N = 4, and 22% from N = 4 to N = 5. This aligns with the increase in W_{eff}, which grows by 50% from N = 2 to N = 3, 33% from N = 3 to N = 4, and continues to diminish at higher N. The significant initial W_{eff} expansion leads to higher current gains, which taper as W_{eff} growth slows.

In summary, while GAA-Nsh has an advantage in I_{ON} at smaller widths, Fsh shows stronger improvement as W_{sh} increases, closing the performance gap at larger dimensions. GAA-Nsh retains better SS throughout, but Fsh's gradual SS degradation and faster I_{ON} improvement make it competitive, especially at larger W_{sh} where it extends up to 24 nm.

B. RO ANALYSIS OF GAA-NSH AND FSH ARCHITECTURES AT MX = 18 NM

Using the devices from Figure 10 in the RO setup shown in Figure 8, we evaluate the corresponding INVD1 circuit speed for both contact schemes (BPR and BS-PR with BSC). Figure 11 shows the INVD1 C_{eff} and circuit speed for 0.7 V V_{DD} and fixed I_{OFF} = 1 nA, expressed as percentages relative to the GAA-Nsh device with W_{sh} = 19 nm and N = 3. From Fig. 11, it's clear that the different contact schemes do not significantly affect circuit performance. While BS-PR with BSC reduces local interconnect M0 extensions (smaller $C_{G\text{-}M0}$), the increased fringe fields between gate and BS-PR & BSC undo the reduced $C_{G\text{-}M0}$,

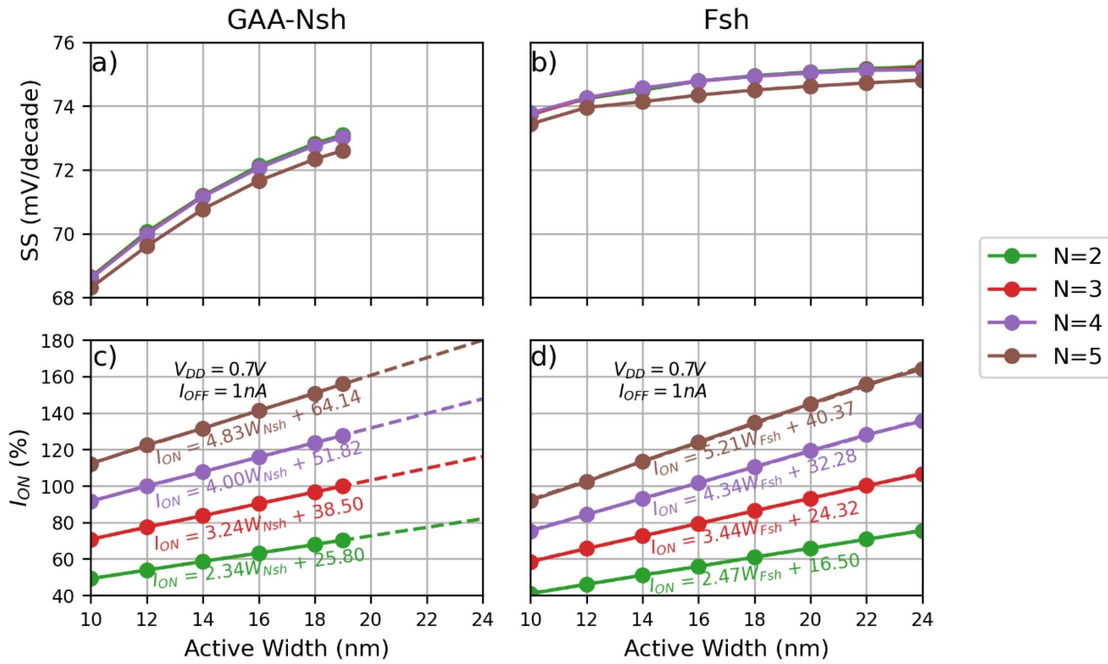

FIGURE 10. TCAD device results for NMOS on-current and subthreshold slope (SS) for a wide range of active widths (W_{sh}) and number of stacked sheets (N); for Mx = 18 nm. Reference device is 3-sheet GAA-Nsh with 19 nm active.

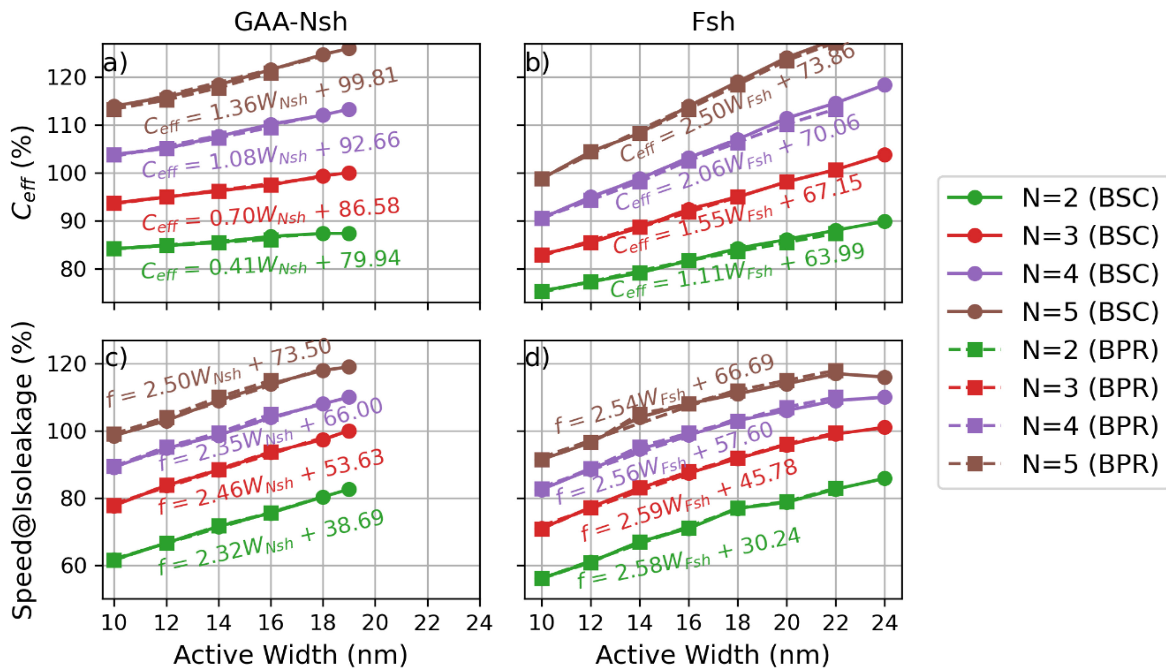

FIGURE 11. INVD1 speed (at iso-leakage) for a wide range of active widths (W_{sh}) and number of stacked sheets (N). No noticeable difference between BPR and BS-PR with BSC; for Mx = 18 nm. Reference device is 3-sheet GAA-Nsh with 19 nm active.

as shown in Figs. 11a and 11b, where negligible differences in C_{eff} are observed between the two contact schemes.

In Figs. 11a and 11b, the C_{eff} behaviour for both GAA-Nsh and Fsh shows distinct trends as a function of W_{sh} and N. In general, both the intrinsic channel capacitance ($C_{channel}$) and the parasitic gate-to-source/drain capacitance ($C_{G\text{-}S/D}$) increase linearly with W_{sh}, leading to C_{eff}'s linearity with W_{sh}. Due to the distinct layout difference between GAA-Nsh and Fsh (Fig 6), C_{eff} rises slower for GAA-Nsh than for Fsh. In GAA-NSh, a growing W_{sh} leads to a reduced N-P separation; due to GAA-Nsh's fixed gate polygon length W_G. As W_{sh} increases, the total gate sidewall area actually decreases due to the larger holes cut out by the sheets and their surrounding gate oxides. Thus, for GAA-Nsh, the

C_{eff} rises less fast than for Fsh, where the gate polygon length W_G grows by the same amount as W_{sh}. As a result, the rise in GAA-Nsh C_{eff} is moderate, remaining relatively controlled across all widths. At W_{sh} = 10 nm, GAA-Nsh exhibits a higher C_{eff} compared to Fsh, with a gap of 12-15% across different sheet counts, largely because GAA-Nsh has a fixed W_G, leading to higher initial parasitic C. However, as W_{sh} increases to 16 nm, the gap narrows, and GAA-Nsh maintains a 5-7% higher C_{eff}. At W_{sh} = 19 nm for GAA-Nsh and W_{sh} = 24 nm for Fsh, Fsh surpasses GAA-Nsh in C_{eff}, with Fsh being 12% larger at higher N. This shift occurs because, in Fsh, C_{G-D2D} remains constant as W_G grows with W_{sh}, whereas GAA-Nsh sees a reduction in $C_{G\text{-}D2D}$, leading to a more gradual increase in C_{eff} (11a). Here, D2D indicates the part of the M0 connection that bridges between the NMOS drain and the PMOS drain, closing the output of the inverter INVD1.

These differences in C_{eff} directly explain the speed behaviour observed in Figs. 11c and 11d. For GAA-Nsh, the linear increase in speed with W_{sh} can be attributed to the moderate rise in C_{eff}, where the balance between the increasing $C_{channel}$ and decreasing C_{G-D2D} results in steady speed improvements. As parasitic C are reduced, the drive strength improves more rapidly than the increase in C_{eff} would suggest, leading to higher circuit speed.

In contrast, for Fsh, the speed saturates at larger W_{sh}, as seen in Fig. 11d. This saturation is due to the sharper rise in C_{eff} with W_{sh}, as parasitic C continue to grow with the increasing W_G. At smaller widths, GAA-Nsh outperforms Fsh, with a 7-12% speed advantage at W_{sh} = 10 nm, but as W_{sh} increases to 16 nm, the gap narrows to 6-7.5%. At W_{sh} = 22 nm for Fsh and W_{sh} = 19 nm for GAA-Nsh, Fsh initially surpasses GAA-Nsh in speed for lower N, being 3.4% faster at N = 2 and 0.6% faster at N = 3. However, at higher N (N = 4 and N = 5), GAA-Nsh reclaims the lead, outperforming Fsh by 3-5%. At W_{sh} = 24 nm, Fsh begins to saturate, and its performance even starts to decrease at higher N, allowing GAA-Nsh to maintain an advantage. Thus, the trends in C_{eff} directly correlate with the speed performance, where GAA-Nsh benefits from reduced parasitic $C_{G\text{-}S/D}$, while Fsh experiences a more pronounced increase in C_{eff}, leading to its speed saturation.

C. OPTIMAL NUMBER OF STACKED SHEETS

In our earlier calculations, the GAA-Nsh device with W_{sh} = 19 nm and N = 3 was consistently chosen as the reference device. The reasoning for this becomes clear when evaluating circuit speed at iso-power, as shown in Fig. 12. Here, we focus on determining the optimal number of stacked sheets based on speed and power consumption. To make this comparison, the power level is fixed at 39 μW, which corresponds to the power consumed by the GAA-Nsh reference device at V_{DD} = 0.7 V. This result confirms that this particular GAA-Nsh configuration provides the best balance between speed and power efficiency, explaining why it was selected as the reference.

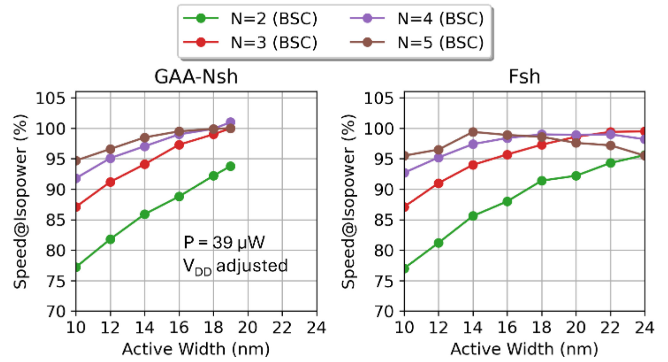

FIGURE 12. INVD1 speed (at iso-power) for GAA-Nsh and Fsh for various active widths and number of stacked sheets.

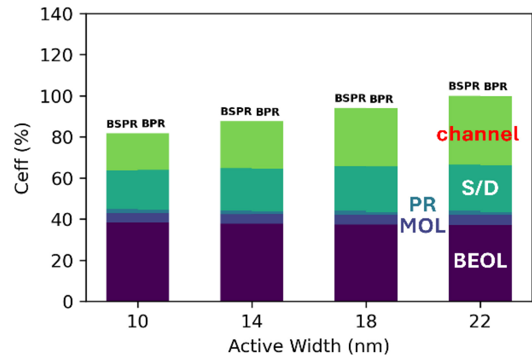

FIGURE 13. C_{eff} contributions of Fsh with 3 sheets for various active widths (normalized to 22 nm active width).

When comparing different W_{sh} and N, GAA-Nsh shows a steady increase in speed with W_{sh}, reaching 92% at N = 2 and 100% at N = 3-5 by W_{sh} = 19 nm, with diminishing returns beyond 16 nm. In contrast, Fsh has a more gradual speed increase, with N = 2 rising from 75% at 10 nm to 85% at W_{sh} = 24 nm, and N = 3-5 reaching 100% between W_{sh} =14-20 nm. However, for N = 4-5, speed starts to decrease beyond 20 nm, indicating saturation. Overall, GAA-Nsh performs better at smaller W_{sh}, while Fsh scales more gradually but experiences slight speed reductions at larger W_{sh} due to parasitics.

D. CEFF BREAK-UP INTO FEOL/MOL/BEOL CONTRIBUTIONS

By consecutively removing circuit components, their relative contribution to overall C_{eff} can be estimated. The removal order is: BEOL, middle-of-line (MOL), power rails (PR), S/D epi, and contact. The remaining capacitance represents the $C_{channel}$. C_{eff} contributions are shown for different W_{sh} (Fig. 13) and N values (Fig. 14).

Across W_{sh} and N, BEOL contributes approximately 40% to C_{eff}, while MOL and PR combined account for about 5%. For the reference Fsh device (N = 3, W_{sh} = 22 nm), $C_{G-S/D}$ makes up around 20% of C_{eff}, with the $C_{channel}$ contributing 35%. Both $C_{G-S/D}$ and $C_{channel}$ scale linearly with N and W_{sh}. Notice that there is little difference in C_{eff} between BPR and BS-PR with BSC.

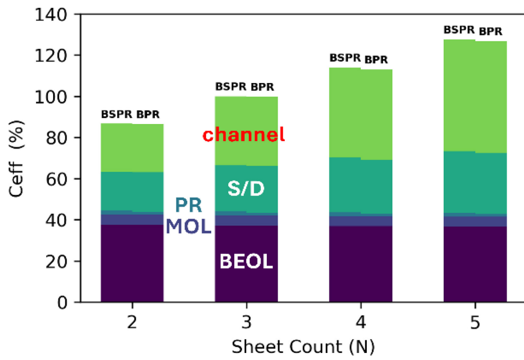

FIGURE 14. C_{eff} contributions of Fsh with 22 nm active width for various number of stacked sheets (normalized to N = 3).

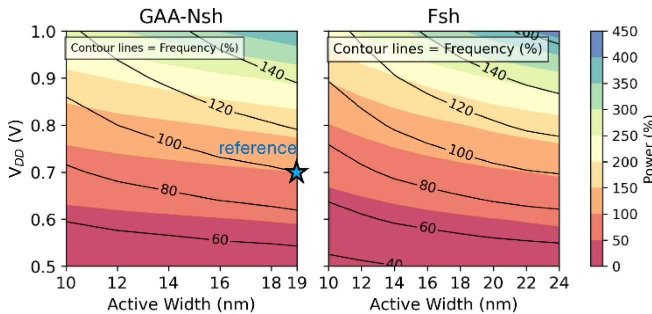

FIGURE 15. INVD1 speed and power for 3-sheet GAA-Nsh and Fsh for various W_{sh} and V_{DD} (for Mx = 18 nm). The absolute reference is GAA-Nsh with W_{sh} =19 nm at 0.7V.

These findings suggest that circuit speed improvements are best achieved by lowering BEOL capacitance and $C_{G\text{-}S/D}$.

E. POWER-PERFORMANCE LANDSCAPE FOR WIDE RANGE OF ACTIVE WIDTHS AND VDD

Figure 15 presents the power and frequency results from RO simulation for both GAA-Nsh and Fsh architectures at N = 3, across different W_{sh} and V_{DD}. The contour lines represent the frequency (speed) of the RO in percentage, while the color gradient indicates power consumption, also in percentage. All data is normalized to 3-sheet 19 nm wide GAA-Nsh at 0.7 V V_{DD}. The x-axis shows W_{sh}, and the y-axis reflects V_{DD}.

At constant V_{DD} of 0.7 V, the 100% speed mark of our 19 nm reference GAA-Nsh can be matched by the 23 nm Fsh; albeit at a slightly higher power consumption for Fsh (+3%). However, if we lower our speed target to 80%, the 11 nm GAA-Nsh matches with 13 nm Fsh; respectively with a power consumption of 80% and 74%. By lowering the speed target, Fsh reduces its needed active width overhead from 4 nm to 2 nm w.r.t. GAA-Nsh. Moreover, 13 nm Fsh consumes 7.5% less power than 11 nm GAA-Nsh.

At constant V_{DD} of 0.9 V, the 140% speed mark matches between 18.5 nm GAA-Nsh and 21 nm Fsh; both at a similar power consumption at around 262%. Again, if we lower our speed target to 120%, we see that 13 nm GAA-Nsh corresponds with 14 nm Fsh; at a respective power consumption of 219% and 200%. Again, we see a benefit in lowering the speed target, where the Fsh's necessary active width overhead reduces from 2.5 nm to just 1 nm. Moreover, 14 nm Fsh seems to be consuming 10% less power w.r.t. 13 nm GAA-Nsh.

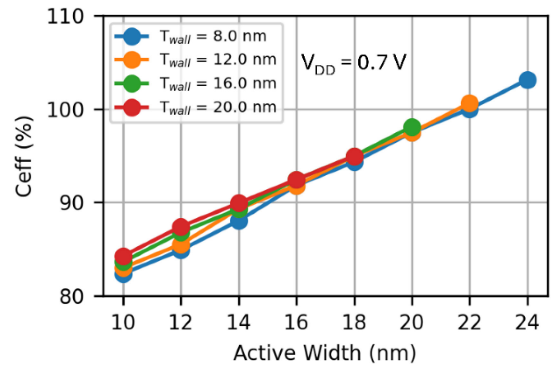

FIGURE 16. Impact of Fsh wall thickness (T_{wall}) on C_{eff}, for various active widths.

At constant W_{sh} of 10 nm, both devices can reach the same speed target, albeit at 40 mV higher V_{DD} for Fsh w.r.t. GAA-Nsh. This relation seems to hold for several speed targets; ignoring the corresponding power consumptions.

If we now increase our active width to the constant value of 18 nm, Fsh seems to require 20 mV higher V_{DD} than GAA-Nsh to achieve the 60% speed target. Going up to the 100% & 140% speed marks, Fsh respectively needs 28 mV & 33 mV higher V_{DD} than GAA-Nsh.

In summary, at nominal V_{DD} of 0.7 V, Fsh requires ∼20% wider active to match GAA-Nsh speed. Increasing V_{DD} to 0.9 V, reduces Fsh's required active width overhead to ∼10% to match GAA-Nsh speed. Depending on the speed target, Fsh's power consumption is either equal to or 7-10% lower than GAA-Nsh. This makes Fsh more energy efficient than GAA-Nsh, esp. at low W_{sh} and high V_{DD}.

F. CHANGING FORKSHEET WALL THICKNESS (TWALL)

The impact of T_{wall} in Fsh devices on circuit performance was studied for the BS-PR with BSC configuration, across various W_{sh} with N = 3. In this study, the Fsh device with T_{wall} = 8 nm and W_{sh} =22 nm was considered as the reference, and all quantities were normalized to this device. Figure 16 illustrates the relationship between C_{eff} and W_{sh} for the Fsh architecture at varying T_{wall}. Notice that the maximally possible active width (W_{shmax}) reduces as T_{wall} increases, due to our fixed CH.

The results demonstrate a linear increase in C_{eff} as W_{sh} expands from 10 nm to W_{shmax} for all T_{wall} values, confirming that larger W_{sh} increase the channel area and, consequently, the capacitance. The impact of wall thickness is more subtle. For example, for W_{sh} = 10 nm, T_{wall} = 20nm results in a C_{eff} of approximately 84%, compared to around 81% for T_{wall} = 8nm: thus C_{eff} rises ∼4%. This indicates that thicker walls slightly raise the $C_{G\text{-}S/D}$ by increasing the W_G, which is defined as $2W_{sh} + T_{wall} + 2GE$, where GE is

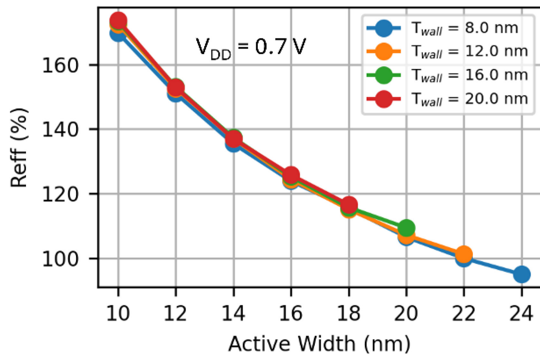

FIGURE 17. **Impact of Fsh wall thickness (T_{wall}) on R_{eff}, for various active widths.**

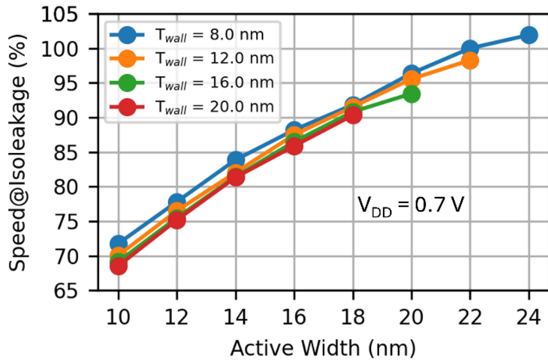

FIGURE 18. **Impact of Fsh wall thickness (T_{wall}) on INVD1 speed (at iso-leakage), for various active widths.**

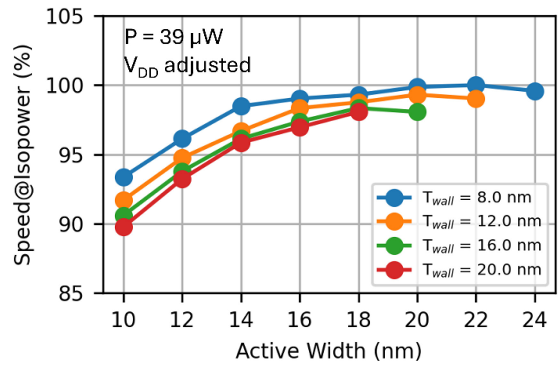

FIGURE 19. **Impact of Fsh wall thickness (T_{wall}) on INVD1 speed (at iso-power), for various active widths.**

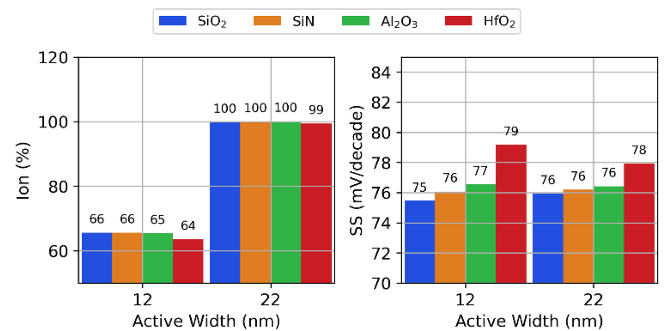

FIGURE 20. **Impact of Fsh wall permittivity on NMOS on-current and subthreshold slope (SS), for narrow & wide active.**

the gate extension. However, as W_{sh} increases, the relative influence of T_{wall} diminishes. This suggests that while T_{wall} influences W_G and thus $C_{G\text{-}S/D}$—its effect is secondary to that of W_{sh}.

Additionally, thicker walls increase the N-P distance, leading to longer D-D connections over the Fsh wall, where the local interconnect metal M0 is at its thinnest, leading to higher R_{eff}, as shown in Figure 17. For 10 nm W_{sh}, R_{eff} increases by 2.3% going from T_{wall} of 8 nm up to 20 nm. Thus, the primary driver of C_{eff} and R_{eff} in these devices remains W_{sh}, with T_{wall} playing a secondary role.

Figure 18 shows the corresponding INVD1 speed (at iso-leakage) for various W_{sh} and Fsh T_{wall}. Similar trend as for C_{eff} can be observed, with minimal T_{wall} (here 8 nm) performing best, while also providing the largest range of W_{sh}.

If we now plot speed at iso-power (Fig. 19), 4% speed penalty occurs when increasing T_{wall} from 8 nm to 20 nm, at a constant W_{sh} of 10 nm. Similar speed loss can be observed for other W_{sh}. Same speed (here 94%) can be maintained for {T_{wall}, W_{sh}} being {8 nm, 10 nm} and {20 nm, 13 nm}. In other words, same speed and power can be maintained if active width is increased by 0.25 nm per nm increase of T_{wall}.

G. CHANGING FORKSHEET WALL PERMITTIVITY

In this section, we investigate the impact of Fsh wall permittivity on device characteristics and circuit performance. Materials with different dielectric permittivities are considered: SiO_2 (3.9), SiN (7), Al_2O_3 (12) and HfO_2 (22).

As shown in Fig. 20, increasing the wall permittivity (k) in Fsh devices leads to a significant deterioration in SS, while the impact on I_{ON} is minimal. At W_{sh} = 12 nm, SS rises from 75.5 mV/decade for SiO_2 to 79.2 mV/decade for HfO_2, and at W_{sh} = 22 nm, it increases from 75.9 mV/decade to 77.9 mV/decade. This degradation in SS indicates a reduced gate control of the channel, caused by stronger fringing fields in high-permittivity materials, resulting in higher parasitic capacitances. However, I_{ON} remains largely unaffected, decreasing slightly from 65.6% (SiO_2) to 63.6% (HfO_2) at W_{sh} = 12 nm, and showing almost identical performance near 100% for all materials at W_{sh} = 22 nm. For wider sheets, the relative contribution of the channel-wall facet diminishes w.r.t. the total effective channel width (W_{eff}). Therefore, changes in k of the wall have less impact on the overall drive strength and gate control of the channel.

Thus, high-permittivity materials negatively impact SS, but their effect on I_{ON} is minimal. Although the I_{ON} remains largely unaffected by changes in k value of the wall, the RO simulation results in Figure 21 reveal that the impact on speed, R_{eff}, and C_{eff} is not negligible.

The Speed at Iso-leakage decreases with increasing k, with HfO_2 showing the slowest speed at both 12 nm (72%) and 22 nm (96%), while SiO_2 achieves the highest speed (80% at 12 nm and 102% at 22 nm). This trend can be attributed to

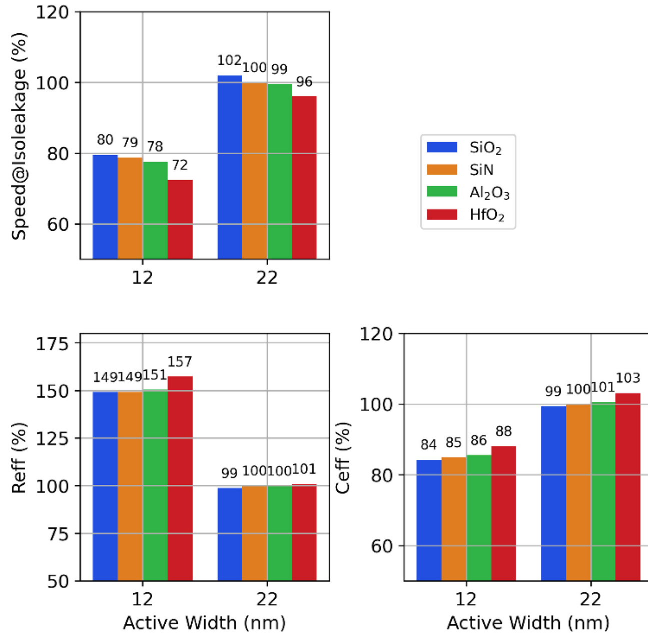

FIGURE 21. Impact of Fsh wall permittivity on INVD1 speed (at iso-leakage), corresp. R_{eff} & C_{eff}, for narrow & wide active.

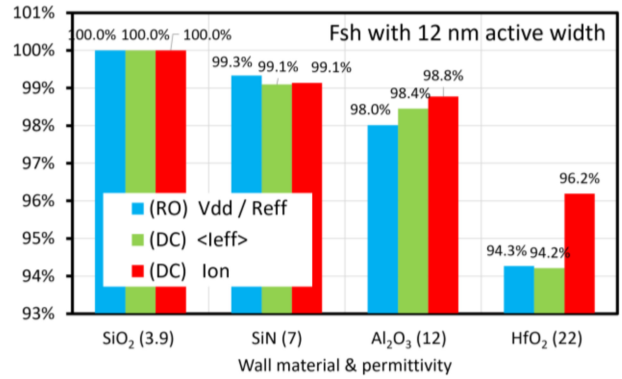

FIGURE 22. Rather than I_{ON}, DC device $<I_{eff}>$ is a better predictor of RO R_{eff} behaviour. Data for narrow active width (12 nm).

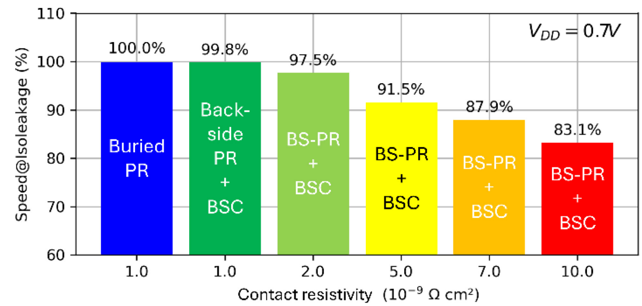

FIGURE 23. Impact of BSC contact resistivity on INVD1 speed (at iso-leakage). Data shown for Fsh; similar for GAA-Nsh.

the considerable rise in C_{eff} where HfO_2 shows the highest values—88% at 12 nm and 103% at 22 nm.

R_{eff} shows a significant increase with higher k value. For instance, at 12 nm, HfO_2 results in 6% higher R_{eff}, compared to SiO_2. While I_{ON} device current corresponds to full saturation $\{V_{GS},V_{DS}\} = \{V_{DD},V_{DD}\}$, the overall switching current of the INVD1 (RO $I_{eff} = V_{DD}/R_{eff}$) is composed of the charging current of the capacitive load and the cell's own short circuit current; dominated by the $(V_{DD}/2\text{-}V_t)^2$ terms. This RO situation can be approximated by the average DC effective device current (DC $<I_{eff}>$) for $\{V_{GS},V_{DS}\}=\{V_{DD}/2,V_{DD}\}$ & $\{V_{DD},V_{DD}/2\}$; for NMOS and PMOS. For fixed I_{OFF}, in first approximation, the ratio V_t/SS remains constant. If SS increases, V_t increases by a similar factor. Device $<I_{eff}>$ is more affected by V_t-shift than I_{ON}; due to I_{eff}'s smaller effective V_{GS} overdrive $(V_{DD}/2\text{-}V_t)$ vs I_{ON} $(V_{DD}\text{-}V_t)$. Fig 22 shows that DC $<I_{eff}>$ is a better proxy for RO I_{eff} than I_{ON}.

Thus, while the I_{ON} remains stable, the combined effects of increased C_{eff} and R_{eff} considerably degrade performance, particularly for materials with higher k value like HfO_2, making lower-k value materials such as SiO_2 preferable for improved circuit speeds, especially at smaller W_{sh}.

H. BACKSIDE CONTACT RESISTIVITY

Due to its larger overall contact area, BPR offers slightly lower access resistance compared to BS-PR with BSC. However, the newer backside processing technique introduces uncertainty about whether the same contact resistivity as in frontside contacts can be achieved. To account for this, we evaluated several BSC contact resistivities, ranging from 10^{-9} $\Omega.cm^2$ (equivalent to FS) to its 10-fold value. When the BSC resistivity is 10 times that of FSC (ρ(BSC)/ρ(FSC) = 10), the circuit speed decreases by 17%, as shown in Fig. 23. This relationship appears approximately linear: speed penalty (%) = 1.7 × ρ(BSC)/ρ(FSC).

I. ACTIVE WIDTH STUDY AT METAL PITCH, MX = 24 NM

In the previous analysis, we compared GAA-Nsh and Fsh architectures at Mx = 18 nm. While Fsh offered an advantage by reducing parasitic capacitance due to its unique design rules, it suffered from poor gate control, causing it to underperform compared to GAA-Nsh at smaller W_{sh}. The performance gap closed at larger W_{sh}, where both architectures were comparable, although we observed some extra power consumption in Fsh without offering any significant advantage over GAA-Nsh. To address this, we proposed a GAA-Fsh structure, which retains the design benefits of Fsh but improves gate control. In this configuration, the Fsh wall is etched along the width and filled with a gate stack, forming a GAA setup. However, this approach is only feasible with a thicker wall, which can be achieved at larger Mx. Therefore, we now benchmark Nsh, Fsh, and GAA-Fsh architectures at Mx = 24 nm and a CH = 120 nm across 5 metal tracks. T_{wall} of these devices was maintained at 20 nm, with a gate-S/D separation of 10 nm for GAA-Fsh N/P devices (Fig. 2a), while the W_{sh} was varied from 15 nm to 30 nm. For this study, we consider Fsh device with W_{sh} = 21 nm and N = 3 as the reference device.

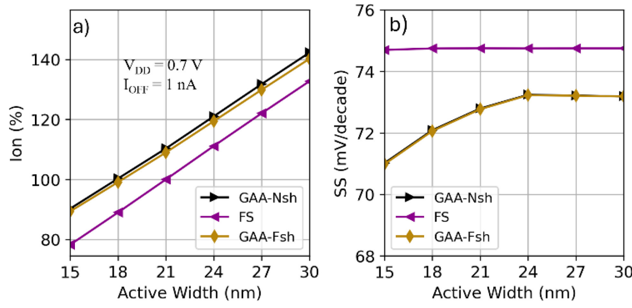

FIGURE 24. I_{ON} and SS evaluated for NFET for Mx = 24 nm case. Due to its tri-gate structure, Fsh shows 6-11% ON current drop and 2-4 mV/dec SS degradation & versus Nsh. GAA-Fsh shows full recovery.

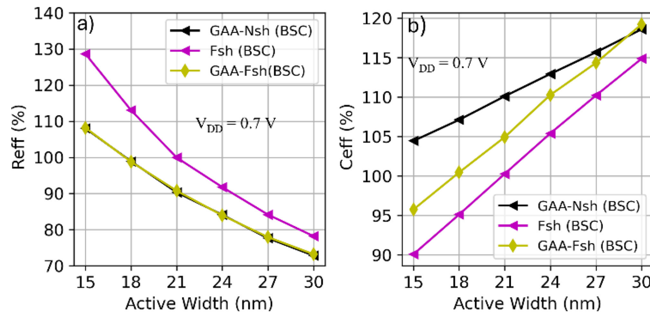

FIGURE 25. a) R_{eff} and b) C_{eff} extracted at Mx = 24 nm for W_{sh} ranging from 15-30 nm for Nsh and Fsh.

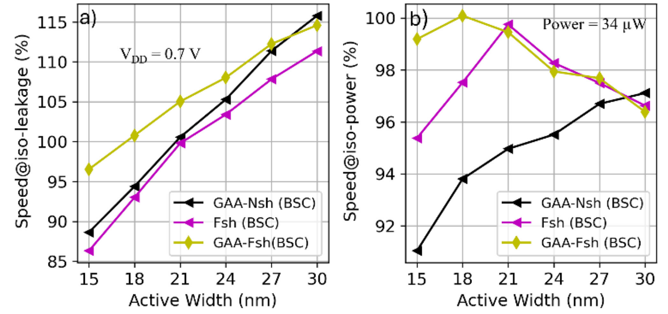

FIGURE 26. a) Speed@iso-leakage and b) Speed@iso-power extracted for Mx = 24 nm at W_{sh} ranging 15-30 nm. Data normalized to 21 nm Fsh with BPR @ V_{DD} 0.7V.

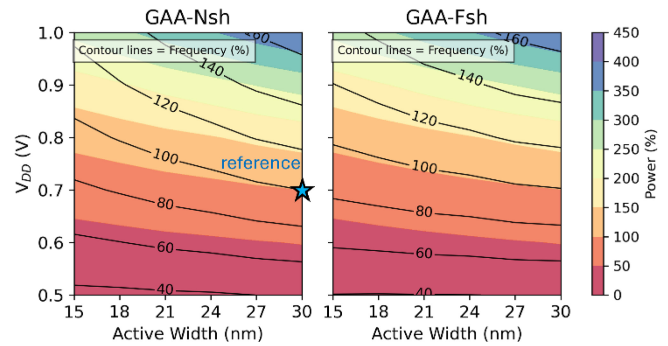

FIGURE 27. INVD1 speed and power for 3-sheet GAA-Nsh and GAA-Fsh for various W_{sh} and V_{DD} (for Mx = 24 nm). The reference is GAA-Nsh with W_{sh} = 30 nm at 0.7V.

Figure 24 presents the sub-threshold swing (SS) and on-current (I_{ON}) characteristics for GAA-Nsh, Fsh, and GAA-Fsh NFET devices. As anticipated, transitioning from GAA-Nsh to Fsh results in SS deterioration due to its non-full GAA design, which also causes ∼10% reduction in I_{ON} at small W_{sh}. However, this degradation is mitigated in the GAA-Fsh design.

The R_{eff} and C_{eff} evaluated for the 5-stage ring-oscillator at V_{DD} = 0.7 V for various W_{sh} are shown in Fig. 25. At smaller W_{sh}, an increase in R_{eff} (∼20%) for Fsh compared to GAA-Nsh is observed (Fig. 25a), attributed to SS and I_{ON} degradation in Fsh. However, at larger W_{sh}, the gap decreases to ∼7% due to SS degradation observed in GAA-Nsh as well. The deterioration of gate-control in Fsh can be mitigated by using GAA-Fsh, where R_{eff} for GAA-Fsh can reach low values of GAA-Nsh. Conversely, Fsh exhibits lower C_{eff} compared to GAA-Nsh, especially at smaller W_{sh} (∼15% lower) because the W_G depends on W_{sh} for Fsh but is fixed for GAA-Nsh (Fig. 9). This gap reduces to ∼3% at larger W_{sh} due to increased parasitic capacitance in Fsh resulting from the wider gate. For GAA-Fsh, which follows the same design rules as Fsh, C_{eff} is lower than GAA-Nsh at smaller W_{sh} (with a gap of ∼10%) but approaches the level of GAA-Nsh at larger W_{sh}. However, C_{eff} is higher in GAA-Fsh compared to Fsh due to additional parasitic gate capacitance from the etched metal filling at the etched wall.

Figure 26 displays the frequency (speed) evaluated under conditions of equal leakage (I_{OFF} = 1 nA and V_{DD} = 0.7 V) and equal power (34 μW at 0.7 V for the reference device) based on ring oscillator (RO) simulations. Under iso-leakage conditions, GAA-Fsh demonstrates superior performance compared to GAA-Nsh and Fsh at smaller W_{sh} values. As W_{sh} increases, GAA-Nsh begins to outperform GAA-Fsh due to its reduced gate parasitic capacitance. At smaller W_{sh} values, GAA-Nsh performs slightly better than Fsh, with the performance gap widening at larger W_{sh} values. Under iso-power conditions, the maximum speed is achieved at a W_{sh} of 18 nm for GAA-Fsh and 21 nm for Fsh, where Fsh attains performance levels comparable to GAA-Fsh but at a larger W_{sh}. In contrast, in GAA-Nsh, speed increases with W_{sh}, peaking at 30 nm. However, the peak performance of GAA-Nsh is ∼ 3% lower than that of Fsh, which is attributed to the capacitance contribution from the N-P separation.

Similar to Figure 15, which compared GAA-Nsh and Fsh, Fig. 27 compares the power and frequency performance of GAA-Nsh and GAA-Fsh across both W_{sh} and V_{DD}. In this plot, all the values are normalized to GAA-Nsh device of W_{sh} = 30 nm and V_{DD} = 0.7 V.

For low active widths (15 nm), GAA-Fsh achieves 3-10% higher frequency than GAA-Nsh at a similar power consumption; for V_{DD} ranging from 0.5 to 1 V. GAA-Fsh's performance benefit (w.r.t. GAA-Nsh) shrinks as active width W_{sh} approaches 30 nm. This is due to Nsh and Fsh specific layouts (Fig 6), where Fsh has a shorter W_G than Nsh for small W_{sh}, resulting in lower parasitic $C_{G\text{-}S/D}$. As W_{sh}

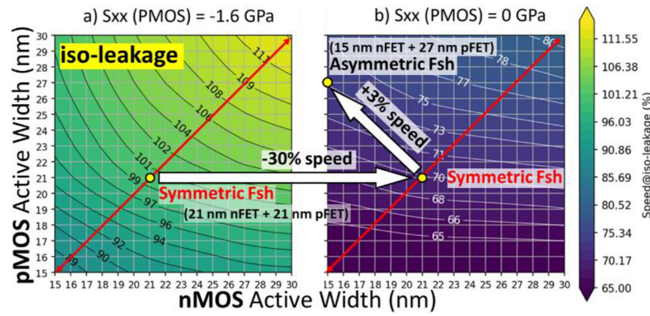

FIGURE 28. 2D contour plot of speed@iso-leakage for Fsh at 24 nm Mx calculated for various N-and P-FET W_{sh} combinations evaluated at a) -1.6 GPa and b) 0 GPa stress on pFET.

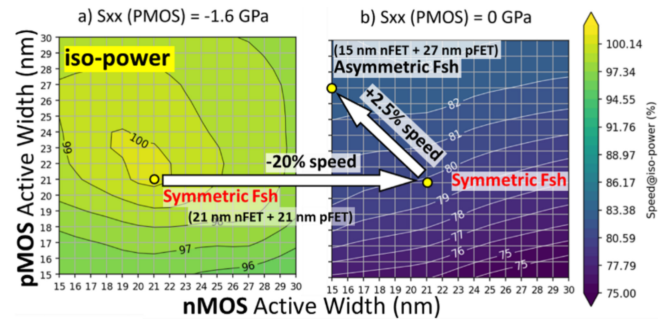

FIGURE 29. 2D contour plot of speed@iso-power for Fsh at 24 nm Mx calculated for various N-and P-FET W_{sh} combinations evaluated at a) -1.6 GPa and b) 0 GPa stress on pFET.

increases towards 30 nm, GAA-Fsh's benefit over GAA-Nsh disappears.

Across all V_{DD} and W_{sh} values, both devices show almost identical power curves. Due to the GAA nature of both devices, their intrinsic device characteristics are almost identical (see Fig 24). In RO context, this leads to an almost identical R_{eff} (Fig 25a) and hence similar power consumption (V_{dd}^2/R_{eff}). GAA-Fsh's benefit comes from its lower C_{eff} (esp at small W_{sh}) (Fig 25b). The corresponding frequency benefit is apparent in Fig 27. At V_{DD} around 0.75 V, 22 nm wide GAA-Fsh can achieve the same performance (100%) as 24 nm wide GAA-Nsh. At VDD = 0.9 V, 15 nm wide GAA-Fsh can achieve the same performance (120%) as 18 nm wide GAA-Nsh.

Overall, at V_{DD} = 0.7 V, GAA-Fsh has 7% higher frequency than GAA-Nsh for small W_{sh} (15 nm). This benefit disappears as W_{sh} approaches its maximum (30 nm). In order to achieve the same frequency as GAA-Nsh, GAA-Fsh's active width can be 2-3 nm shorter.

J. ASYMMETRIC N/P WSH FOR FSH AT MX = 24 NM

In the preceding sections, only ideal cases were considered, where both NFETs and PFETs are highly stressed. However, achieving stressed Nsh/Fsh has been recognized as a significant challenge due to the presence of inner spacers, which can degrade the balance of NFET and PFET devices, if PFET stress cannot be maintained [18]. Therefore, in this section, the performance impact of stress loss on PFETs is examined, along with the impact of asymmetry (larger PFET W_{sh} compared to NFET) to recover lost performance.

Figures 28 and 29 present the speed evaluated under iso-leakage and iso-power conditions for different combinations of NFET and PFET W_{sh} and PFET stress levels. It is observed that for both stress scenarios, there is a range of W_{sh} values that provide similar performance. While this is beneficial from a variability perspective, it does not result in substantial improvements with small W_{sh} adjustments.

However, in the case of Fsh, it is feasible to have a large skew in W_{sh}, for instance, by displacing the wall from the N/P center. This is depicted in Figures 28 and 29, where a wide range of NFET and PFET W_{sh} values is evaluated. In Figures 28b and 29b, it is observed that a full stress loss in PFETs reduces the performance by approximately 30% under iso-leakage conditions and 20% under iso-power conditions for the symmetric case. However, a partial recovery of around 3% of the lost performance is achieved by having asymmetric N-P W_{sh} while maintaining the cell footprint.

This analysis highlights the critical impact of stress on PFET performance and suggests that asymmetry in W_{sh} can be a second order strategy to mitigate performance degradation in stressed Nsh/Fsh architectures.

V. CONCLUSION

This study presents a comprehensive TCAD and DTCO comparison of Gate-All-Around Nanosheet (GAA-Nsh) and Forksheet (Fsh) architectures, focusing on their performance across key parameters such as active width (W_{sh}), sheet count (N), wall thickness, and permittivity. GAA-Nsh demonstrates a clear advantage at smaller W_{sh} due to its superior gate control, which results in better subthreshold swing (SS) and on-current (I_{ON}). However, as W_{sh} increases, Fsh shows stronger improvement in I_{ON}, closing the performance gap at larger dimensions, particularly at widths up to 24 nm, compared to 19 nm for GAA-Nsh. While Fsh demonstrates greater energy efficiency than GAA-Nsh at higher V_{DD} and narrower widths, achieving comparable speed with reduced power consumption and smaller active width overhead. However, at best, Fsh speed can only match GAA-Nsh at larger widths, due to limited gate control.

The largest improvement in I_{ON} is observed between N = 2 and N = 3, after which the gains diminish at higher sheet counts. In terms of speed, GAA-Nsh outperforms Fsh at smaller W_{sh} due to better gate control, while Fsh benefits from being able to scale to larger W_{sh}, making it more competitive as W_{sh} increases. A 3-sheet configuration is identified as the optimal trade-off between performance and power efficiency. Additionally, the choice of contacting scheme, whether BPR or BSPR with BSC, shows negligible impact on RO performance.

Further analysis into wall thickness and permittivity indicates that thinner walls and lower permittivity values provide better performance for Fsh devices, while thicker walls and higher-k materials lead to degraded SS and lower speed. Additionally, the study explores the effect of contact resistivity in Buried Power Rail (BPR) and Backside Power Rail (BS-PR) schemes, highlighting the critical role of minimizing contact resistance to optimize circuit performance.

To address Fsh's limitations, a novel GAA-Fsh architecture is introduced. This hybrid design combines the scalability benefits of Fsh with the superior gate control of GAA. However, this structure is only feasible at larger metal pitches (Mx). GAA-Fsh demonstrates significant performance improvements over both GAA-Nsh and Fsh, where the combination of Fsh's design rules and GAA's full gate coverage provides an advantage. Additionally, the study examines an asymmetric Fsh configuration, in which the wall is shifted to allow for different active widths for NMOS and PMOS devices. This asymmetry partially mitigates the performance loss in stressed devices, offering a practical approach to enhance Forksheet performance without sacrificing the advantages of its design.

In summary, GAA-Nsh remains the preferred option for smaller W_{sh} due to its stronger gate control and power efficiency, while Fsh's scalability makes it a competitive option at larger W_{sh}. The GAA-Fsh structure presents a promising hybrid solution, though its implementation requires larger metal pitches to fully leverage its benefits. The introduction of asymmetry in Fsh further improves its performance, making it a viable architecture for future technology nodes.

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