electronics

MDPI

Article

Column-Parallel Adaptive-Gain Single-Slope ADC Using a Single Global Ramp and Column-Local Capacitive Attenuation for High-Speed HDR Imaging

Hyunyoung Yoo [1,2], Chanhyuk Park [1,3], Minhyun Jin [1,4] and Myonglae Chu [1,*]

[1] Interuniversity Microelectronics Centre (IMEC), Kapeldreef 75, 3001 Leuven, Belgium; hyunyoung.yoo.ext@imec.be (H.Y.); chan-hyuk.park.ext@imec.be (C.P.); minhyun.jin@imec.be (M.J.)
[2] Department of Electronic Engineering, Seoul National University of Science and Technology, 232 Gongneung-ro, Seoul 01811, Republic of Korea
[3] Department of AI Semiconductor Engineering, Korea University Sejong Campus, 2511 Sejong-ro, Sejong-si 30019, Republic of Korea
[4] Department of Semiconductor Engineering, Pohang University of Science and Technology (POSTECH), Pohang 37673, Republic of Korea
* Correspondence: myonglae.chu@imec.be

Abstract

This paper presents a column-parallel adaptive-gain single-slope (SS) analog-to-digital converter (ADC) for high-speed high-dynamic-range (HDR) CMOS image sensors. Conventional adaptive-gain approaches often rely on dual-ramp generation or duplicated column circuits, which increase area and power overhead. In contrast, the proposed architecture achieves adaptive-gain operation using a single global ramp shared across all columns. A reconfigurable capacitive attenuation network embedded inside each column comparator locally scales the ramp at the comparator input, enabling seamless transition between high-gain operation for low-level signals and unity-gain operation for large signals within a single exposure and readout cycle. To suppress mode-dependent offsets while maintaining low noise, a configurable dual-source-follower ramp buffer symmetrically buffers the ramp and reference voltages during auto-zeroing and is reconfigured as a full-sized buffer during unity-gain conversion. Switching-induced column offsets are compensated using optical black pixels and lightweight digital processing. The ADC is implemented in a 110 nm CMOS image sensor process and validated through post-layout simulations including extracted parasitics and Monte Carlo mismatch analysis. The core ADC consumes 36.8 µW per column. Simulation results demonstrate linearity error below 1% without missing codes and show that the proposed AG_{x8}-to-AG_{x1} configuration extends the effective dynamic range up to 78.3 dB.

Keywords: CMOS image sensor; single-slope ADC; adaptive gain; HDR; single global ramp; capacitive attenuation; column-parallel ADC

Academic Editors: Massimo Piotto and Francesco Gagliardi

Received: 23 March 2026
Revised: 20 May 2026
Accepted: 21 May 2026
Published: 23 May 2026

1. Introduction

With the growing demand for applications such as surveillance and industrial inspection, image sensor systems are increasingly required to capture scenes that contain both very dark and bright regions within a single frame. Numerous techniques have been proposed to extend the dynamic range (DR) to address this requirement. Prior studies [1–5] have shown that DR can be enhanced by improving low-signal performance through multi-sampling or by combining multiple frames captured with different exposure times for high

dynamic range (HDR) reconstruction. However, these multi-frame approaches inevitably reduce the effective frame rate and introduce distortions when imaging fast-moving objects.

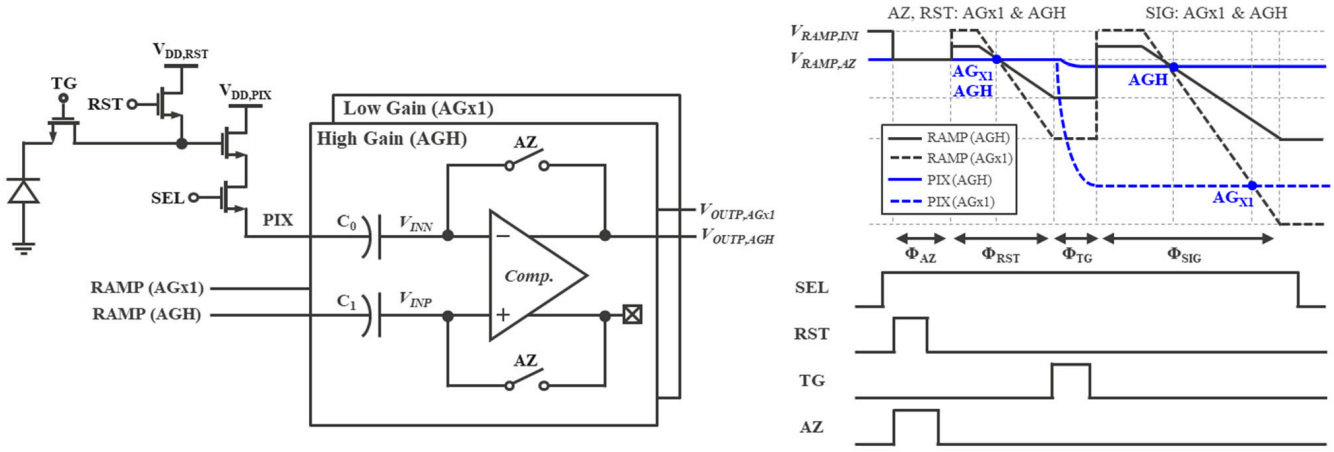
To avoid such motion artifacts, single-exposure HDR techniques are generally preferred. Among these, pixel-level DR extension methods such as dual conversion gain (DCG), lateral overflow integration capacitor (LOFIC), and split-photodiode (Split-PD) structures have been widely investigated. DCG pixels [6,7] extend DR by switching between a low conversion gain mode for bright signals and a high conversion gain mode for dark signals. Although effective, this technique requires additional in-pixel components, such as a capacitor and a gain-switching transistor, increasing pixel complexity and area overhead. LOFIC structures [8,9] extend DR by redirecting excess charge into an auxiliary capacitive node when the main photodiode approaches saturation. Reliable operation requires precise control of the overflow transistor's off-voltage and the internal potential profile, resulting in substantial design complexity. Split-PD structures [10,11] improve DR by dividing the pixel area into two photodiodes with varied sizes or sensitivities and combining their outputs. However, implementing two photodiodes with distinct ratios in a limited pixel area demands advanced process control and typically complicates fabrication. Overall, these HDR pixel techniques require additional pixel-level components or specialized processing steps beyond those of a conventional 4-T pixel. Implementing such structures within the same pixel area often necessitates stringent process control, increasing manufacturing cost and complexity. Alternatively, enlarging the pixel area to accommodate these features reduces spatial resolution for a given sensor size. As a result, these approaches are not well suited for high-speed imaging and are generally unsuitable for mid-range image sensors targeting approximately 70 dB DR, where low cost and high manufacturability are critical.

To address the limitations of HDR pixels, several studies have explored column-level DR extension in the readout circuitry. Prior work [12] employed programmable-gain amplifiers (PGAs) in the column readout path, where the gain is adaptively adjusted based on the pixel signal level. While this method enables DR extension, it requires a dedicated PGA per column, resulting in significant area overhead and increased power consumption. To reduce this overhead, another study [13] reused the auto-zero (AZ) capacitor of a single-slope (SS) analog-to-digital converter (ADC) as a capacitive gain stage. Although eliminating the extra PGA, this technique still requires an additional active sample-and-hold circuit to separately capture the reset level, increasing circuit complexity and limiting scalability. A different approach [14] implemented column-level adaptive-gain by providing two ramp signals with different slopes and selecting the appropriate ramp based on the pixel signal range. This method avoids modifications to the pixel signal path but requires a ramp generator capable of producing two different ramp slopes to drive the entire column array, which introduces substantial loading and routing challenges and degrades ramp linearity and uniformity.

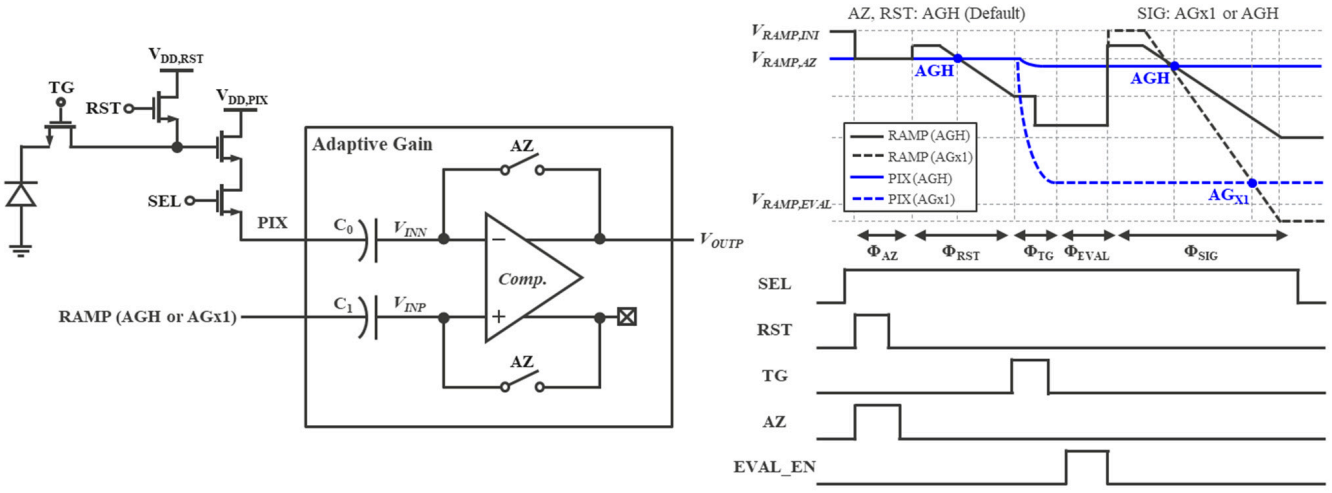
This work proposes a column-level adaptive-gain readout technique with minimal additional circuit overhead. The proposed method operates using only a single ramp slope generated by a conventional ramp generator and leverages the intrinsic structure of a standard single-slope ADC to achieve gain adaptation without modifying either the pixel array or the ADC architecture. In the following sections, the proposed circuit architecture, circuit implementation and analysis, error-correction techniques, results and validation, and concluding remarks are presented in detail.

2. Principle of Adaptive-Gain Operation

Figure 1 illustrates the timing comparison between a conventional dual-gain HDR image sensor based on single-slope (SS) ADC operation and the adaptive-gain HDR image sensor. In the conventional dual-gain readout scheme shown in Figure 1a, two column readout ADCs are assigned to a single pixel to simultaneously process the pixel signal using ramp signals with different gains. During the auto-zero phase (Φ_{AZ}), both ADCs sample the pixel reset level. Subsequently, during the reset conversion phase (Φ_{RST}), analog-to-digital conversion is performed using two ramps with different slopes. After charge transfer from the photodiode to the floating diffusion during the transfer gate phase (Φ_{TG}), the signal conversion phase (Φ_{SIG}) is carried out again using the two distinct ramp signals. In this conventional structure, dual-gain readout is achieved at the cost of increased column readout resources. Compared with the standard configuration that employs one ADC per column, the dual-gain approach requires twice the number of column ADCs to maintain the same frame rate.



(**a**)



(**b**)

Figure 1. Timing comparison with conventional adaptive-gain HDR image sensors. (**a**) Readout using two column ADCs, (**b**) adaptive readout using two ramp signals (AGH: High analog gain mode, AG_{x1}: Low analog gain mode, Φ_{AZ}: Auto-zero, Φ_{RST}: Reset conversion, Φ_{TG}: Charge transfer, Φ_{EVAL}: Evaluation, Φ_{SIG}: Signal conversion).

To overcome these limitations, the adaptive-gain scheme of [14] is discussed in further detail, as shown in Figure 1b. In [14], an additional evaluation phase is inserted between the reset and signal conversions to assess the pixel signal level and select an appropriate ramp slope. By dynamically choosing the ramp based on the signal amplitude, dual-gain readout can be realized using a single ADC per column with only a minor readout timing overhead, while preserving the frame rate and maintaining one ADC per column. However, this adaptive-gain approach requires the ramp generator to simultaneously provide two ramp signals with different slopes to the entire column array. Since the ramp signal occupies a significant portion of the row readout time and must drive all columns concurrently, its linearity and settling characteristics are critical. Generating and distributing two distinct ramp slopes across the full array therefore demands careful system-level optimization and incurs additional power consumption. Instead, this work proposes an adaptive-gain operation that employs only a single global ramp signal while adjusting the effective ramp gain locally at the column level. By eliminating the need for multiple global ramp slopes, the proposed scheme simplifies the ramp generation and distribution network, reduces power consumption, and enables efficient adaptive-gain HDR readout without sacrificing frame rate. Unlike PGA-based approaches that rely on active gain stages introducing additional power consumption and noise, the proposed architecture achieves gain adaptation through passive attenuation at the comparator input, by splitting the auto-zero (AZ) capacitors, requiring no additional active circuits or bias current.

Figure 2 shows the block diagram of a conventional image sensor employing column-parallel ADCs, together with the detailed architecture of the proposed adaptive-gain ADC. A typical image sensor readout system consists of a pixel array, row drivers, a timing generator, and column-parallel analog-to-digital converters (ADCs). The proposed adaptive-gain ADC is built upon a standard single-slope (SS) ADC architecture composed of a comparator, a ramp generator, and counters. To enable adaptive-gain operation, only a compact adaptive-gain (AG) digital logic block is added to the conventional 10-bit SS ADC. The AG logic occupies approximately 420 μm^2, which is a minute fraction of the total column comparator area (3000 μm^2). In addition, minor modifications are introduced in the comparator input capacitive network and the column ramp buffer to support reconfigurable ramp gain control, with the additional switches in the capacitive network requiring only about 210 μm^2. As the overall ADC structure and pixel array remain unchanged, these AG-related components represent a low-overhead integration that remains well within the standard column pitch. The comparator employs a structure similar to those in [15,16], incorporating correlated double sampling (CDS) through auto-zeroing (AZ). After the pixel reset level is converted, the comparator evaluates the pixel signal level during the evaluation phase, and the AG logic determines the appropriate ramp gain for the subsequent signal conversion. Instead of generating multiple global ramp slopes, the proposed scheme adaptively adjusts the effective ramp gain at the column level by reconfiguring the capacitive network at the comparator input. The ramp buffer is configured to support this gain reconfiguration while maintaining proper ramp driving capability. Importantly, the global ramp generator itself remains unchanged and can be implemented using a conventional current-steering DAC-based ramp generator widely adopted in SS ADCs. The counter employs a hybrid structure in which a global Gray-code counter is shared across multiple column groups, while column-level latches locally capture the conversion results to form the final digital output. The detailed circuit implementation and operating principle of the adaptive-gain mechanism are described in Section 3.

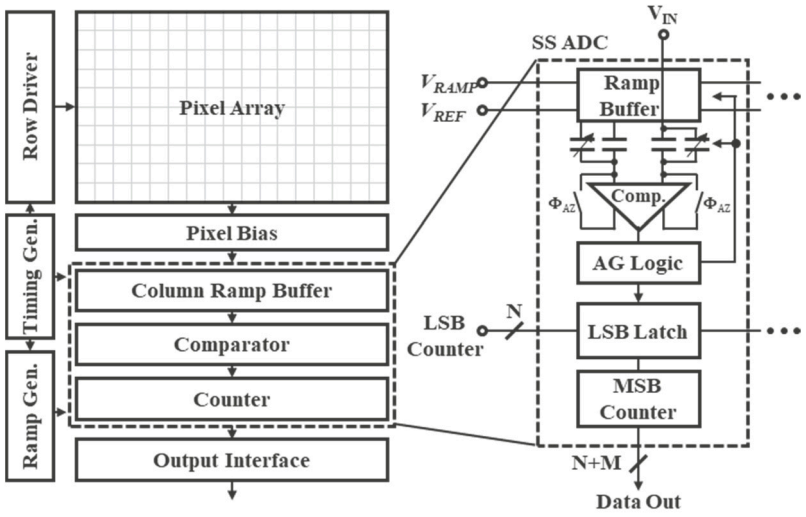


Figure 2. Architecture of the proposed adaptive-gain ADC.

3. Circuit Implementation

3.1. Passive Ramp Gain Adaptive Comparator

Figure 3 illustrates the operating sequence of the proposed column-level adaptive-gain comparator. To minimize power supply fluctuations during comparator toggling, the architecture adopts the constant-current comparator design described in [17]. This design ensures a steady current flow from VDD to GND regardless of the comparator's decision state. By suppressing transient supply noise and ground bounce typically triggered by simultaneous toggling, this approach effectively reduces crosstalk and fixed pattern noise (FPN), ensuring high image quality during high-speed readout. The pixel signal is coupled through capacitor C_0, while the ramp signal is applied through a reconfigurable capacitive network composed of C_1 and C_2. The comparator operates through five sequential phases: auto-zero (Φ_{AZ}), reset conversion (Φ_{RST}), charge transfer (Φ_{TG}), evaluation (Φ_{EVAL}), and signal conversion (Φ_{SIG}). The evaluation phase determines the appropriate gain mode prior to signal conversion.

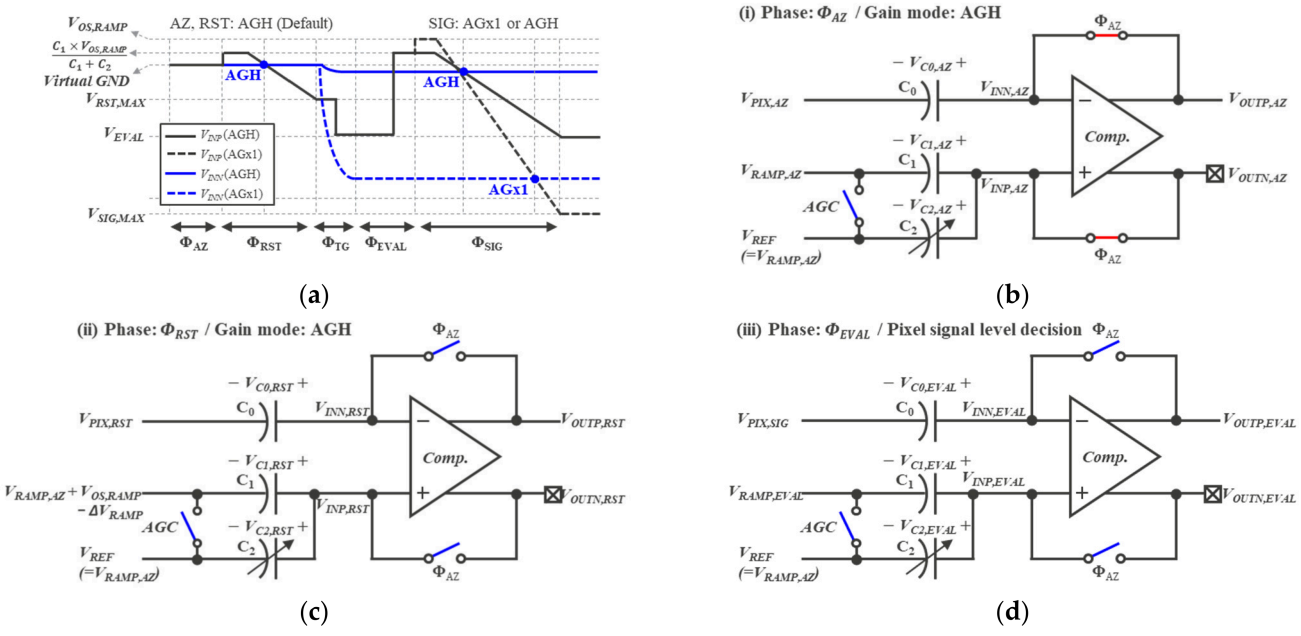


Figure 3. *Cont.*

https://doi.org/10.3390/electronics15112266

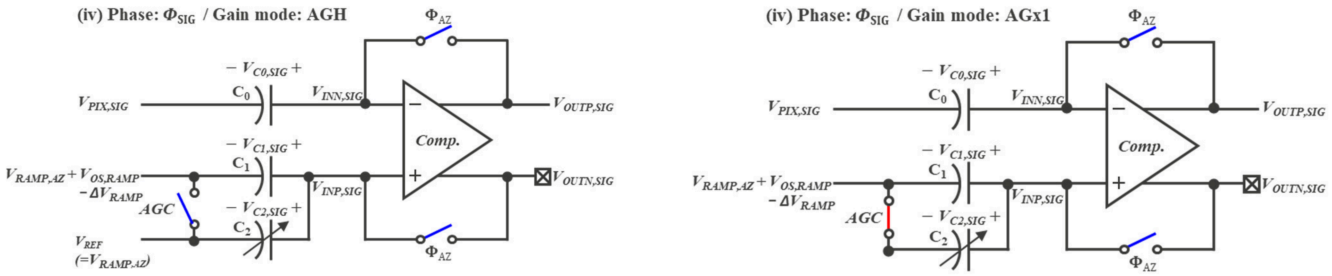


Figure 3. Adaptive-gain operation of the column comparator: (**a**) one-row readout timing, (**b**) auto-zero (AZ) phase, (**c**) reset (RST) phase in the AGH mode, (**d**) evaluation phase, (**e**) signal (SIG) phase in the AGH mode, and (**f**) signal (SIG) phase in the AG_{x1} mode.

During the auto-zero phase Φ_{AZ}, the comparator input nodes V_{INP} and V_{INN} are shorted by the AZ switches, and the intrinsic offset of the comparator is sampled across the capacitors. As a result, both input nodes are set to the same offset level, such that

$$V_{INP,AZ} = V_{INN,AZ} = V_{OS,AZ} \quad (1)$$

At the same time, the ramp signal is initialized to a reference level $V_{RAMP,AZ}$. The charges stored on the ramp-side capacitors are given by

$$Q_{C1,AZ} = C_1(V_{OS,AZ} - V_{RAMP,AZ}) \quad (2)$$

$$Q_{C2,AZ} = C_2(V_{OS,AZ} - V_{REF}) = C_2(V_{OS,AZ} - V_{RAMP,AZ}) \quad (3)$$

where V_{REF} is set equal to $V_{RAMP,AZ}$ to avoid the offset variation introduced by capacitor reconfiguration during ramp gain switching at the end of Φ_{EVAL}. Once Φ_{AZ} is completed, the AZ switches are opened, and the stored charges on the capacitors are preserved throughout the subsequent phases. During the reset conversion phase Φ_{RST}, the pixel floating diffusion (FD) node reset level is converted. To improve noise performance, the A/D conversion of the reset level is always performed in the high analog gain (AGH) mode. This configuration suppresses comparator-referred noise during reset conversion, thereby extending the effective dynamic range toward the dark region. The AGH capacitive network configuration is shown in Figure 3b, which remains identical to that used at the end of Φ_{AZ}. The stored charges are updated as

$$Q_{C1,RST} = C_1(V_{OS,AZ} + V_{OS,RST} - V_{RAMP,AZ}) \quad (4)$$

$$Q_{C2,RST} = C_2(V_{OS,AZ} + V_{OS,RST} - V_{RAMP,AZ}) \quad (5)$$

where $V_{OS,RST}$ represents the additional offset introduced by AZ switch charge injection and clock feedthrough during the reset phase. For simplicity, the timing waveforms shown in Figure 3a are illustrated without offset voltage components. During the auto-zero (AZ) operation, V_{INP} and V_{INN} are initialized to the same reference voltage, and subsequent pixel and ramp signals are coupled as relative voltage changes with respect to this common level. Accordingly, V_{INP} and V_{INN} are set to virtual ground at the beginning of Φ_{RST}, and only their subsequent voltage variations are shown. Using charge conservation, the effective comparator input voltages during Φ_{RST} can be derived. As shown in Figure 3c, they are expressed as

$$V_{INP,RST} = V_{OS,AZ} + V_{OS,RST} + \frac{C_1}{C_1 + C_2} \cdot (V_{OS,RAMP} - \Delta V_{RAMP}) \quad (6)$$

$$V_{INN,RST} = \mathrm{V}_{OS,AZ} + \mathrm{V}_{OS,RST} \tag{7}$$

where $V_{OS,RAMP}$ is the initial ramp offset to guarantee ramp linearity and cancel out the mismatch of $\mathrm{V}_{OS,RST}$ at V_{INP} and V_{INN}, and ΔV_{RAMP} represents the ramp signal. The factor $\frac{C_1}{C_1+C_2}$ effectively attenuates the ramp slope, thereby increasing the effective analog gain of the pixel signal as seen by the comparator. Note that the ramp slope is synchronized with the counter clock frequency to ensure precise conversion timing. To enhance the signal integrity of the global ramp, the proposed design utilizes a current-steering ramp generator [18], which maintains a constant current consumption from the power supply. Unlike conventional architectures that suffer from switching transients, this current-steering approach minimizes power supply fluctuations. This is particularly effective in mitigating the impact of parasitic inductances from the package and bondwires, thereby ensuring high ramp linearity even at high-speed operation.

When V_{INP} crosses V_{INN}, the comparator is triggered and latches the corresponding counter value, completing the reset-level A/D conversion. After the reset conversion, during the charge transfer phase Φ_{TG}, the light-integrated pixel signal $V_{PIX,SIG}$ is transferred to the floating diffusion and applied to the comparator input. The comparator then enters the evaluation phase Φ_{EVAL} to determine the appropriate ramp gain for the subsequent signal conversion. During Φ_{EVAL}, the circuit configuration remains identical to that of Φ_{RST}; however, the ramp signal is shifted to a predefined level, $V_{RAMP,EVAL}$, so that $V_{INP,EVAL}$ moves to the V_{EVAL} level, as shown in Figure 3d. If V_{INN} does not exceed V_{EVAL}, the capacitive network remains in the high analog gain (AGH) mode, as illustrated in Figure 3e. Otherwise, the comparator is reconfigured to the analog gain x1 ($\mathrm{AG_{x1}}$) mode, as shown in Figure 3f. In the $\mathrm{AG_{x1}}$ configuration, the ramp signal is applied to the comparator input without any attenuation, enabling a lower effective analog gain. Accordingly, the comparator input voltages during the signal conversion phase Φ_{SIG} are expressed as follows.

In the AGH mode,

$$V_{INP,SIG} = \mathrm{V}_{OS,AZ} + \mathrm{V}_{OS,RST} + \frac{C_1}{C_1+C_2} \cdot (V_{OS,RAMP} - \Delta V_{RAMP}) \tag{8}$$

$$V_{INN,SIG} = \mathrm{V}_{OS,AZ} + \mathrm{V}_{OS,RST} - \mathrm{V}_{PIX,SIG} \tag{9}$$

In the $\mathrm{AG_{x1}}$ mode,

$$\begin{aligned} V_{INP,SIG} &= \mathrm{V}_{OS,AZ} + \mathrm{V}_{OS,RST} + \tfrac{C_1}{C_1+C_2} \cdot V_{OS,RAMP} + \tfrac{C_2}{C_1+C_2} \cdot (V_{OS,RAMP} + V_{OS,AGx1}) \\ &\quad - \Delta V_{RAMP} \\ &= \mathrm{V}_{OS,AZ} + \mathrm{V}_{OS,RST} + \left(V_{OS,RAMP} + \tfrac{C_2}{C_1+C_2} \cdot V_{OS,AGx1} - \Delta V_{RAMP}\right) \end{aligned} \tag{10}$$

$$V_{INN,SIG} = \mathrm{V}_{OS,AZ} + \mathrm{V}_{OS,RST} - \mathrm{V}_{PIX,SIG} \tag{11}$$

During this brief evaluation window, if the pixel signal V_{INN} lies extremely close to the decision threshold V_{EVAL}, the comparator may encounter metastability or noise-induced decision delays. To ensure robust operation, a digital redundancy margin is incorporated into the gain-switching boundary. By intentionally setting the decision threshold at a level that ensures the $V_{PIX,SIG}$ range in AGH mode partially overlaps with the $\mathrm{AG_{x1}}$ transition point, the system remains tolerant to marginal decision errors. Even if the comparator fails to toggle due to thermal noise during Φ_{EVAL} and defaults to the AGH mode, the signal can still be accurately digitized without saturation. This architectural redundancy eliminates the need for complex hysteresis circuits or digital filtering while maintaining decision reliability. In the $\mathrm{AG_{x1}}$ mode, an inherent offset component, $V_{\mathrm{OS,AGx1}}$, exists at V_{INP} due to the switching operation of the ramp-side capacitive network. When the reset code obtained in the AGH mode is combined with the signal code converted in the $\mathrm{AG_{x1}}$ mode to form a full-scale digital code through correlated double sampling (CDS), this offset introduces a discontinuity at the transition point between the two gain modes. If the offset is uncompensated, the resulting offset step can lead

to missing codes and non-monotonic behavior in the reconstructed full code. Moreover, capacitor mismatch between C_1 and C_2 can introduce AGH-AG_{x1} gain mismatch over column readout circuits, which can result in different offset values even after offset compensation.

To account for column-to-column variations arising from capacitor mismatch and offset voltage non-uniformities, an additional digital correction is required. The proposed digital compensation scheme, which suppresses the column-wise offset mismatch, is described in detail in Section 3.3. By combining high-gain readout for low-level signals with $\times 1$ gain conversion for large signals and applying simple digital compensation, the proposed scheme enables efficient single-exposure HDR readout with minimal area and power overhead.

3.2. Dual-Source Followers for Noise Optimization of the Column Ramp Buffer

The proposed adaptive-gain ADC employs configurable dual-source-follower (SF) structures as column-level ramp buffers to minimize offset between the ramp and reference signals during the auto-zero (AZ) phase while optimizing noise performance across different gain modes. As described in the previous section, the adaptive-gain operation adjusts the effective ramp gain by reconfiguring a capacitive attenuation network at the comparator input. While this passive-domain gain control eliminates the need for additional active amplifiers, it introduces offset variations associated with changes in the ramp-side capacitive configuration. To ensure consistent comparator operation across gain modes, it is therefore essential to align the reference voltage, V_{REF}, as closely as possible to the ramp voltage at the end of the AZ phase, $V_{RAMP,AZ}$. In conventional single-slope (SS) ADCs, the ramp signal is buffered by a source follower to isolate the ramp generator from comparator kick-back noise, which introduces a voltage shift to the gate-to-source voltage (V_{GS}). If the reference signal is not buffered in the same manner, a systematic mismatch arises between the buffered ramp and the unbuffered reference, directly translating into a comparator input offset. Although this mismatch can be mitigated by inserting an identical buffer in the reference path, such an approach doubles the number of ramp buffers, increasing column-level area and power consumption.

To avoid this overhead, a configurable dual-source-follower ramp buffer is proposed, as shown in Figure 4. The original ramp buffer is partitioned into two half-sized source followers, SF1 and SF2, each biased with half of the original current, such that their combined device size and total bias current remain identical to those of a conventional single ramp buffer. In the high analog gain (AGH) mode, shown in Figure 4a, SF1 and SF2 independently buffer the ramp and reference signals, respectively. This symmetric buffering ensures that both signals experience identical source-follower-induced voltage shifts, thereby minimizing offset during the AZ phase. In the AG_{x1} mode, shown in Figure 4b, the inputs and outputs of SF1 and SF2 are shorted, and the two devices operate as a single full-sized source follower to drive only the ramp signal, restoring the low-noise and high-speed buffering capability required for large-signal conversion.

The attenuation ratio in AGH mode and the configuration of the source followers are controlled by the adaptive-gain control (AGC) signal generated by the digital adaptive-gain logic, shown in Figure 5a. During the evaluation phase (Φ_{EVAL}), the comparator output (*CMP_OUT*) is sampled and latched when *EVAL_EN* is asserted, producing a stable gain decision. As illustrated in Figure 5b, the AGC signal is updated only within the evaluation window and remains constant throughout the subsequent signal conversion phase (Φ_{SIG}), ensuring that no dynamic reconfiguration occurs during A/D conversion. The digital logic simultaneously generates the control signals $CTRL\langle 1:0\rangle$, which configure the capacitive attenuation network to realize the desired attenuation ratio in AGH mode or to short all capacitors together in AG_{x1} mode.

From a noise perspective, the proposed reconfigurable ramp buffer provides a clear advantage over a fixed dual half-sized buffer implementation. Unlike higher-order digital CDS, which necessitates multiple reset and signal conversion cycles—thereby doubling the readout time—the proposed scheme maintains the standard single-CDS timing, preserving high-speed operation. Furthermore, compared to chopping techniques that require complex switching phases and additional column-level circuitry, the proposed dual--source-follower (SF) structure minimizes layout complexity by reconfiguring existing components. In AGH mode, capacitive attenuation suppresses the contribution of ramp buffer noise at the comparator input, and the reduced ramp slope limits the effective noise bandwidth, rendering the noise penalty of half-sized buffers negligible. In contrast, in AG_{x1} mode, the ramp signal is applied without attenuation and with a higher slope, making ramp buffer

noise more critical. By reconfiguring SF1 and SF2 into a single full-sized source follower in AG_{x1} mode, the proposed scheme avoids the noise degradation that would arise from permanently using half-sized buffers. As a result, the proposed design achieves both robust offset matching in AGH mode and low-noise ramp driving in AG_{x1} mode, enabling adaptive-gain readout with improved noise performance without increasing column area or power consumption.

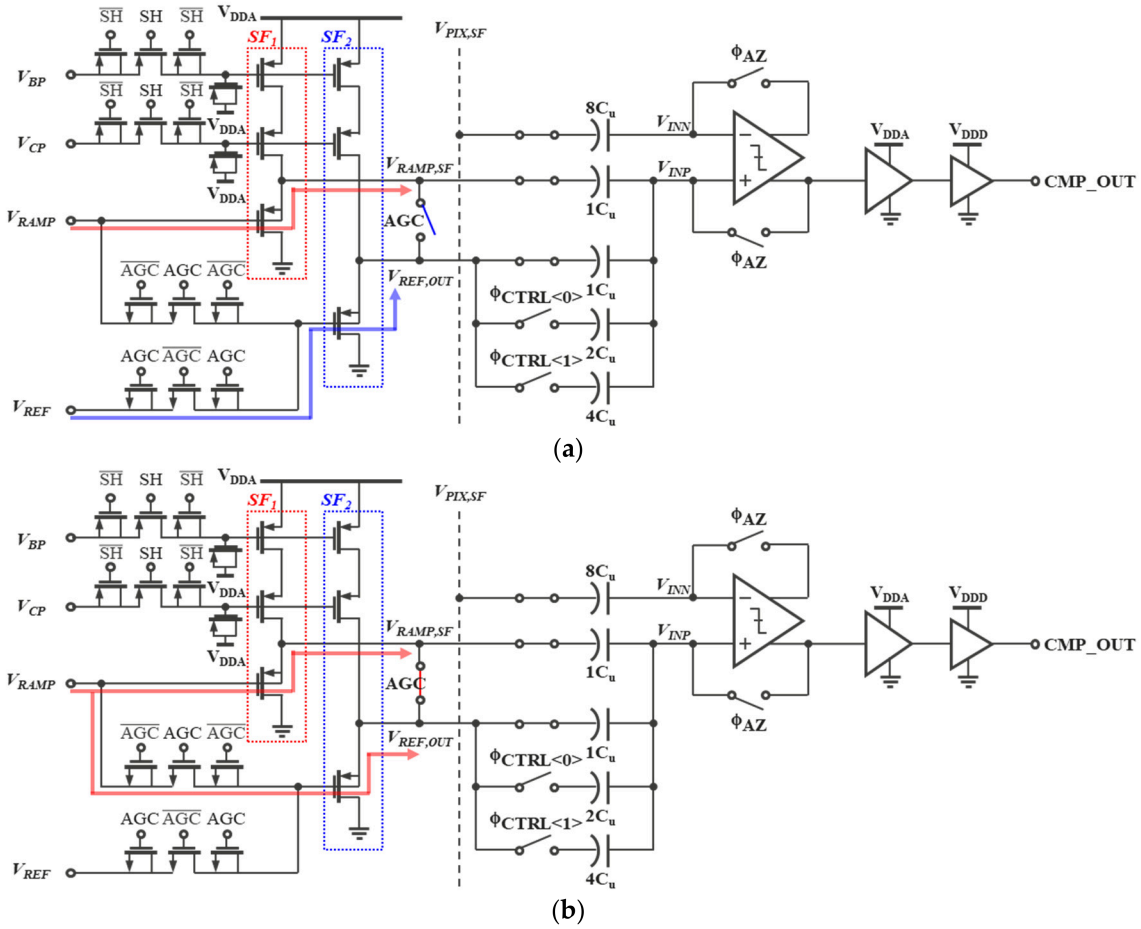


Figure 4. Column ramp buffers with three-stage comparator. (**a**) High analog gain (AGH) configuration, in which two half-sized source followers (SF1 and SF2) independently buffer the ramp and reference signals to minimize offset during the auto-zero phase. (**b**) Low analog gain (AG_{x1}) configuration, where SF1 and SF2 are shorted and operate as a single full-sized source follower to drive the ramp signal with reduced noise.

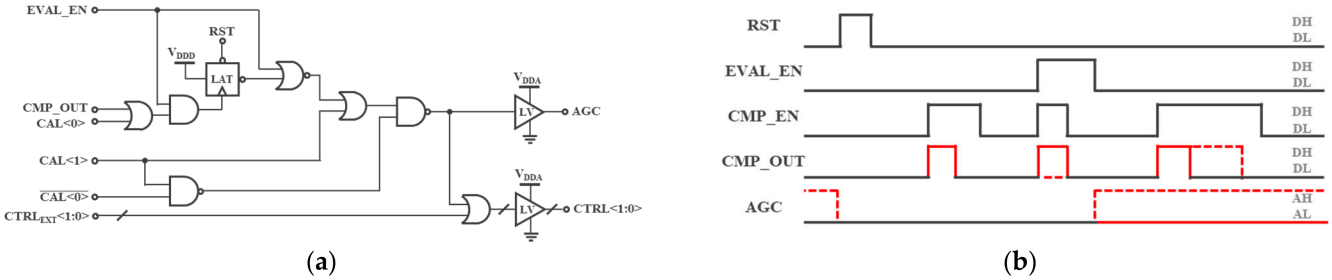


Figure 5. Adaptive-gain digital control logic. (**a**) Simplified schematic of the adaptive-gain decision logic generating the AGC and $CTRL\langle 1:0\rangle$ signals based on the comparator output during the evaluation phase. (**b**) Timing diagram illustrating the relationship between reset, evaluation, comparator enable, and AGC signals, showing that the gain decision is latched during Φ_{EVAL} and held constant throughout signal conversion.

3.3. Column-Level Offset and Gain Calibration Using Optical Black Pixels

Under dark input conditions, the offset behavior of the proposed gain-switching scheme can be analyzed using (8) and (10). Figure 6 illustrates the ramp-related offset behavior for the two readout modes. In the AGH-only mode, the same effective ramp gain is applied during both reset and signal conversions. Consequently, the ramp-related offset component is identical for the reset and signal phases, $D_{\mathrm{OS,ramp}} = D_{\mathrm{RST,AGH}} = D_{\mathrm{SIG,AGH}}$. As a result, correlated double sampling (CDS) naturally cancels the offset under dark conditions, yielding a zero output code:

$$D_{\mathrm{CDS,AGH}} = D_{\mathrm{SIG,AGH}} - D_{\mathrm{RST,AGH}} = 0 \tag{12}$$

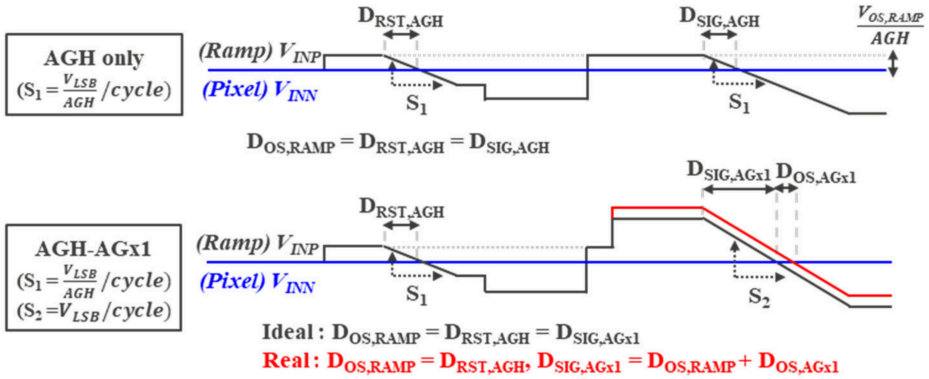


Figure 6. Ramp-related offset behavior in different readout modes. (**Top**) AGH-only operation, where identical ramp gain is applied during reset and signal conversions. (**Bottom**) AGH–AG$_{x1}$ operation, where the effective ramp gain changes between reset and signal conversions, potentially introducing an additional offset component during signal conversion.

In the AGH–AG$_{x1}$ mode, the capacitive attenuation applied to the ramp is removed prior to signal conversion. The ramp offset level therefore increases in proportion to the gain ratio used for pixel signal A/D conversion. Under ideal dark conditions, the effective ramp slope (i.e., the gain at the comparator input) increases by the same gain ratio. Both the ramp offset and slope scale identically. The ramp reaches the comparator threshold more rapidly, while the voltage swing is expanded by the same factor. Although the analog ramp level is shifted, the conversion step size is increased proportionally. The digital output code after A/D conversion thus remains identical to that obtained during reset conversion under dark conditions. The CDS output is therefore zero even in the AGH–AG$_{x1}$ mode:

$$D_{\mathrm{CDS,AGH\ -\ AGx1}} = D_{\mathrm{SIG,AGx1}} - D_{\mathrm{RST,AGH}} = 0 \tag{13}$$

In practice, however, capacitive switching during ramp-gain reconfiguration introduces an additional offset component for signal conversion. This switching-induced offset generates an extra digital code $D_{\mathrm{OS,AGx1}}$, as indicated by the red in Figure 6. Under this condition, the CDS result in the AGH–AG$_{x1}$ mode becomes

$$D_{\mathrm{CDS,AGH-AGx1}} = D_{\mathrm{SIG,AGx1}} - D_{\mathrm{RST,AGH}} = \left(D_{\mathrm{OS,ramp}} + D_{\mathrm{OS,AGx1}}\right) - D_{\mathrm{OS,ramp}} = D_{\mathrm{OS,AGx1}} \tag{14}$$

Thus, all AGH–AG$_{x1}$ data include an additional offset term originating from ramp-gain switching. The impact of this offset on full-code reconstruction is illustrated in Figure 7. As shown in Figure 7a, in the ideal case, when the pixel signal is smaller than ADC_{SAT}/AGH, where ADC_{SAT} denotes the full-scale input range of the ADC, the output is represented exclusively by AGH-only conversion, producing digital codes from 0 to $2^N - 1$. For larger signals, the AGH–AG$_{x1}$ readout is activated. The final full code is reconstructed by multiplying the AGH–AG$_{x1}$ CDS result by the AGH factor. As shown in Figure 7b, when no offset is present, the two response curves connect seamlessly, resulting in a continuous and monotonic transfer characteristic. In contrast, when the offset term $D_{\mathrm{OS,AGx1}}$ exists, the gain multiplication applied for full-code reconstruction also scales this offset, as illustrated in Figure 7c,d. Consequently, a discontinuity appears at the transition point between the AGH-only and AGH–AG$_{x1}$ regions. Since the switching-induced offset varies from

column to column due to capacitor mismatch, this discontinuity causes column-wise fixed-pattern noise (FPN). In severe cases, the combined effects of offset and gain mismatch lead to missing codes and non-monotonic behavior in the reconstructed full-code transfer characteristic.

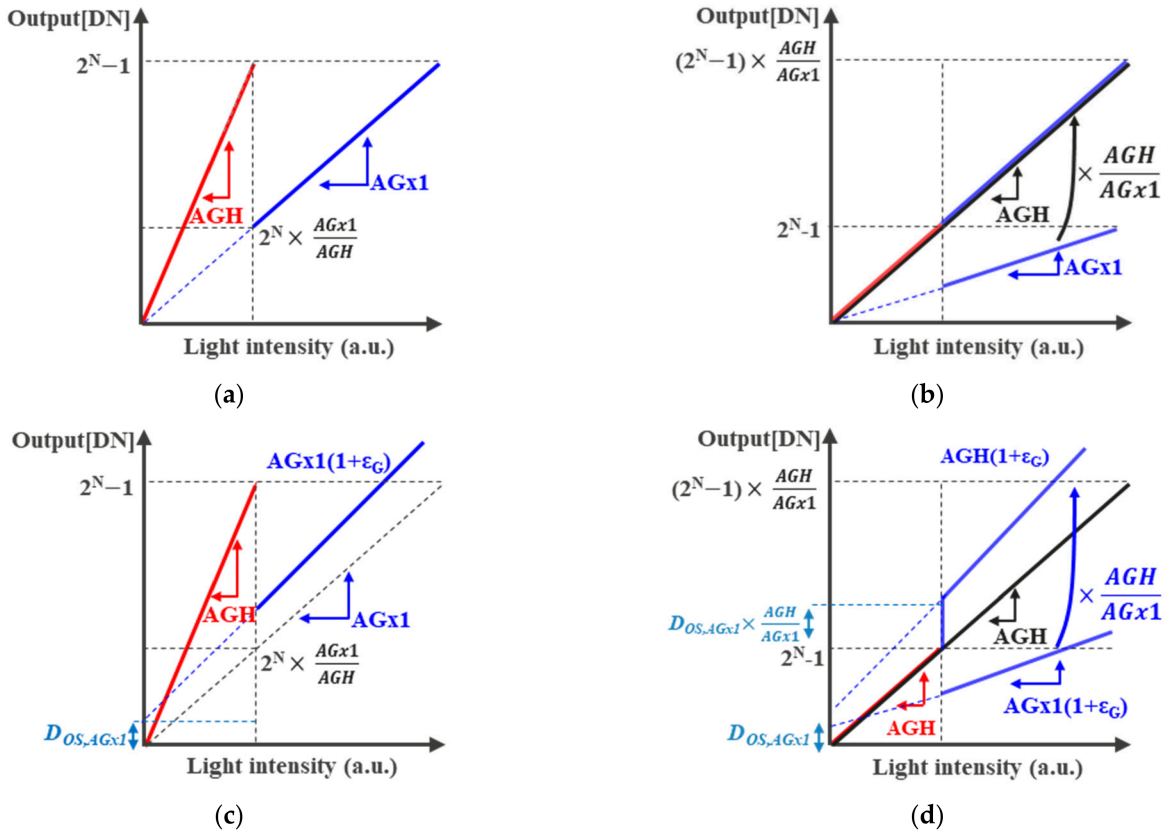


Figure 7. Impact of offset and gain mismatch on full code reconstruction: (**a**) Ideal AGH and AG_{x1} responses in the absence of offset and capacitor mismatch. (**b**) Full code reconstructed from the ideal AGH and AG_{x1} responses, showing a continuous and monotonic transfer characteristic. (**c**) Practical AGH and AG_{x1} responses including offset and gain mismatch. (**d**) Discontinuity and missing codes in the reconstructed full code caused by the combined effects of offset and gain mismatch between AGH and AG_{x1} modes.

To suppress this offset-induced discontinuity, optical black (OB) pixels are employed for column-wise offset sensing. As shown in Figure 8, OB pixel arrays are placed at the top and bottom of the active pixel region. A subset of these OB pixels is dedicated to measuring the AGH–AG_{x1} offset component. These pixels are intentionally read out in the AGH–AG_{x1} mode under dark conditions with minimum exposure time, such that their outputs contain only the switching-induced offset. The measured digital codes are stored in line memory as column-wise offset references $D_{OS,AGx1}$. The remaining OB pixels are used for conventional frame-adaptive dark-level correction (F-ADLC) to track temporal variations in dark current. The overall compensation procedure is summarized in Figure 9. OB pixels for column offset sensing are first read out and stored, followed by OB pixels for F-ADLC, and finally, the active pixels are read out row-by-row. During ISP processing, the final reconstructed full code is generated by applying a subtraction-based correction flow. Specifically, both the column-wise offset term and the frame-adaptive dark-level term are subtracted from the reconstructed full code of each active pixel, thereby removing offset-induced discontinuities while preserving temporal dark-current compensation.

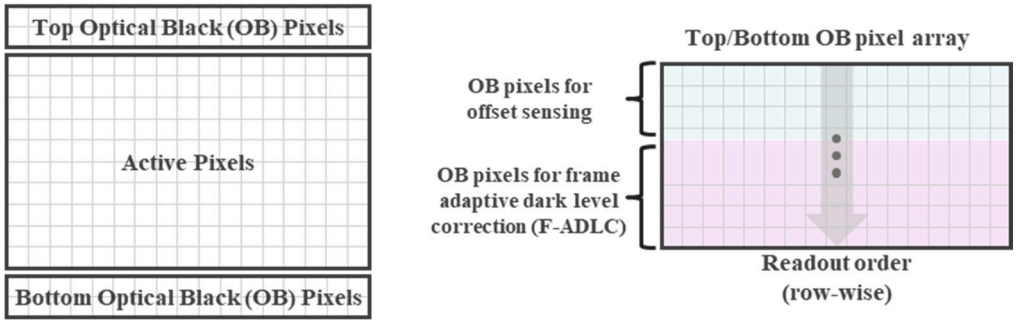


Figure 8. Organization of optical black (OB) pixels for column-wise offset sensing and frame-adaptive dark-level correction. Top and bottom OB pixel arrays are placed adjacent to the active pixel region. A subset of OB pixels is used for column-wise offset sensing, while the remaining OB pixels are utilized for frame-adaptive dark-level correction (F-ADLC) following the row-wise readout order.

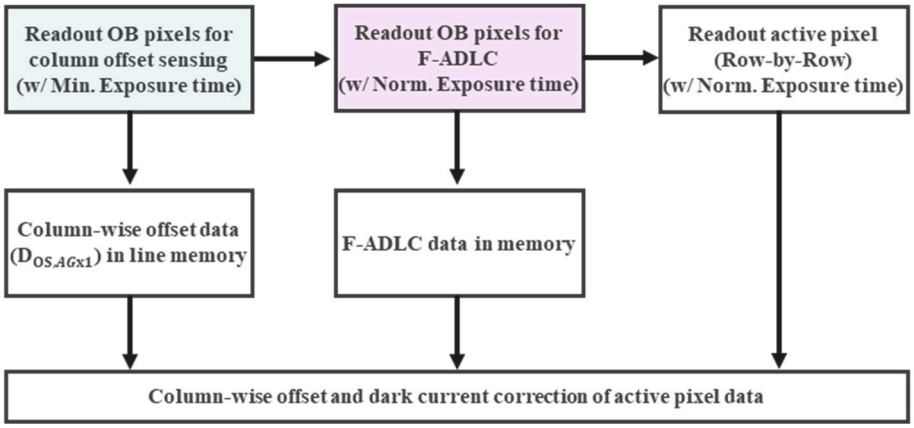


Figure 9. Digital column offset and dark-current compensation flow using optical black (OB) pixels. OB pixels are sequentially read out for column-wise offset sensing and frame-adaptive dark-level correction (F-ADLC), followed by row-by-row readout of active pixels. The measured column-wise offset and F-ADLC data are stored in memory and applied in the ISP to compensate for the reconstructed full code of active pixel data.

During full-code reconstruction, the digital gain-selection result indicated by the AGC signal in Figure 5 determines how the CDS output is interpreted and which calibration terms are applied. When the AGC result is low (AGH-only mode), the CDS output is

$$D_{\mathrm{CDS}} = D_{\mathrm{SIG,AGH}} - D_{\mathrm{RST,AGH}} \tag{15}$$

which directly represents pixel signals in the range from 0 to $2^N - 1$. Conversely, when the AGC result is high (indicating AGH–AG_{x1} mode), the full code is reconstructed by incorporating the pre-measured column-level dark reference data to compensate for the gain-dependent offset step. As derived in (16), the CDS output is computed from the difference between the light and dark conversions under the specific AGH–AG_{x1} transitions:

$$D_{\mathrm{CDS}} = \left(D^{\mathrm{light}}_{\mathrm{SIG,AGH\ -\ AGx1}} - D^{\mathrm{dark}}_{\mathrm{SIG,AGH\ -\ AGx1}}\right) - \left(D^{\mathrm{light}}_{\mathrm{RST,AGH\ -\ AGx8}} - D^{\mathrm{dark}}_{\mathrm{RST,AGH\ -\ AGx8}}\right) \tag{16}$$

By retrieving the gain-specific dark codes from memory and performing this subtraction, the ISP effectively eliminates the inherent offset component, ensuring a seamless and monotonic transition between the two gain modes. After applying the AGH scaling factor, the CDS result in the AGH–AG_{x1} mode maps to the output code range from 2^N up to $(2^N - 1) \times AGH$, thereby extending the dynamic range while ideally maintaining continuity with the AGH-only region. However, although the offset term can be removed through digital compensation, multiplying the AGH–AG_{x1} data by the fixed AGH factor can amplify column-to-column gain errors originating from capacitive mismatch in the ramp-side attenuation network. In the proposed architecture, the AGH scaling factor is applied

digitally and identically across all columns. In contrast, the effective AG_{x1} ramp gain is determined by the analog capacitive attenuation network and can vary from column to column due to mismatch. This inconsistency results in a column-dependent gain error after digital reconstruction, which may introduce residual deviation near the transition point at 2^N and potentially disturb continuity between the AGH-only and AGH–AG_{x1} regions. Let the effective AG_{x1} gain of a given column be expressed as $1 + \varepsilon_G$, where ε_G denotes the relative gain error. Near the transition boundary, the resulting deviation in the AG_{x1} code can be approximated as

$$\Delta D_{\mathrm{AGx1}} \approx \varepsilon_G \cdot \frac{2^N}{\mathrm{AGH}}, \tag{17}$$

where N is the resolution of the single-slope ADC. To preserve continuity and monotonicity across the transition, this deviation must remain within ±0.5 LSB in the AG_{x1} code domain. This requirement yields:

$$| \Delta D_{\mathrm{AGx1}} | < \frac{1}{2} \Rightarrow | \varepsilon_G | < \frac{\mathrm{AGH}}{2^{N+1}} \tag{18}$$

In this work, the AGH factor is set to 8 to achieve wide dynamic range extension. For a 10-bit ADC ($N = 10$), the above condition yields an allowable gain error of approximately

$$| \varepsilon_G | < \frac{8}{2^{11}} \approx 0.39\% \tag{19}$$

To ensure sufficient matching precision within the layout, the unit capacitor in the ramp-side attenuation network was sized at 50 fF. Given the susceptibility of such minute capacitance to interconnect parasitics at the 110 nm node, a selective shielding strategy was employed. Specifically, grounded metal layers were routed to isolate the capacitor array from high-swing digital signals, such as the AGC lines, thereby suppressing cross-coupling. Post-layout extraction, which accounted for all intra-layer and inter-layer parasitics as well as switch transistor capacitances, confirms that this implementation achieves the required gain consistency. As confirmed by the Monte Carlo simulation results shown in Figure 10, the resulting column-wise gain variation stays within the allowable range across process and temperature corners, thereby preserving continuous and monotonic full-code reconstruction over the extended dynamic range.

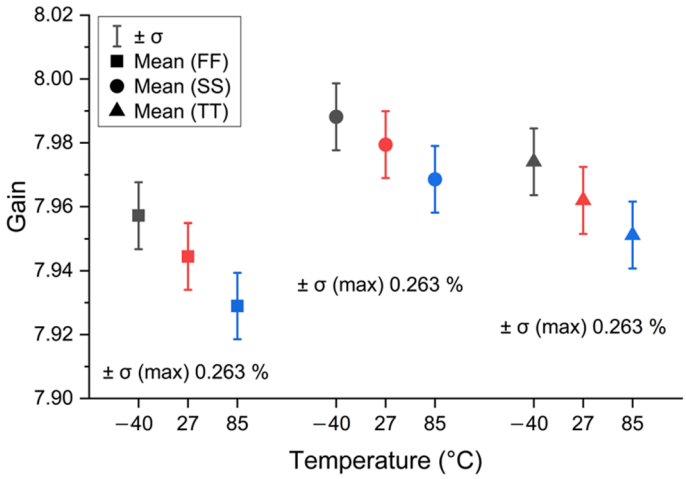


Figure 10. Adaptive-gain ratio results of the designed capacitive network obtained from Monte Carlo simulations with 1000 samples across different process and temperature corners.

4. Simulation Results

The proposed adaptive-gain single-slope (SS) ADC was designed using a standard 110 nm CMOS image sensor process, operating with supply voltages of 3.3 V for the analog domain and 1.2 V for the digital domain. All performance metrics reported in this work were obtained from comprehensive post-layout simulations of the analog blocks, including parasitics extracted with a full Resistance–Capacitance-Coupling capacitance (RCC) level, and physical layout constraints to ensure realistic evaluation. Based on post-layout timing analysis, a global Gray-code counter is

shared among 128 columns to ensure sufficient counting speed and timing margin at this technology node. At a counting frequency of 1.4 GHz, the total power consumption per column is 36.8 µW. The detailed power breakdown in Table 1 shows that the comparator and ramp buffer dominate the power consumption, while the additional AG logic contributes negligibly to the overall budget.

Table 1. Power breakdown of the core blocks used in the SS ADC.

Block Name	Power Per Column (µW)
Ramp Buffer	13.1 (3.3 V Domain)
Comparator	15.7 (3.3–1.2 V Domain)
AG Logic	0.00968 (1.2 V Domain)
Gray Counter	2.84 (1.2 V Domain)
Binary Counter	5.12 (1.2 V Domain)
Total	**36.8**

The input-referred dark noise was evaluated for gain configurations ranging from ×1 to ×16 and AG_{x2}–AG_{x1} to AG_{x16}–AG_{x1} for adaptive-gain operation. For these simulations, a pixel with a 15,000 e- full-well capacity (FWC), a 100 µV/e- conversion gain (CG), and a 120 µVrms source follower noise was assumed. This CG value represents a conservative baseline for high-performance sensors; in practical applications with higher conversion gains (e.g., over 180 µV/e-), the input-referred noise in the electron domain would be further reduced. As shown in Figure 11, the integrated noise decreases as the analog gain increases. This trend is primarily attributed to the reduction in effective noise bandwidth. As analyzed in [19], the noise bandwidth of a single-slope ADC (SS-ADC) employing correlated double sampling (CDS) is fundamentally determined by its time-varying system characteristics rather than static pole locations. In the proposed architecture, the effective noise bandwidth is dynamically modulated by the ramp signal slope at the comparator input. A lower ramp slope (higher gain) effectively narrows the effective noise bandwidth toward the OTA's AC bandwidth, leading to the reduction in total integrated noise observed in Figure 11. This time-domain bandwidth modulation governs the noise performance across different gain modes. Depending on the gain configuration, single-gain operation shows the noise values ranging from 5.242 e- to 1.668 e-, while adaptive-gain modes exhibit an input-referred noise range of 3.096 e- to 1.669 e-. The adaptive-gain mode shows slightly higher noise compared to the equivalent high-gain mode due to the additional CDS time (500 ns) required for AGC operation; however, this timing overhead has a negligible impact on the total integrated noise.

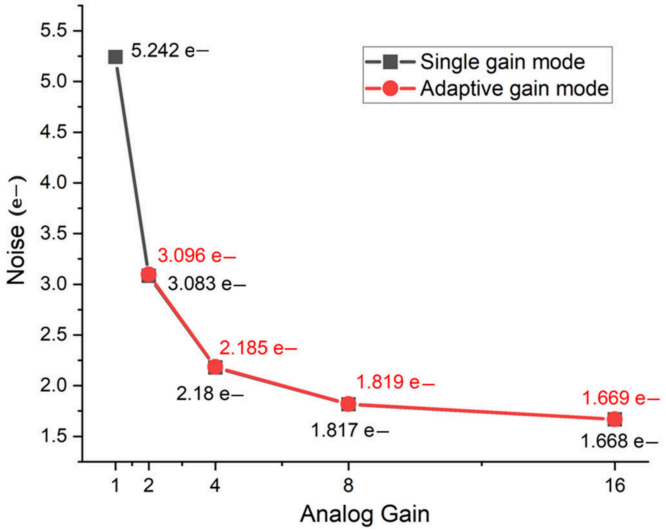
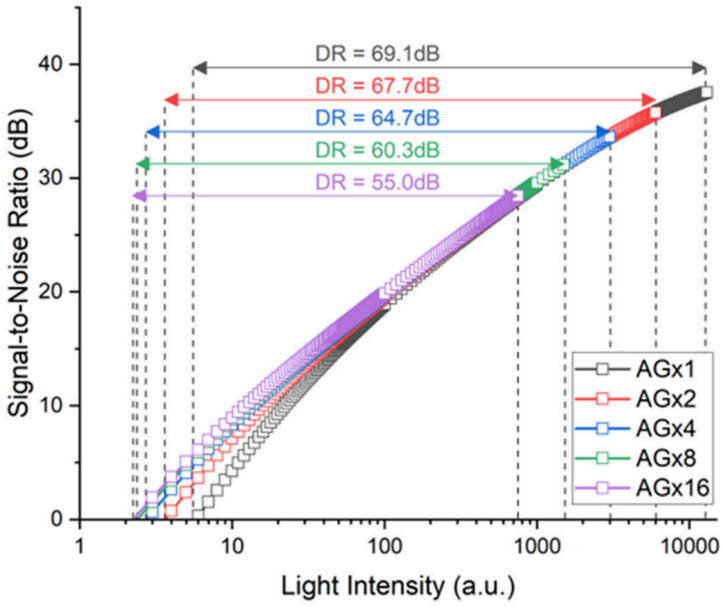


Figure 11. Input-referred noise according to analog gain.

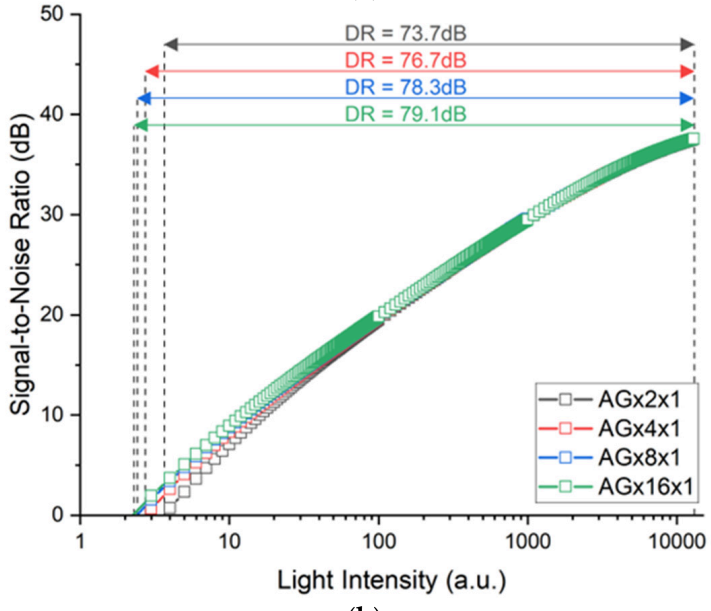
At the gain transition points, photon shot noise becomes the dominant noise component, significantly exceeding the dark noise. For example, the calculated shot noise at the transition points for AG_{x4}–AG_{x1} and AG_{x8}–AG_{x1} configurations is 61.16 e- and 44.72 e-, respectively. Since the

shot noise effectively masks the dark noise at these signal levels, switching to the AG_{x1} mode for higher intensities does not lead to a noticeable noise penalty. Consequently, the proposed adaptive-gain scheme maintains a smooth SNR transition across gain boundaries, ensuring seamless and high-quality HDR reconstruction.

Figure 12a illustrates the SNR curves and achievable DR for single-gain operations. While high-gain settings (up to ×16) shift the noise floor (SNR = 0 dB) toward the dark region, the peak SNR is simultaneously constrained by the reduced ADC swing range. In contrast, as shown in Figure 12b, the proposed adaptive-gain scheme maintains the maximum peak SNR across all levels because it dynamically switches the gain before reaching the saturation limit of high-gain operation. Simultaneously, it benefits from the high-gain noise floor in dark regions. Consequently, the proposed AG_{x8}–AG_{x1} configuration achieves a dynamic range of 78.3 dB, representing an improvement of 18 dB and 23.3 dB compared to AG_{x1} and AG_{x8} single-gain operations, respectively.



(**a**)



(**b**)

Figure 12. SNR and DR results for (**a**) single gain readout and (**b**) adaptive-gain readout.

Particular attention was given to evaluating potential non-ideal effects introduced by capacitive gain switching, such as linearity degradation and inter-column interference. The linearity results presented in Figure 13 confirm that the proposed digital offset calibration and gain-matching strategy effectively suppress transition-induced errors. The integral nonlinearity (INL) remains below 1% across the full input range, with no missing codes observed. To assess inter-column crosstalk, simulations were conducted on an array of eight adjacent columns. While the fourth column was swept across its entire input range, the neighboring columns were held under dark conditions to monitor any digital code deviation. By shielding the comparator decision paths and AGC feedback signals routed along the column height, the induced code variation was limited to a range of +0.3 DN to −0.6 DN, as shown in Figure 14. These results verify that the proposed architecture maintains high signal integrity during high-speed adaptive-gain operation. Finally, Table 2 summarizes the simulated performance of the proposed design and compares it with prior state-of-the-art adaptive-gain and HDR-enhanced ADC architectures.

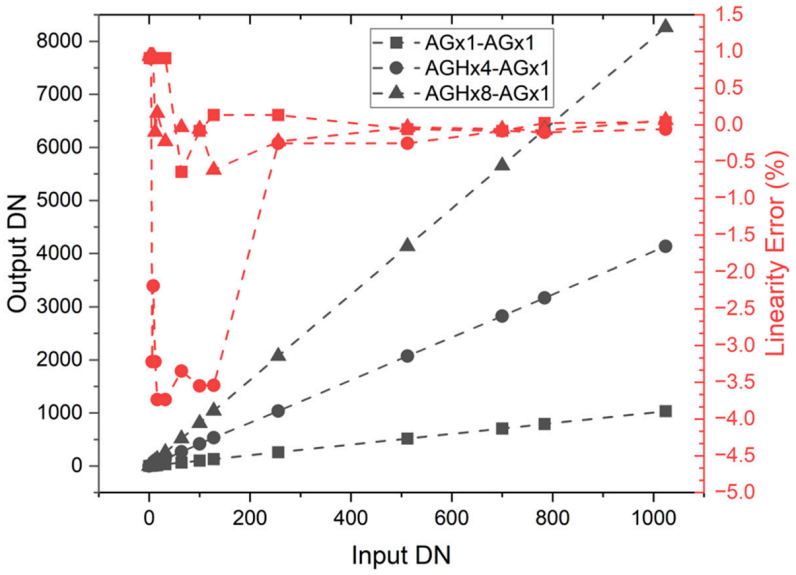


Figure 13. Sensor code linearity and linearity error.

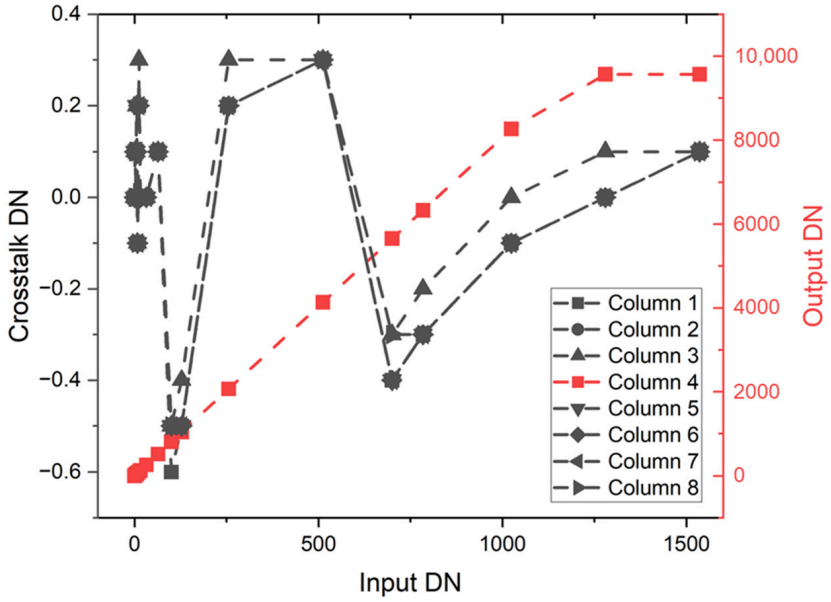


Figure 14. Crosstalk simulation over eight columns.

Table 2. Performance summary and comparison.

Reference	[12]	[13]	[14]	This Work [a]
Process	130 nm	90 nm, 40 nm (logic)	90 nm, 65 nm (logic)	110 nm
Resolution (bits) [b]	10 + 2	12 + 2	12 + 2	10 + 3
Conversion time (µs)	N/A	11	6.69	10.5
Adaptive-gain method	Signal gain	Ramp gain	Ramp gain	Ramp gain
Additional circuits for adaptive-gain operation	Amplifier	Active Sample and Hold	Dual ramp generator	No
Adaptive-gain mode	1×, 4×	N/A	1×, 4×	1×, 8×
Column-wise calibration	Per 8 blocks	No	No	Yes
ADC counter-clock frequency (GHz)	0.81	N/A	2.672	1.4
Nonlinearity	±5 LSB	<0.3%	<0.18%	< 1%
Dark random noise (e-rms)	3.5	1.6	4.6	1.6
Dynamic range (dB)	66.7	78	76.3	78.3
FoM [c]	N/A	1.378×10^{-5}	2.462×10^{-5}	2.619×10^{-5}

[a] Simulation results, [b] Final digital code resolution with adaptive-gain operation, [c] FoM = ([Conversion time(µs)] × [Noise(e-)])/(2^[Resolution] × [Dynamic Range(dB)]).

5. Conclusions

In this work, a column-parallel adaptive-gain single-slope ADC architecture has been developed to enable high-speed HDR operation without resorting to dual-ramp generation or duplicated column circuits. By locally reconfiguring the capacitive attenuation network at each comparator input while sharing a single global ramp, the proposed approach preserves architectural simplicity and scalability while achieving adaptive gain within a single exposure and readout cycle. A key challenge in such adaptive-gain operation lies in maintaining continuity and linearity across gain transition boundaries. This work systematically addresses the associated non-idealities, including switching-induced offset and column-dependent gain mismatch, through a reconfigurable dual-source-follower structure for mode-switching offset suppression, and an optical black pixel-based calibration scheme for column-wise offset correction. As a result, the proposed architecture maintains linearity without missing codes and ensures stable transition behavior. With modest per-column power consumption and compatibility with a standard CMOS image sensor process, the proposed ADC provides a low-overhead implementation for HDR image sensors that require low cost, extended dynamic range, and robust image quality.

Author Contributions: Circuit design, layout and simulation, H.Y. and C.P.; writing—original draft preparation, H.Y., C.P., M.J. and M.C.; project administration, M.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Global Semiconductor Advanced Fab Utilization Project through the National NanoFab Center, funded by the Ministry of Science and ICT, Republic of Korea (No. RS-2024-00511995).

Data Availability Statement: Data is contained within the article.

Acknowledgments: The authors would like to express their sincere gratitude to Stefan De Gendt of imec for his invaluable coordination of the IMEC-NNFC project. His leadership and support were essential in successfully conducting the NNFC internship project, which provided the foundational environment and resources to complete this work.

Conflicts of Interest: All authors were employed by the company IMEC. The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

References

1. Sugimura, D.; Mikami, T.; Yamashita, H.; Hamamoto, T. Enhancing color images of extremely low light scenes based on RGB/NIR images acquisition with different exposure times. *IEEE Trans. Image Process.* **2015**, *24*, 3586–3597. [CrossRef] [PubMed]
2. Velichko, S.; Johnson, S.; Pates, D.; Silsby, C.; Hoekstra, C.; Mentzer, R.; Beck, J. 140 dB dynamic range sub-electron noise floor image sensor. In Proceedings of the International Image Sensor Workshop (IISW), Hiroshima, Japan, 30 May–2 June 2017.
3. Lim, Y.; Koh, K.; Kim, K.; Yang, H.; Kim, J.; Jeong, Y.; Lee, S.; Lee, H.; Lim, S.-H.; Han, Y.; et al. A 1.1e- temporal noise 1/3.2-inch 8Mpixel CMOS image sensor using pseudo-multiple sampling. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 7–11 February 2010; pp. 396–397.
4. Kitamura, K.; Theuwissen, A. A two conversions/sample differential slope multiple sampling ADC with accelerated counter architecture. In Proceedings of the International Image Sensor Workshop (IISW), Vaals, The Netherlands, 8–11 June 2015.
5. Yeh, S.-F.; Chou, K.-Y.; Tu, H.-Y.; Chao, C.Y.-P.; Hsueh, F.-L. A 0.66 e^- rms temporal-readout-noise 3D-stacked CMOS image sensor with conditional correlated multiple sampling (CCMS) technique. In Proceedings of the IEEE Symposium on VLSI Circuits, Kyoto, Japan, 16–19 June 2015; pp. C84–C85.
6. Ma, C.; Liu, Y.; Li, J.; Zhou, Q.; Chang, Y.; Wang, X. A 4MP high-dynamic-range, low-noise CMOS image sensor. In Proceedings of the SPIE 9403, Image Sensors and Imaging Systems, San Francisco, CA, USA, 9–10 February 2015; p. 940305.
7. Jang, D.; Park, D.; Cha, S.; Kwon, H.; Kim, M.; Lee, S.; Lee, H.; Kim, S.; Lee, N.; Han, J.; et al. 0.8 µm-pitch CMOS image sensor with dual conversion gain pixel for mobile applications. In Proceedings of the International Image Sensor Workshop (IISW), Snowbird, UT, USA, 23–27 June 2019.
8. Akahane, N.; Sugawa, S.; Adachi, S.; Mori, K.; Ishiuchi, T.; Mizobuchi, K. A sensitivity and linearity improvement of a 100-dB dynamic range CMOS image sensor using a lateral overflow integration capacitor. *IEEE J. Solid-State Circuits* **2006**, *41*, 851–858. [CrossRef]
9. Fujihara, Y.; Murata, M.; Nakayama, S.; Kuroda, R.; Sugawa, S. An over 120 dB single exposure wide dynamic range CMOS image sensor with two-stage lateral overflow integration capacitor. *IEEE Trans. Electron Devices* **2021**, *68*, 152–157. [CrossRef]
10. Willassen, T.; Solhusvik, J.; Johansson, R.; Yaghmai, S.; Rhodes, H.; Manabe, S.; Mao, D.; Lin, Z.; Yang, D.; Cellek, O.; et al. A 1280×1080 4.2µm split-diode pixel HDR sensor in 110nm BSI CMOS process. In Proceedings of the International Image Sensor Workshop (IISW), Vaals, The Netherlands, 8–11 June 2015; pp. 8–11.
11. Iida, S.; Sakano, Y.; Asatsuma, T.; Takami, M.; Yoshiba, I.; Ohba, N.; Mizuno, H.; Oka, T.; Yamaguchi, K.; Suzuki, A.; et al. A 0.68e- rms random-noise 121dB dynamic-range sub-pixel architecture CMOS image sensor with LED flicker mitigation. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 10.2.1–10.2.4.
12. Totsuka, H.; Tsuboi, T.; Muto, T.; Yoshida, D.; Matsuno, Y.; Ohmura, M.; Takahashi, H.; Sakurai, K.; Ichikawa, T.; Yuzurihara, H.; et al. An APS-H-size 250Mpixel CMOS image sensor using column single-slope ADCs with dual-gain amplifiers. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 31 January–4 February 2016; pp. 116–117.
13. Hung, L.; Matsuura, K.; Suto, H.; Kodama, K.; Tanaka, Y.; Ono, T.; Fujimagari, J.; Akiyama, K.; Akahide, M.; Inada, Y. An 0.08 e^-· pJ/step 14-bit gain-adaptive single-slope column ADC with enhanced HDR function for high-quality imagers. In Proceedings of the IEEE Symposium on VLSI Technology and Circuits, Kyoto, Japan, 11–16 June 2023; pp. 1–2.
14. Oike, Y.; Akiyama, K.; Hung, L.D.; Niitsuma, W.; Kato, A.; Sato, M.; Kato, Y.; Nakamura, W.; Shiroshita, H.; Sakano, Y.; et al. 8.3 M-pixel 480-fps global-shutter CMOS image sensor with gain-adaptive column ADCs and chip-on-chip stacked integration. *IEEE J. Solid-State Circuits* **2017**, *52*, 985–993. [CrossRef]
15. Lee, Y.; Kim, S.; Jun, J. A 10-bit 13.3 µW single-slope analog-to-digital converter with auto-zero power-down technique. *Electron. Lett.* **2024**, *60*, e13148. [CrossRef]
16. Lee, Y.; Kim, S.; Kim, J.; Kim, S.; Jun, J. A low power digitizer array with adaptive split current source for 3D-stacked 100 MP high dynamic range imager. *IEEE Sens. J.* **2025**, *25*, 22609–22617. [CrossRef]
17. Jun, J.; Seo, H.; Kwon, H.; Lee, J.; Yoon, B.; Lee, Y.; Kim, Y.; Joo, W.; Lee, J.; Koh, K. A 0.7 µm-pitch 108 mpixel nonacell-based CMOS image sensor with decision-feedback technique. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX, USA, 27 May–1 June 2022; pp. 283–287.
18. Park, S.-Y.; Kim, H.-J. CMOS image sensor with two-step single slope ADC using differential ramp generator. *IEEE Trans. Electron Devices* **2021**, *68*, 4966–4971. [CrossRef]
19. Jung, H.-Y.; Chu, M.; Seo, M.-W.; Kim, S.; Song, J.; Lee, S.-G.; Byun, S.-J.; Kim, M.; Bae, D.; Lee, J.; et al. Design and analysis on low-power and low-noise single slope ADC for digital pixel sensors. In Proceedings of the IS&T Int'l. Symposium on Electronic Imaging: Imaging Sensors and Systems, Online, 17–26 January 2022; pp. 256-1–256-4.