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ABSTRACT

Owing to its broad transparency window, ultra-low propagation losses, and compatibility with complementary metal–oxide–semiconductor (CMOS) fabrication processes, silicon nitride (SiN) has emerged as a highly attractive platform for extending integrated photonics into the visible and near-infrared spectrum. By incorporating active components such as modulators, light sources, and detectors, complex photonic systems with unprecedented functionality and performance become possible. These systems enable a wide range of applications, including biosensing, on-chip spectroscopy, imaging, and quantum computing. However, the low refractive index of SiN relative to III–V gain materials poses a major challenge for implementing evanescently coupled lasers, the dominant coupling scheme in silicon photonics at the telecommunication wavelengths. Although a silicon intermediate layer is often used to alleviate this mismatch, its strong absorption at shorter wavelengths precludes its use. Here, we present an integration strategy that overcomes this limitation by employing a CMOS-compatible a-Si:H layer with two etch depths, which was engineered to achieve the required optical properties at shorter wavelengths. This intermediate structure enables efficient vertical coupling between the SiN photonic circuit and a micro-transfer-printed GaAs-based semiconductor optical amplifier. Using this scheme, we demonstrate on-chip amplification with a gain of more than 13 dB as well as lasing in the submicrometre wavelength range. Finally, we showcase the versatility of this process by integrating a second amplifier stage following the laser, achieving on-chip output powers exceeding 4 mW. These results highlight the potential of this method for developing fully integrated evanescently coupled laser systems operating in the near-infrared band.

I. INTRODUCTION

The visible to near-infrared (VIS-NIR) spectrum is essential for advanced optical technologies, spanning applications from biomedical imaging to precision sensing. Techniques such as optical coherence tomography (OCT) leverage this spectral range to achieve high-resolution imaging, benefiting from the low absorption of water, which allows deeper penetration into biological tissues.[1]

The realization of such demanding applications has been greatly accelerated by the rapid advancement of integrated photonics over the past decades. This progress has enabled the development of complex optical systems on a chip, offering unmatched scalability, compactness, cost-effectiveness, and performance.[2,3] However, the widely adopted silicon-on-insulator (SOI) platform, which dominates the photonics industry, is unsuitable for wavelengths below 1.1 μm due to the significant absorption of silicon in this spectral region.

Silicon nitride (SiN) has emerged as a leading material for integrated photonics in this wavelength range due to its broad transparency window and exceptionally low optical losses, which can reach sub-dB/cm values near 405 nm.[4,5] Furthermore, the SiN platform leverages the mature complementary metal–oxide–semiconductor (CMOS) infrastructure originally developed for the electronics industry, allowing for scalable manufacturing. This compatibility, as highlighted in a recent review of CMOS-integrated technologies,[6] supports a wide range of applications by facilitating seamless electronic–photonic co-integration. Finally, the lower refractive index contrast compared to silicon-on-insulator platforms provides greater tolerance to fabrication imperfections, which in turn enhances process robustness and improves the overall reliability of photonic devices.

However, realizing full photonic functionality on-chip beyond passive guiding requires the integration of active components such as lasers, modulators, and photodetectors that operate efficiently in the VIS-NIR range. While GaAs-based nanoridge lasers have been successfully monolithically grown on 300 mm silicon wafers,[7] heterogeneous integration, such as wafer bonding and flip-chip, has emerged as a highly promising strategy for managing the increasing complexity of photonic systems due to enabling the co-integration of diverse materials on a single platform.[2,8–10] Among these approaches, micro-transfer printing (MTP) stands out as a highly flexible and versatile heterogeneous integration method,[11,12] having demonstrated successful incorporation of components such as lithium niobate and lithium tantalate modulators,[13,14] III–V-based photodetectors,[15,16] and lasers or LEDs based on gallium nitride (GaN), gallium arsenide (GaAs), indium phosphide (InP), and other III–V materials.[17–20]

Nonetheless, a significant challenge remains. The large refractive index contrast between SiN (2) and III–V (3.4) semiconductors severely limits efficient mode coupling. Consequently, conventional adiabatic tapering strategies, originally developed for silicon-on-insulator (SOI) platforms with more moderate index differences, are not directly applicable. Direct III–V-to-SiN butt-coupling has emerged as an effective approach to overcome this large index mismatch at shorter wavelengths, as evidenced by the recent demonstration of micro-transfer-printed 800 nm lasers on SiN.[21] In addition to enabling efficient coupling, this approach benefits from superior thermal handling, since the III–V device can be integrated directly on top of silicon, eliminating the buried oxide that would otherwise act as a thermal insulator. However, direct butt-coupling imposes stringent requirements on vertical alignment accuracy, which complicates its implementation in wafer-scale fabrication. To relax these alignment constraints, an alternative two-step coupling strategy employing an intermediate dielectric layer has been proposed.[22] In this scheme, submicrometre-emitting lasers have been demonstrated using wafer bonding, in which light is first butt-coupled from the III–V device into an intermediate dielectric layer, followed by evanescent-coupling from the dielectric layer to the SiN waveguide. While this approach improves alignment tolerance and enables efficient mode coupling, it relies on etched facets, which introduce reliability concerns,[23,24] particularly in applications demanding long-term stability, such as in space-based photonic systems. On the other hand, even though the use of cleaved facets with specialized coatings could improve laser longevity by mitigating facet-related degradation,[25,26] currently no wafer-scale integration using cleaved facets has been shown. Consequently, extending evanescent coupling schemes to shorter wavelengths remains a key challenge, as these approaches have the potential to combine the robustness and high coupling efficiency of fully adiabatic transitions with the maturity and scalability of CMOS-compatible fabrication processes.

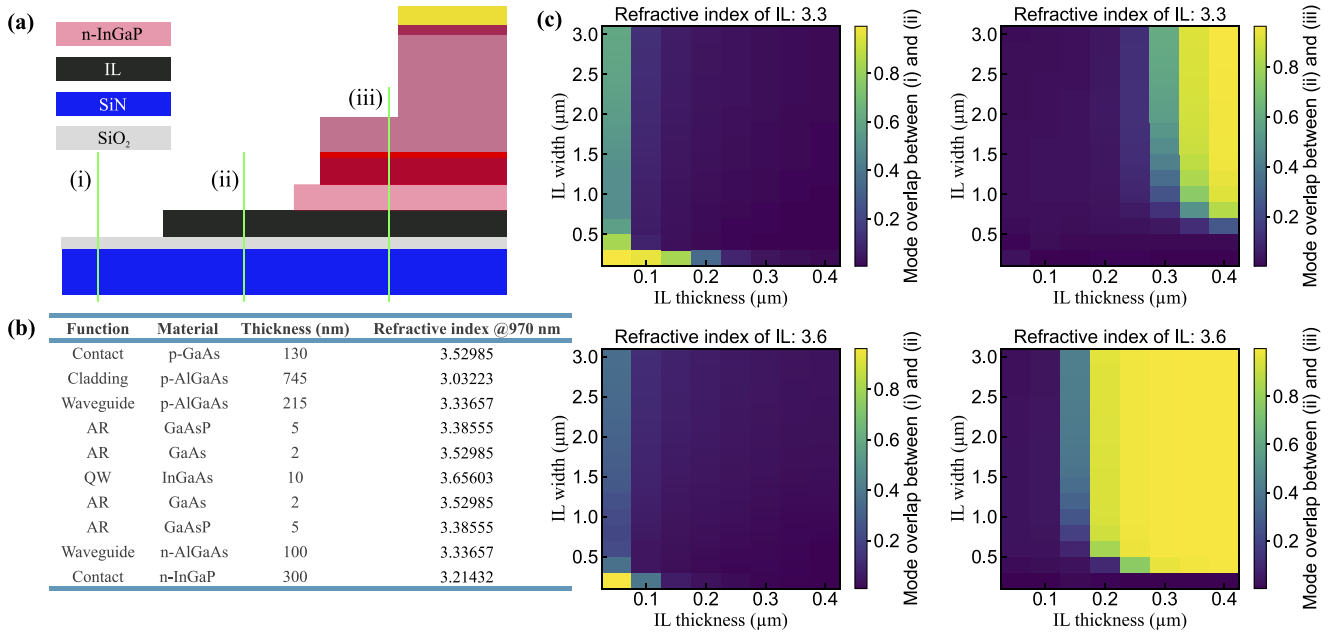
By introducing an intermediate layer with tailored geometry and optical properties, adiabatic coupling can be achieved at both interfaces, accommodating the refractive index requirements of both SiN and III–V materials. In addition, this multilayer strategy eliminates the need for optical facets while preserving CMOS-compatibility and scalability. Such approaches have previously been demonstrated at 1550 nm using silicon[27,28] or hydrogenated amorphous silicon (a-Si:H)[29] intermediate layers to facilitate coupling between the SiN and the III–V devices. Compared with other suitable candidates, such as gallium phosphide (GaP) and GaAs, these intermediate layer solutions maintain full CMOS compatibility and avoid complex integration processes.

However, while evanescent III–V-on-SiN coupling using a-Si:H or Si-based interlayers has been explored at telecom wavelengths, extending this approach to the submicrometre regime is non-trivial. At shorter wavelengths, a-Si:H exhibits significantly increased optical absorption, and the reduced mode size imposes stricter constraints on adiabatic coupling design. In this work, we address these challenges by employing a robust, misalignment tolerant, multi-taper transition based on an a-Si:H layer with two etch depths and a deposition recipe optimized for lower loss at short wavelengths. This enables the demonstration of CMOS-compatible evanescently coupled GaAs-based amplifiers and lasers on SiN operating in the submicrometre wavelength range.

II. DESIGN

To ensure the adiabatic mode transition between the SiN waveguide and the III–V semiconductor optical amplifier (SOA), an intermediate layer is introduced [Fig. 1(a)]. Its required optical properties will be determined by the phase-matching condition, where the effective indices of the coupled modes must remain sufficiently close to enable gradual energy transfer without exciting higher-order modes.[30] This must be achieved while also considering fabrication constraints. The III–V SOA stack, which is shown in the table in Fig. 1, has a minimum tip width of 300 nm due to the high aspect ratio of the device and a minimum n-type contact thickness of 300 nm, which should remain thick enough to not degrade its electrical characteristics.

Ideally, the mode must remain largely unperturbed each time a new layer is introduced, gradually transitioning to the new layer. This implies that the mode stays predominantly in the SiN when the intermediate layer is added, and similarly remains in the intermediate layer once the SOA is placed on top. By evaluating the overlap between the fundamental TE mode of the decoupled layer and the fundamental TE supermode [Figs. 1(i, ii) and (ii, iii)] as a function of the intermediate layer's refractive index, thickness, and width, we can identify which refractive indices and therefore which materials are suitable at this wavelength. This is also the motivation for



Function	Material	Thickness (nm)	Refractive index @970 nm
Contact	p-GaAs	130	3.52985
Cladding	p-AlGaAs	745	3.03223
Waveguide	p-AlGaAs	215	3.33657
AR	GaAsP	5	3.38555
AR	GaAs	2	3.52985
QW	InGaAs	10	3.65603
AR	GaAs	2	3.52985
AR	GaAsP	5	3.38555
Waveguide	n-AlGaAs	100	3.33657
Contact	n-InGaP	300	3.21432

FIG. 1. (a) Side view of the device depicting the 300 nm thick, 3 μm wide SiN layer, the intermediate layer (IL), and the III–V SOA on top. The underlying 2.9 μm thick thermal oxide is omitted for clarity. The three regions of interest for the mode overlap calculation are shown. The intermediate layer is depicted as a black box with the refractive index, width, and thickness as design parameters. (b) Epitaxial layer stack of the SOA. For the refractive indices, the wavelength 970 nm is considered. (c) 2D colormaps depicting the calculated mode overlap at 970 nm between the IL and SiN or III–V for different refractive indices and geometries of the IL.

choosing a 3 μm wide, 300 nm thick SiN waveguide, which ensures a high effective index and helps keep the mode confined within the SiN.

The mode overlaps were calculated using Lumerical's built-in mode overlap function at a wavelength of 970 nm, and the results are shown in Fig. 1(c). For a refractive index of 3.3, an intermediate layer thickness of ~400 nm is required to achieve >95% overlap when the III–V is introduced. This leaves little margin for increasing either the thickness of the n-type contact layer or the minimum III–V tip width beyond 300 nm, the latter potentially being imposed by the high aspect ratio of the structure. Increasing the refractive index to 3.6 reduces the required thickness to ~200 nm. On the SiN side, a thickness of roughly 50 nm is sufficient in both cases. These results highlight two important points. First, the intermediate layer must exhibit a relatively high refractive index (>3.3), effectively ruling out CMOS-compatible materials such as silicon-rich SiN. Second, a single thickness is not sufficient for optimal coupling, necessitating two distinct etch depths. Within the range of refractive indices above 3.3, we therefore selected values that keep the two required thicknesses as close as possible. This choice minimizes transition losses, relaxes the processing burden associated with depositing very thick layers, and provides greater design flexibility for the III–V SOA, particularly if a tip width larger than 300 nm or an n-type contact layer thicker than 300 nm is required. Based on these considerations, an intermediate layer refractive index of ~3.5–3.6 is most desirable. Among the available materials, hydrogenated amorphous silicon uniquely satisfies these requirements by combining a high refractive index with CMOS compatibility and a mature low-temperature deposition process, which makes it particularly well suited for NIR and telecom photonic platforms.

To assess the potential of the integration scheme, the refractive index and material losses of various 220 nm thick a-Si:H recipes were characterized using ellipsometry and the cutback method, respectively. Waveguides with lengths ranging from 1 to 6 mm and widths ranging from 300 to 6000 nm were fabricated via electron beam lithography (EBL) and reactive ion etching. The reasoning behind the different widths was to assess the etching quality. By increasing the width, the scattering losses due to the roughness of the sidewalls are reduced, isolating the contribution of material absorption. Light was coupled in and out through grating couplers fabricated directly on the a–Si:H layer. From these measurements, shown in Fig. 2, the propagation loss at 948 nm decreases from ~70 dB/cm for a 300 nm wide core to 13 dB/cm when the core width is increased to 6 μm. The significant loss increase for narrower core widths, combined with the pronounced sidewall roughness of a representative test structure visible in the scanning electron micrograph inset, indicates that the etching recipes employed in our R&D process environment require substantial improvement to reduce scattering losses. At the same time, the measured loss for wider waveguides demonstrates that a-Si:H exhibits promising material performance for submicrometre applications: for a typical taper transition length of 100 μm, this corresponds to ~0.13 dB of total material loss. With further optimization of the a-Si:H deposition recipes, the usability of this integration scheme can be extended to shorter wavelengths. While

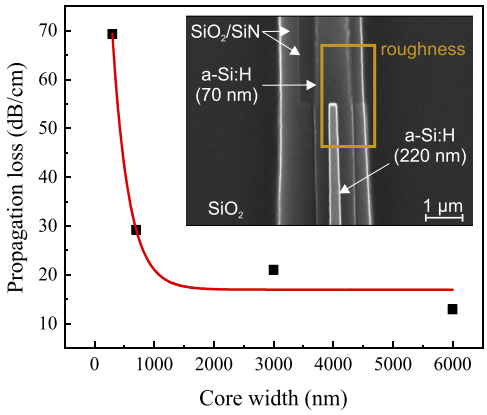


FIG. 2. Propagation loss measurement of 220 nm thick a–Si:H waveguides for different core widths at a wavelength of 948 nm. The inset shows a scanning electron microscope image of a representative test structure. The pronounced sidewall roughness associated with the fabrication is particularly evident in the 70 nm thick a–Si:H layer. Contrast variations in the SiO_2/SiN layer arise from the locally thinned oxide during the processing.

state-of-the-art a-Si:H waveguides have demonstrated sub-1 dB/cm at telecom wavelengths,[31] propagation losses of ~15 dB/cm have also been reported at 830 nm for amorphous silicon waveguides.[32] Taken together, these results suggest that the proposed integration scheme could form part of a broadband platform spanning wavelengths from the telecom regime down to ~800 nm, provided that material absorption, etching-induced scattering and the refractive index are carefully optimized.

With an a–Si:H recipe found, we proceeded with the design of the tapers. To relax fabrication constraints and maintain compatibility with DUV lithography, a minimum feature size of 120 nm was selected for the passive circuitry. A schematic representation of the full transition is shown in Fig. 3(a), along with the transverse electric (TE) mode profiles at key positions along the tapers, obtained through Lumerical finite difference eigenmode (FDE) simulations at a wavelength of 970 nm. With the introduction of each successive layer, the optical modes remain localized at their initial positions and only gradually transition, confirming the feasibility of the evanescent coupling scheme at this wavelength. Figures 3(b) and 3(c) display scanning electron microscope (SEM) and optical microscope images of the final fabricated device, respectively.

To couple the optical mode from the 300 nm thick low-pressure chemical vapor deposition (LPCVD) SiN layer into the a-Si:H layer, a 70 nm thick a-Si:H taper is designed, separated by a thin SiO_2 spacer. This spacer minimizes perturbations to the mode and also serves as an etch-stop layer, as detailed in Sec. III. The taper begins with a 120 nm wide tip and expands to 1200 nm over a length of 25 μm. In the second stage, the mode transitions into the 220 nm thick a-Si:H layer via a second taper of 15 μm, which broadens from 120 to 600 nm. Subsequently, the waveguide widens to 1.65 μm over an additional 15 μm, followed by a straight section. This

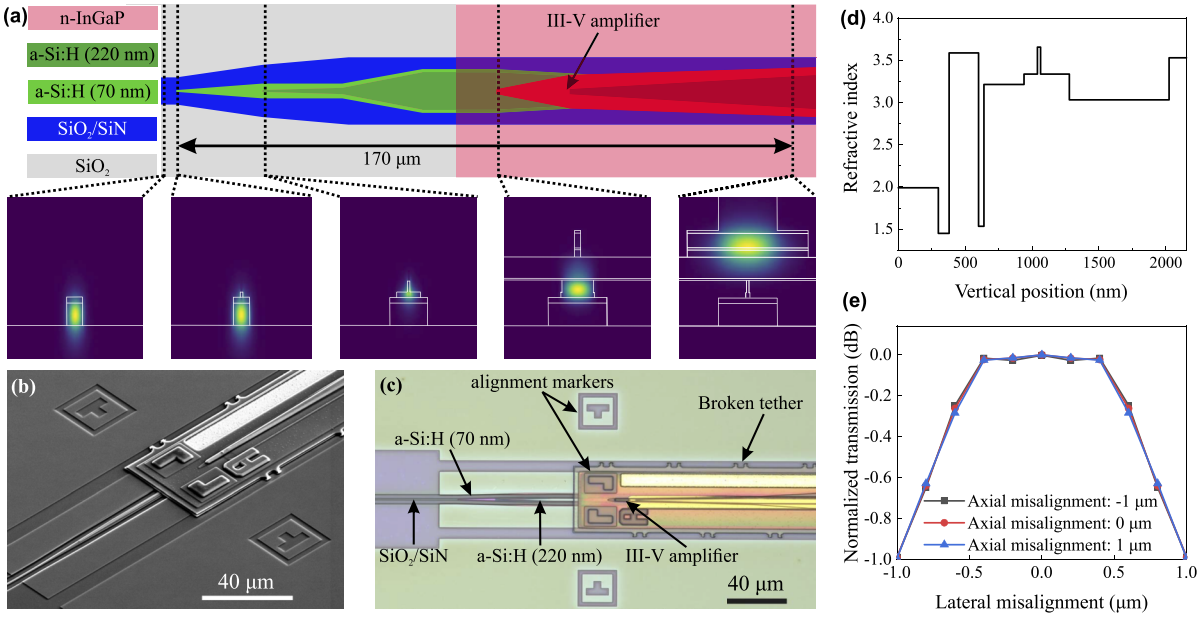


FIG. 3. (a) Schematic layout depicting the required tapers for efficient coupling between the SiN waveguide and the micro-transfer printed GaAs-based amplifier. The different colors in the III–V section illustrate the multi-taper transitions in the epitaxial layers. Simulated fundamental TE mode profiles are shown at critical locations along the transition. The adhesive BCB layer is omitted from the schematic for clarity. [(b), (c)] SEM and optical microscope images of the integrated amplifier on the SiN chip. (d) Schematic of the vertical refractive index profile, illustrating the waveguide stack used to achieve evanescent coupling from the passive SiN layer to the III–V amplifier. (e) Simulated normalized transmission at a wavelength of 970 nm as a function of in-plane misalignment along the lateral (Y) and axial (X) directions during the integration process.

straight segment mitigates optical interaction with the n-contact of the printed III–V amplifier and provides alignment tolerance during integration. To evaluate the coupling efficiency of these passive transitions, 3D finite-difference time-domain (FDTD) simulations were performed in Lumerical at a wavelength of 970 nm. The simulated transmission from SiN to the fundamental TE mode of the 220 nm thick a-Si:H waveguide, including the material loss of a-Si:H, was −0.36 dB, and the total reflection coupled back to the fundamental TE mode −31.6 dB. Of the total transmission loss of 0.36 dB, ~0.07 dB originates from the absorption in the a-Si:H layer, whereas the remaining 0.29 dB is attributed to the incomplete adiabatic mode transition. While longer tapers could further improve coupling efficiency, this would come with increased total optical loss due to material absorption and, most notably, sidewall roughness from non-optimized a–Si:H etching processes performed in an R&D process environment. Therefore, the chosen taper lengths represent a balance between high enough transmission and overall fabrication-induced loss minimization.

Next, the transition between the a-Si:H waveguide and the GaAs-based amplifier is simulated, incorporating a 40 nm thick benzocyclobutene (BCB) intermediate adhesion layer. The GaAs taper expands from 300 to 3000 nm, while the a-Si:H taper narrows from 1.65 μm to 120 nm over a length of 100 μm, ensuring adiabatic mode transfer. Simulations including the material loss of a-Si:H show a transmission of −0.48 dB to the fundamental TE mode of the GaAs-based waveguide, and a total reflection −41.1 dB with −66.4 dB reflected back into the fundamental TE mode. Of the total transmission loss of 0.48 dB, ~0.13 dB originates from the absorption in the a-Si:H layer, whereas the remaining 0.35 dB is attributed to mode mismatch between the waveguides. The refractive index profile, as well as the thicknesses of all materials that were used for the design process, are shown in Fig. 3(d). To assess the alignment tolerance, sensitivity simulations are performed for both lateral and axial misalignments introduced during micro-transfer printing. The results are shown in Fig. 3(e). The evaluation metric is the transmission to the fundamental TE mode in the III–V, normalized to the ideal, perfectly aligned case. With typical sample-scale MTP tools offering 1 μm (3σ) alignment accuracy, coupling efficiencies of ~80% are maintained, increasing to 95% when using state-of-the-art wafer-scale tools with an improved alignment precision of 0.5 μm. These results demonstrate that the proposed evanescent coupling scheme offers high performance and a high misalignment tolerance, making it suitable for scalable integration without the stringent processing demands associated with butt-coupling.

To assess the robustness of the platform, the impact of processing variations during the a–Si:H deposition and partial etching steps was thoroughly investigated via three-dimensional FDTD simulations. The analysis reveals that while the passive SiN to a–Si:H transition exhibits high tolerance to fabrication deviations, the transition to the GaAs-based SOA is more sensitive, particularly to negative thickness variations that disrupt taper adiabaticity. A comprehensive discussion of this study is provided in the supplementary material.

III. FABRICATION

Micro-transfer printing (MTP) is a versatile heterogeneous integration technique that uses an elastomeric polydimethylsiloxane (PDMS) stamp to transfer devices from one substrate to another with high precision. The adhesion between the PDMS stamp and the target device increases with peeling velocity, due to the viscoelastic properties of PDMS. This dynamic adhesion control enables precise transfer and placement of devices on new substrates. MTP has been successfully applied to integrate devices from a variety of material platforms, such as lithium niobate modulators, silicon photodiodes, and III–V lasers. A key feature of this technique is the use of a sacrificial layer, on which the device is grown. When this layer is removed through an underetching process, the device is left suspended on its native substrate, connected only by tethers. These tethers provide mechanical support and can be made from various materials, including photoresist, or a variety of dielectrics. The material and the dimensions of the tethers determine the force necessary to break them in the transfer process.

The fabrication process of the lasers is depicted in Fig. 4. Micro-transfer printing begins with the preparation of active devices, or "coupons" on the source III–V wafer. This wafer, consisting of a GaAs-based epitaxial layer stack, is grown and processed through multiple steps of optical i-line lithography and a combination of dry and wet etching processes to define the device mesa, expose the underlying GaAs sacrificial release layer and pattern the SiN tethers for mechanical support. Wafers containing hundreds of such devices, with varying lengths and taper designs, are then released by immersing them in a selective wet etchant composed of $NH_4OH:H_2O_2:H_2O$ in a 1:10:10 ratio for 20 min. This solution offers high selectivity against InGaP allowing clean removal of the GaAs release layer while preserving surrounding structures and producing a smooth bonding interface. Following the etch, the devices remain suspended above the substrate, supported by mirrored pairs of 700 nm thick SiN tethers with a 45 μm pitch. Each tether incorporates a narrow (2.5 μm) constriction that localizes stress and ensures deterministic breakage during micro-transfer printing. The tethers ensure sufficient adhesion to prevent coupon detachment and provide the mechanical rigidity required to resist capillary-induced collapse during the drying process. Finally, the wafer is left to dry under ambient conditions at room temperature to avoid mechanical stress on the suspended structures.

The target preparation begins with an 8-inch polished Si wafer with a 2.9 μm thermal oxide layer. Subsequently, 300 nm of LPCVD SiN is deposited, followed by an 80 nm plasma enhanced chemical vapor deposition (PECVD) silicon dioxide layer. Finally, a 220 nm layer of PECVD a-Si:H is deposited at 350 °C. The wafer is then cleaved into individual chips for further processing. For the fabrication of the passive circuitry, electron beam lithography using a positive e-beam resist (ARP.6200.13) and reactive ion etching using a mixture of CHF_3, SF_6, and O_2 are used in a top–down approach. The minimum feature size used is 120 nm, making it compatible with deep ultraviolet (DUV) lithography processes. In the first exposure, the 220 nm thick a-Si:H waveguides are patterned. During the same step, a large area is also opened for the subsequent definition of the SiN waveguides. In addition, trenches are etched at the anticipated landing locations of the coupon edges to absorb any remaining spikes left from tether breaking, preventing misalignment during printing. Next, a partial etch of 150 nm is performed to create the 70 nm thick a-Si:H layer, with the underlying 80 nm SiO_2 serving as a stop layer to protect the SiN beneath. In the third exposure, the SiN

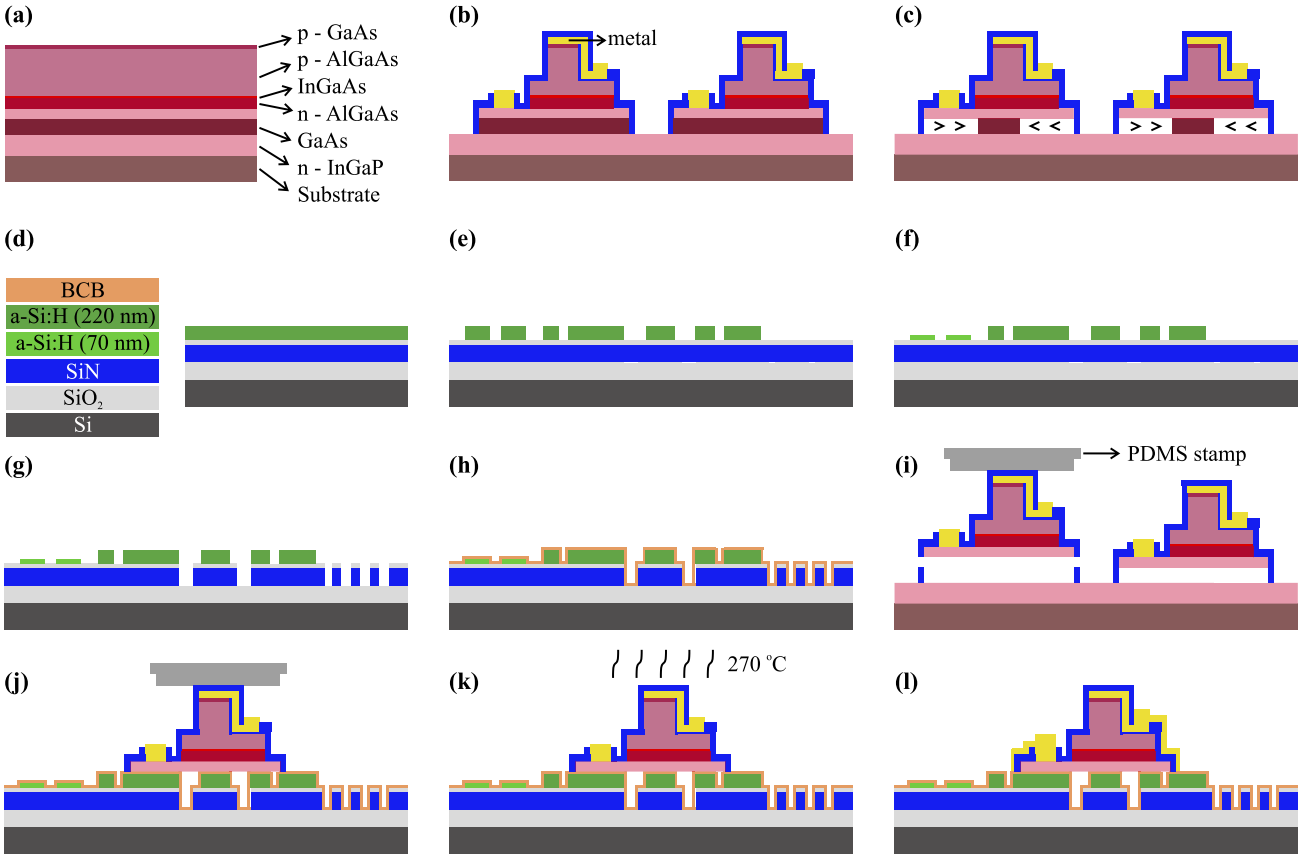


FIG. 4. Process flow for the fabrication of evanescently coupled lasers on SiN. (a) III–V epitaxial layers. (b) Device definition for MTP. (c) Underetching. (d) Target wafer with 220 nm PECVD a-Si:H on 80 nm SiO_2, overlying 300 nm LPCVD SiN, and a bottom cladding of 2.9 μm thermal oxide. (e) Patterning of 220 nm thick a-Si:H layer. (f) Partial etching for the definition of 70 nm thick a-Si:H waveguides. (g) Patterning of SiN. (h) Spin-coating of adhesive BCB. (i) Picking of device from the source. (j) Printing of device on the target. (k) BCB curing at 270 °C. (l) Metallization for electrical contacts.

circuitry is fabricated. With the laser cavity complete, a 40 nm thick adhesive layer of BCB diluted in mesitylene at a 1:9 ratio is spin-coated, followed by baking at 150 °C for 15 min. Afterward, MTP is performed using an X-Celeprint MTP-100 tool, which provides an alignment accuracy of ±1 μm (3σ) for single-device placement and ±1.5 μm for printed arrays. Alignment is achieved using two pairs of alignment markers located on both the target and the device on each side of the interface, as shown for one side in Fig. 3(c). Each amplifier measures 1380 × 50 μm^2, for which a PDMS stamp featuring a single post of dimensions 1500 × 50 μm^2 is used. The stamp is laminated onto the coupon surface, followed by a rapid upward acceleration that enhances the interfacial adhesion, causing the tethers to break at their mechanically weakest points. Printing is carried out with the target substrate heated to 80 °C to promote adhesion to the BCB bonding layer. Due to the smoothness of the backside of the coupon, even a BCB thickness as low as 15 nm is sufficient to ensure successful attachment. Once integration is complete, the BCB is cured at 270 °C for 2 h to achieve full cross-linking. Finally, metal contact pads consisting of 40 nm sputtered Ti followed by 1 μm of thermally evaporated Au are deposited to facilitate electrical connections.

In summary, although the fabrication of the evanescently coupled lasers involves multiple steps for the preparation of the target, the process relies entirely on standard techniques and avoids critically scaled dimensions, with minimum feature sizes maintained above 120 nm. Sensitivity studies (shown in the supplementary material) indicate that the dominant performance parameter is the thickness of the initially deposited 220 nm thick a-Si:H layer. Large negative variations can degrade performance by a few dB, whereas positive deviations are better tolerated. By exploiting this asymmetry and targeting slightly thicker nominal layers, together with the fact that layer thickness can typically be controlled to within ~5% through appropriate process tuning, the associated performance degradation can be kept limited. Therefore, even though good reliability and only minor device-to-device variations are observed at the sample scale, where many key fabrication steps are monitored, a similar level of robustness is expected to be maintained upon scaling to wafer-level fabrication.

IV. CHARACTERIZATION

To validate the simulated results, identical SiN waveguides with an increasing number of transitions are fabricated. As a single transition, we define the transition from the SiN waveguide to the broadened 220 nm thick a-Si:H and back. Light is coupled into and out of the chip using grating couplers with air cladding, which exhibit an insertion loss of ~14 dB per coupler at a wavelength of 970 nm. The propagation losses of single-mode SiN waveguides are characterized using the cutback method, yielding a value of ~2 dB/cm at a wavelength of 970 nm. The measured loss per transition, which inherently includes both propagation and coupling losses, is extracted from these measurements. The results, shown in Fig. 5, demonstrate a simulated loss of 0.72 dB/transition and a measured loss of 1.39 ± 0.08 dB per transition. Here, the ±0.08 dB margin represents the standard error of the slope. This discrepancy between the simulated baseline and the measured 1.39 dB/transition loss is attributed to roughness-induced scattering losses and other processing variations and can be minimized by further optimization of the fabrication process.

To evaluate the potential of the proposed coupling scheme, both amplifiers and lasers are fabricated and measured [Fig. 6(a)]. The sample is placed on a temperature-controlled stage maintained at 20 °C. Light is collected from the output grating coupler in the SiN layer, which is connected to the device output, using a single-mode fiber. The collected signal is then split, with one path sent to a power meter and the other to an optical spectrum analyzer. As a first step, we measure the wavelength-dependent gain of the amplifier for different driving currents using a commercial tunable laser (Toptica CTL 950). The optical power coupled into the waveguide prior to the amplifier was set to −24 dBm to ensure operation within the linear regime and to capture the unsaturated small-signal gain. Figure 6(b) shows the output spectra of the amplifier driven at 60 mA, recorded with a resolution of 100 pm. The input signal is swept from 950 to 990 nm in steps of 2.5 nm, revealing a narrow amplified signal superimposed on a broad amplified spontaneous emission background centered at 970 nm. For comparison, the spectra obtained from a reference waveguide are also included in the plot.

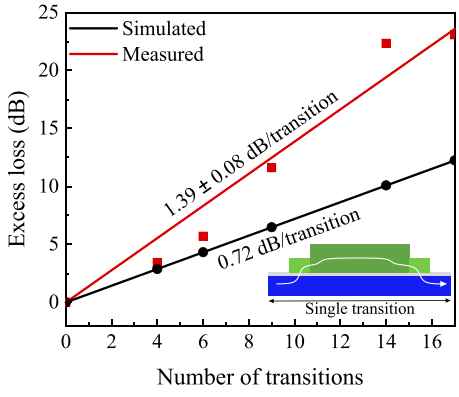


FIG. 5. Simulated and measured excess loss at a wavelength of 970 nm for an increasing number of identical transitions from 300 nm thick SiN to 220 nm thick a-Si:H and back.

The wavelength-dependent gain is shown in Fig. 6(c). A maximum on-chip optical gain of 13 dB is obtained at a driving current of 60 mA and a wavelength of 972.5 nm. When the current is reduced to 30 mA, the gain peak shifts to 975 nm. The observed wavelength shift and the asymmetric gain profile are likely due to a combination of factors: a spectral mismatch between the intrinsic gain spectrum of the standalone amplifier and the wavelength-dependent coupling efficiency of the SiN/a-Si:H/III–V transition sections, as well as thermal effects that induce temperature-dependent refractive index changes in the waveguide stack, slightly shifting the phase-matching conditions, and thereby further influencing the overall gain profile. A local pronounced drop in the measured gain is observed around 960 nm, where the gain decreases by ~4 dB compared to adjacent wavelengths. This feature is primarily attributed to the reference waveguide's grating coupler, which exhibits an anomalous peak at 960 nm, likely caused by particles or other fabrication-related variations. Such behavior was not observed in other, nominally identical, grating couplers on the same chip. This artifact is also visible in the spectra shown in Fig. 6(b).

Following the successful demonstration of gain, an identical amplifier is micro-transfer printed onto a Fabry–Pérot laser cavity. The cavity comprises a high-reflectivity Sagnac loop mirror formed using a 1 × 2 multimode interference (MMI) coupler at one end, and a partially reflective output mirror at the other, implemented with a 2 × 2 MMI coupler, which extracts about 18% of the power in the cavity. The laser is characterized by measuring both the optical output power and emission spectra as a function of driving current. After accounting for the insertion loss of the output grating coupler, the LIV (Light–Current–Voltage) characteristics are presented in Fig. 6(d).

When the device is first biased, lasing occurs at 30 mA, with the optical power rapidly saturating at 0.3 mW around 60 mA. This saturation is caused by thermal rollover, resulting from both the device's just above threshold high series resistance (40 Ω) and the underlying passive stack. In particular, the thick 2.9 μm bottom oxide, which acts as a thermal insulator, causes the device to heat quickly, degrading its performance. The observed high resistance is primarily due to the thin 300 nm n-type InGaP contact layer and the non-optimal contacts; future amplifier designs could lower the resistance by increasing its thickness and optimizing the fabrication process. Due to the relatively high index contrast of the interlayer [n ≈ 3.59 at 970 nm, Fig. 3(d)] relative to the n-type InGaP [n ≈ 3.21 at 970 nm, Fig. 1(b)], any localized mode mismatch introduced by a thicker n-type InGaP layer can be readily compensated through minor adjustments to the intermediate layer geometry. This design flexibility was one of the primary motivators for choosing the high index a-Si:H.

After driving the laser at high currents above 60 mA for a few minutes, a second LIV measurement was performed. In this measurement, the threshold current increased from 30 to 60 mA, and the optical power rose to 0.6 mW at 90 mA without any signs of saturation. The wall-plug efficiency (WPE) is 0.15%, and the differential resistance extracted below and above threshold is found 50 and 20 Ω, respectively. These behaviors can be attributed to two distinct mechanisms. First, at high currents, contact annealing improved the carrier injection, allowing more current to contribute to light generation and increasing the output power. Second, thermal effects caused material degradation, which raised the threshold current. In

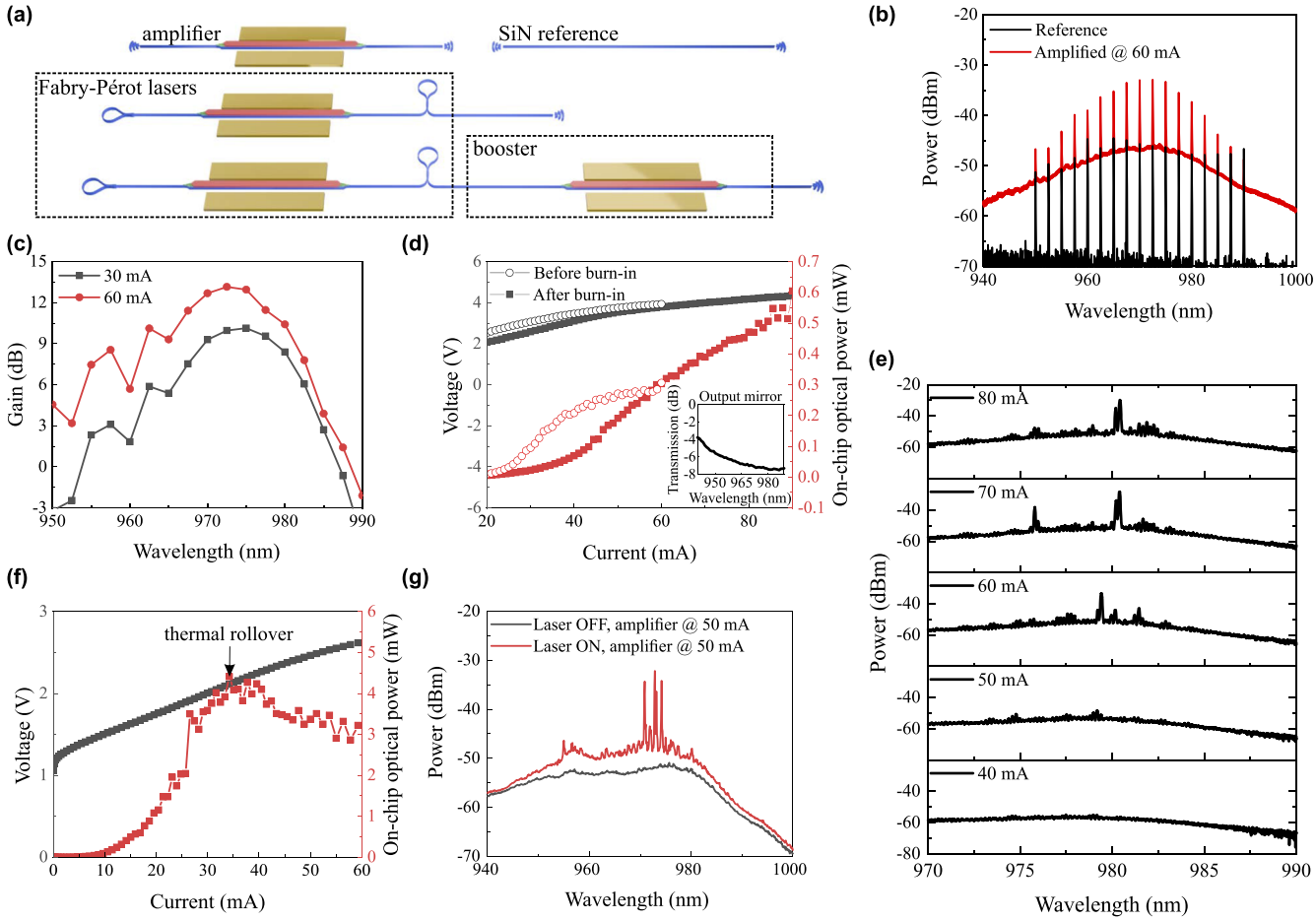


FIG. 6. (a) Schematic of the measured components, including an amplifier, a Fabry–Pérot laser, and a Fabry–Pérot laser with an integrated booster. All amplifier sections are 1.38 mm long. A reference SiN waveguide with identical grating couplers is included to assess the amplifier's gain and the lasers' on-chip optical power. (b) Measured spectra of the reference and amplifier at 60 mA, shown for different input wavelengths. (c) Wavelength-dependent-on-chip gain for two driving current levels, measured with an input power of −24 dBm. (d) On-chip optical power and voltage of the Fabry–Pérot laser as a function of the driving current before and after burn-in. The inset shows the transmission of the output mirror. (e) Laser emission spectra recorded below and above threshold, with a spectral resolution of 100 pm. (f) LIV characteristics of the integrated booster amplifier, measured with the laser section biased at 50 mA, showing an on-chip optical power exceeding 4 mW. (g) Emission spectra of the laser with integrated booster amplifier recorded with a spectral resolution of 100 pm. The amplifier is biased at 50 mA, while the laser is either inactive or co-driven at 50 mA.

both cases, a rounded threshold kink is observed, resulting from dominant amplified spontaneous emission near threshold, combined with distributed optical losses and weak feedback introduced by the evanescent coupling. Lasing spectra below and above threshold are shown in Fig. 6(e). Since no spectral filters are implemented, the laser exhibits multimode behavior. The dominant lasing peak appears around 980 nm, which can be attributed to the combined effect of the output mirror, which provides the highest reflectivity in this range, and to the wavelength-dependent transitions.

To demonstrate the versatility and potential of the integration process, a laser with an integrated booster amplifier is fabricated by transfer-printing a second amplifier stage following the Fabry–Pérot laser. With the laser biased at 50 mA, the amplifier is driven at various currents while recording the optical power and emission spectra. The corresponding LIV measurements are shown in Fig. 6(f). The on-chip optical power exceeds 4 mW at ~35 mA, but rapidly decreases beyond this point due to thermal rollover as previously discussed. The device exhibits a differential resistance of 20 Ω, with a voltage offset relative to the standalone Fabry–Pérot laser. This arises from device-to-device variability in contact processing across the III–V wafer, which resulted in pronounced variation in the electrical characteristics of the individual amplifiers. The superior contacts of the device in combination with the provided gain of the booster resulted in a lower threshold current and a significantly higher output power compared to the standalone FP laser. Figure 6(g) shows the emission spectra of the device. When both laser and amplifier are co-driven at 50 mA, strong multimode lasing is observed. In contrast, driving the amplifier alone produces only small ripples in the spectrum with no lasing, confirming that reflections from the output grating coupler are

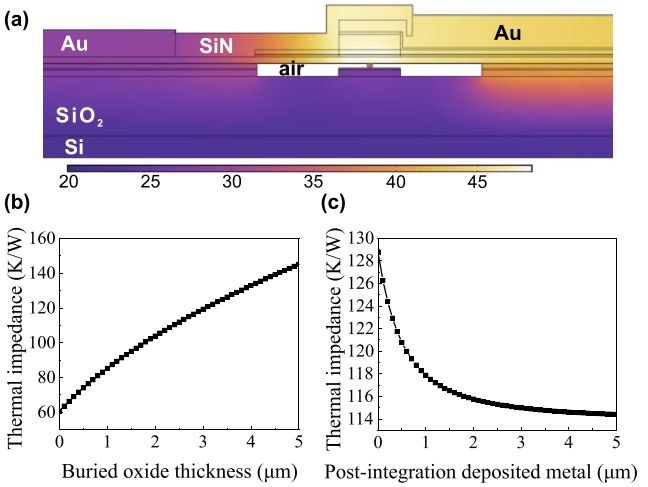


FIG. 7. (a) Cross section of the evanescently coupled GaAs-based laser and the simulated 2D-temperature distribution. At a driving current of 60 mA, the temperature reaches 48.3 °C. (b) Thermal impedance as a function of the buried oxide thickness. (c) Thermal impedance as a function of additional post-integration metallization thickness.

insufficient to form a secondary optical cavity with the laser output mirror.

To better understand the thermal effects and explain the observed thermal rollover, two-dimensional COMSOL simulations are performed. In the simulation, the heat source was concentrated in the active region and the 215 nm thick p-AlGaAs waveguide, where most of the heat is generated. In reality, heat is generated in multiple regions of the device, including the contacts and surrounding layers, due to Joule heating and non-radiative recombination. Although our simulation simplifies the spatial distribution of heat, it captures the dominant thermal behavior and provides valuable insights, as has been demonstrated in similar studies.[33]

In this simulation, we considered a 1 mm-wide and 750 μm thick silicon substrate. For the standalone Fabry–Pérot laser operating at 60 mA, the dissipated power is ~0.24 W. The corresponding volumetric heat generation rate is calculated based on the volume of the active region, which includes the quantum well and its surrounding confinement layers, and the p-AlGaAs waveguide. A fixed temperature boundary of 20 °C is applied at the bottom of the surface of the silicon substrate. The simulated temperature distribution is shown in Fig. 7(a). With our current layer stack and non-optimized electrical contacts, a temperature rise of ~28.3 °C is observed, corresponding to a thermal impedance of 118 K/W. This value is higher than that of other evanescently coupled lasers,[34,35] explaining the pronounced thermal rollover observed experimentally.

To further navigate the thermal limitations and identify practical mitigation strategies, the analysis focuses on the SiN target chip rather than on modifications to the III–V epitaxial stack. Using 2D thermal simulations, the impact of the buried oxide thickness and post-integration metallization on the thermal impedance is evaluated, with the results shown in Figs. 7(b) and 7(c), respectively. The emphasis on post-integration metallization, while keeping the pre-integrated SOA stack fixed, reflects a pragmatic approach aimed at improving thermal performance without requiring changes to the existing III–V material. As expected, reducing the thickness of the buried oxide leads to a significant reduction in thermal impedance. For instance, decreasing the oxide thickness from 2.9 to 2 μm yields an improvement of ~12%, corresponding to a thermal impedance of 104 K/W. While further oxide thinning would continue to improve thermal behavior, it would ultimately introduce optical losses due to leakage into the silicon substrate. This trade-off is intrinsic to evanescent-coupling schemes and highlights one of the key advantages of butt-coupled approaches, where the SOA can be integrated directly on silicon.[21] In contrast, the influence of post-integration metallization is small. Increasing the thickness of the deposited gold from 1 to 2 μm results in only 1.8% reduction, indicating that heat extraction is not limited by top-side metallization in the present configuration. A more substantial contribution arises from the presence of air surrounding the passive waveguide region, as illustrated in the schematic. Since air is a strong thermal insulator, performing oxide planarization prior to SOA integration, thereby eliminating air gaps, leads to a 22% reduction in thermal impedance. Taken together, without altering the original SOA design, the combined effects of oxide planarization, additional post-integration metallization, and reduced bottom oxide thickness lower the thermal impedance to ~77 K/W (35% improvement). Further improvements could be achieved through the integration of thermal management strategies such as thermal shunts or localized heat sinks. For instance, incorporating high-thermal-conductivity pathways to connect the III–V amplifier to the silicon substrate could significantly reduce the thermal impedance, thereby facilitating more efficient heat extraction.[35,36] In tandem with structural optimizations, looking ahead to the next generation of amplifiers, although the epitaxial stack may be revisited to incorporate dedicated thermal spreading layers, the primary focus will be on reducing resistance variability and achieving robust, low-resistance electrical contacts. Lower series resistance directly translates into reduced electrical power dissipation at a fixed driving current and, consequently, a lower temperature rise.

To place our results in context, Table I summarizes representative literature reports of integrated in-plane lasers operating in the submicrometre wavelength regime, comparing key metrics such as integration scheme, coupling architecture, output power, and scalability. To evaluate scalability, two primary factors are considered: process tolerance (including critical dimensions and alignment sensitivity) and integration complexity. Conventional hybrid and heterogeneous direct SiN-to–III–V butt-coupling implementations currently lead in peak output power and thermal performance. However, their scalability is heavily constrained by stringent vertical alignment tolerances and a reliance on high-quality optical facets that are susceptible to degradation, requiring complex passivation strategies. These constraints can be partially mitigated, as shown in prior demonstrations,[9,22] by employing a two-step coupling strategy with the introduction of an intermediate dielectric layer. This configuration consists of evanescent coupling between the SiN and the interlayer, followed by butt-coupling between the interlayer and the III–V. While this hybrid approach improves processing tolerances and achieves high mode-matching efficiency, the underlying sensitivity to vertical misalignment remains fundamentally more challenging than in purely evanescent approaches, and it becomes increasingly critical at shorter wavelengths. Consequently, such architectures are

TABLE I. Comparison of integrated in-plane lasers in the 780 – 1000 nm wavelength range.

Wavelength (nm)	Platform	Integration method	Coupling scheme	Laser-type	Power (mW)	Scalability	Refs.
780	SiN	Wafer bonding	Butt-coupling: III–V → interlayer Evanescent-coupling: Interlayer → SiN	Tunable	10	Moderate-high	9
785	SiN	Hybrid	Butt-coupling	Tunable	11.24	Low	37
800	SiN	MTP	Butt-coupling	FP	4	Moderate	21
976.5	SiN	Wafer bonding	Butt-coupling: III–V → interlayer Evanescent-coupling: Interlayer → SiN	Tunable	10	Moderate-high	22
980	Ta_2O_5	Wafer bonding	Evanescent-coupling	DFB	2	Moderate (100 nm CD)	38
980	SiN	MTP	Evanescent-coupling through an a-Si:H interlayer	FP	0.6 (standalone) 4 (with booster)	High	This work

characterized as having "moderate-high" scalability, reflecting a balance between improved on-chip alignment and persistent facet/vertical tolerance sensitivities. Beyond those coupling-specific constraints, pure hybrid integration schemes introduce a separate scalability limitation due to their reliance on individual chip-to-chip placement, which hinders high-throughput, wafer-scale manufacturing. In contrast, purely heterogeneous evanescent approaches provide a more robust route toward wafer-scale integration because they are primarily sensitive to less restrictive in-plane alignment tolerances. To date, however, realizations below 1 μm remain scarce, with the primary demonstration based on Ta_2O_5 requiring III–V-side critical dimensions on the order of 100 nm to achieve sufficient mode transfer, which impose stringent lithographic and etching constraints that inherently limit scalability. By comparison, our strategy employs an a-Si:H interlayer to enable efficient coupling while maintaining relaxed alignment tolerances and III–V feature sizes exceeding 300 nm. This combination supports a highly scalable integration platform suitable for large-volume manufacturing. Nevertheless, the benefits of this coupling architecture entail an important trade-off: thermal dissipation is inherently constrained by the buried oxide layer. This layer introduces a high thermal resistance that limits peak output power and efficiency, necessitating dedicated thermal management strategies. However, while the output power reported for evanescently coupled lasers in this spectral range is currently modest, this primarily reflects the early maturity of the platform. Analogous to the evolution of telecom silicon photonics, where evanescently coupled lasers progressed from milliwatt-level demonstrations to high-power standards, a similar trajectory is anticipated as the design, processing, and thermal management continue to improve.

V. OUTLOOK

To fully realize the power potential of this integration scheme, future iterations will focus on increasing the n-type contact thickness, improving contact quality to reduce parasitic series resistance, and refining the etching recipes. Beyond power scaling, achieving tunable single-mode lasing will be essential to expand the platform's functionality. While the reported power levels are currently limited, they are already compatible with a variety of applications. For example, optical coherence tomography requires sub-milliwatt output levels to avoid sample damage,[39] while low-power tunable near-infrared sources are promising for applications such as agricultural sensing and food quality monitoring.[40] Finally, efforts will be directed toward scaling the platform to 200- and 300-mm wafer lines. The inherent CMOS compatibility of a-Si:H, along with the wafer-scale capability of micro-transfer printing, makes this approach particularly well-suited for mass production. By circumventing the critical vertical alignment challenges and facet-dependency of butt-coupling, this proposed coupling strategy offers the fabrication tolerance and reliability required for large-scale photonic integrated circuits.

VI. CONCLUSION

In conclusion, we demonstrate a CMOS-compatible approach for the development of evanescently coupled lasers emitting in the submicrometre wavelength range. By employing an a-Si:H taper structure with two etch depths, the mode can transition from the SiN waveguide to the integrated III–V amplifier with a simulated maximum transmission of approximately −0.84 dB. Moreover, we

validate this approach by transfer-printing an amplifier on top of the a-Si:H waveguides. We demonstrate both on-chip optical gain of 13 dB at 972 nm as well as multimode lasing with an on-chip optical power of 0.6 mW. Finally, to showcase the versatility of this integration scheme, we transfer-print a second amplifier stage after the Fabry–Perot laser, and we measure more than 4 mW power on chip.

SUPPLEMENTARY MATERIAL

See the supplementary material for a detailed sensitivity analysis of the impact of processing variations during the deposition and etching of the a-Si:H interlayer.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

K. Akritidis: Conceptualization (equal); Formal analysis (lead); Investigation (lead); Methodology (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (lead) **M. Billet**: Methodology (supporting); Supervision (supporting); Writing – review & editing (supporting). **M. Kiewiet**: Methodology (supporting); Writing – review & editing (supporting). **J.-P. Koester**: Investigation (supporting); Methodology (supporting); Writing – review & editing (supporting). **J. Fricke**: Investigation (supporting); Methodology (supporting); Writing – review & editing (supporting). **P. Della Casa**: Investigation (supporting); Methodology (supporting). **H. Wenzel**: Investigation (supporting); Methodology (supporting). **J. Brouckaert**: Supervision (supporting); Writing – review & editing (supporting). **R. Jansen**: Supervision (supporting); Writing – review & editing (supporting). **G. Roelkens**: Conceptualization (supporting); Methodology (supporting); Writing – review & editing (supporting). **M. Weyers**: Conceptualization (supporting); Supervision (supporting); Writing – review & editing (supporting). **P. Van Dorpe**: Conceptualization (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal). **B. Kuyken**: Conceptualization (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal); .

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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