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TOPICAL REVIEW

Challenges and Opportunities in D-Band Transmitter Architectures and Antenna Design, Integration, and Scalability for 6G Communications: A Brief Review

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ABSTRACT This article reviews the current state-of-the-art (SOTA) key enabling technologies that pave the way for the advancement of scalable 6G antenna array systems for future communications. The focus is on the development of transmitter building blocks, considering the implementation of size, weight, area, and power (SWaP) constrained nodes. First, an overview of communication technologies from 1G to 6G is presented, followed by a discussion of key performance indicators and link budget analysis. To provide further insights into *D*-band (110-170 GHz) system design challenges, this review highlights the significance of 1) high-gain and high-linearity power amplifiers, 2) spectrally pure local oscillator (LO) signal sources, 3) high data rate modulator architectures, 4) scalable antenna array development, and 5) heterogeneous integration approaches. Furthermore, this article presents ongoing research and development on transmitter building blocks across various device fabrication technologies such as CMOS, BiCMOS, and III-V semiconductors. Special attention is given to the high data rate modulator architectures, which comprise 1) heterodyne, 2) homodyne, and 3) direct-digital modulators, followed by addressing the implementation challenges and opportunities in coherent and noncoherent modulation schemes within the context of SWaP-constrained scalable arrays for *D*-band. Additionally, this article reviews heterogeneous integration (HI) while focusing on chiplet designs for multifunctionality, low-loss packaging trends with thermal management solutions, chip-antenna interconnects featuring novel antenna technologies, and bottlenecks in mmWave/sub-THz measurements.

INDEX TERMS Power amplifier, frequency multiplier, direct-digital modulators, scalable antenna arrays, heterogeneous integrations, SWaP, 6G communication, D-band, mmWave and Sub-THz transmitter.

I. INTRODUCTION

Over the past four decades, each decade has brought technological advancements in wireless communications. From the first generation (1G) to the sixth generation (6G), it empowers people with more ingenuity. As shown in Fig. 1, the journey started with the first cellular network in the 1980s (1G), which later opened the door for digital communication and paved the way for data services along with voice communication by using the global system for mobile (GSM), (2G). In the early

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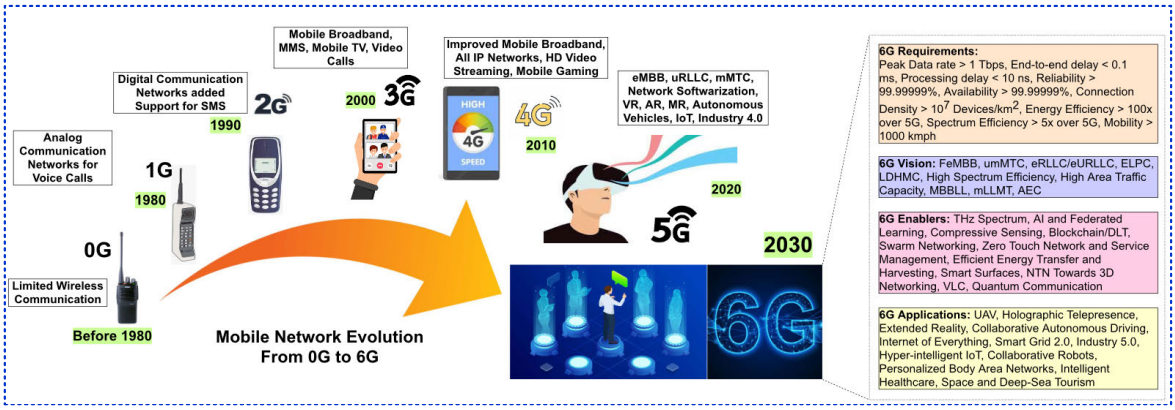


FIGURE 1. Evolution of wireless communication technologies from 1G to 6G with their respective applications [1].

2000s, code division multiple access (CDMA) technology transformed communication by offering data rates within the megabytes/second range, supporting video calls, messaging, and mobile television. This was followed by long-term evolution (LTE) technology or 4G in the early 2010s with enabling features such as voice-over-IP, HD video streaming, and online gaming by using multi-input multi-output (MIMO) and orthogonal frequency division multiplexing (OFDM) techniques. The advent of fifth-generation communication (5G) spurred application-driven networks to explore wider bandwidths, leading to enhanced data rates up to 10 Gb/s and latency as low as 1 ms by using 28 GHz, 39 GHz, 60 GHz, and 77 GHz frequency spectrums.

However, the number of connected devices and the need for greater amounts of data are growing exponentially (10^7 devices/km^2), necessitating the acceleration of technical developments in a new frequency spectrum, that is the sub-THz (95-300 GHz) band. Using these frequencies, 6G aims to deliver mobile ultra-broadband (uMUB), ultrahigh-speed-with-low-latency communication (uHSLLC) with data rates greater than 100 Gb/s and latencies as low as 0.1 ms, and ultra-high-data-density (uHDD) classes of communication that can support up to 100 million devices/km^2 [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12].

Fig. 2 compares the key performance indicators (KPIs) of various wireless communication generations up to 6G. The analysis shows that 6G is pushing the frontiers of application-based communication to new heights by significantly enhancing each KPI. For instance, the targeted data rates for 6G are 10x more than the 5G with 3x better spectral efficiency, and the aim is to support 10x more devices per square kilometer with significantly reduced latency of between 0.01 to 0.1 ms. Additionally, 6G is targeting circuits with 10x greater energy efficiency than the previous 5G, which is essential for scalability [3], [4], [5], [11], [13]. Such stringent requirements require innovative solutions to all hardware, software, and system design aspects.

Fig. 3 shows the potential applications of the sub-THz spectrum, driven by (i) operating frequency, (ii) throughput,

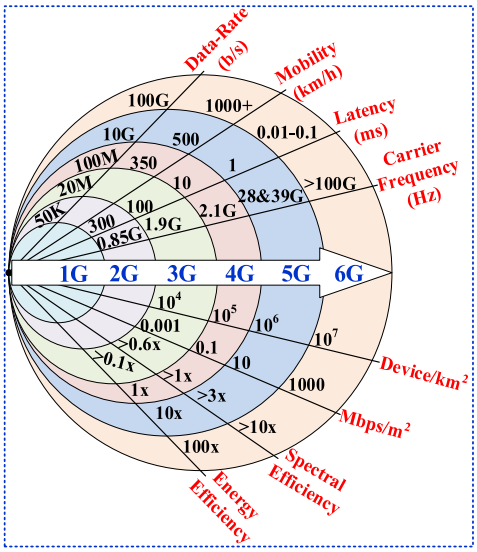


FIGURE 2. Comparison of the key performance indicators (KPIs) for different wireless communication generations [13].

(iii) coverage, and (iv) energy efficiency, including drone-based sensing, vehicle-to-vehicle communication, and high data rate coverage for urban areas, which enables high-frequency micro-cells with consumer virtual-reality oriented services [14]. Fig. 3 also depicts a system-level distributed architecture that enables potential 6G applications. This architecture offers (a) higher signal gain, (b) better reliability, (c) area and power scalability, and (d) adaptability, spatial diversity, and other features needed to realize scalable 6G communication systems [15].

In this context, wireless communication history, characteristics, and targeted KPIs are discussed. In addition, potential applications and system-level architectures have been presented. However, the focus is more on the challenges, opportunities, and SOTA developments in the design and implementation of circuits for *D*-band radios. Achieving 6G KPIs necessitates innovative, compact, energy-efficient, and

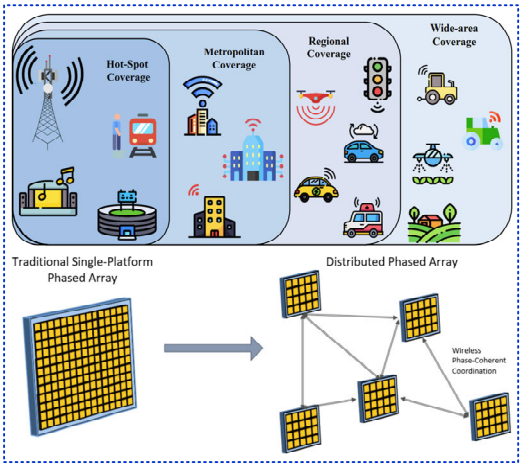


FIGURE 3. Application-oriented networks along with conceptual distributed phased array architecture [14], [15].

scalable building blocks at the circuit level. Section II analyzes the link budget for high data rate *D*-band transceivers, and Section III discusses the open research bottlenecks in circuit design. Section IV addresses the significance and limitations of semiconductor device fabrication technologies and reviews SOTA transmitter components such as (a) high-power, high-gain, and high-linearity amplifiers, (b) spectrally pure and low-phase noise local oscillator signal sources, (c) less-complex, energy-efficient, and high-data-rate (up to 100 Gb/s) modulators, Section V illustrates wide-band, radiation-efficient, and scalable antenna arrays with low-loss integration techniques. Section VI discusses heterogeneous integration, and Section VII describes the mmWave/sub-THz measurements. Section VIII concludes this review with challenges and opportunities in SOTA *D*-band transmitter components/circuits, antenna array, and packaging designs for 6G scalable systems.

II. LINK BUDGET ANALYSIS FOR HIGH DATA RATE TRANSCEIVER

As mentioned earlier, a link budget analysis has been performed to quantify the requirements of a *D*-band transceiver for 6G wireless communications. Both the noncoherent and coherent modulation schemes are evaluated. The latter 8-QAM: 3 bits/symbol) offers a greater spectral efficiency than the former (OOK: 1 bit/symbol). Fig. 4(a) depicts the energy per bit (E_b) to noise spectral density (N_o) ratio plotted against the bit-error rate (*BER*) for various modulation schemes [16]. The E_b/N_o ratio in digital modulation schemes is related to the required signal-to-noise ratio (SNR_{dB}) as follows:

$$SNR_{dB} = \left(\frac{E_b}{N_o}\right)\left(\frac{f_b}{BW}\right) \tag{1}$$

Where f_b is the required bandwidth (*BW*). However, the noncoherent modulation scheme uses $1xf_b$, while the coherent modulation scheme uses $f_b/3$. As a result, OOK modulation necessitates an SNR_{dB} of 17 dB, whereas 8-QAM requires 42 dB to efficiently decode the digitally modulated information with an error-free communication at a *BER* of 10^{-12}. Moreover, the SNR_{dB} requirement is translated into a radio frequency system design by employing equation (2):

$$SNR_{dB} = P_R - \left(N_o + 10log_{10}\left(B\right) + NF\right) \tag{2}$$

Where P_R is the receiver output power, N_o is the noise spectral density, B is the system noise bandwidth, and NF is the receiver noise figure. Equation (2) shows the stringent requirements for wideband systems. Similarly, the noise added by the receiver (NF) must also be minimized to achieve an acceptable SNR_{dB} for error-free communication over a given link distance. Furthermore, the P_R can be further extended by equation (3) as follows:

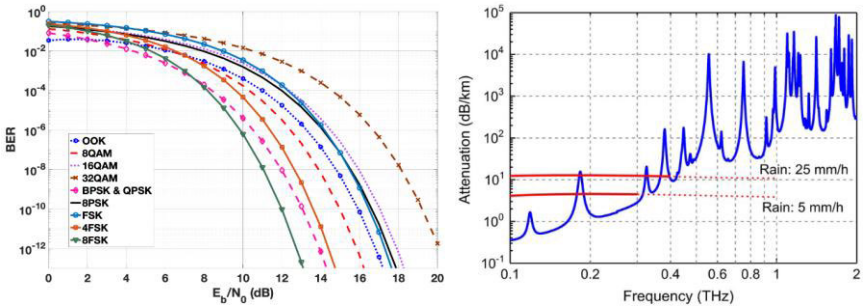
$$P_R = P_{sat} + G_{T,ant} - 2L_P - PL + G_{R,ant} + G_R - (\propto_a (f)) \tag{3}$$

Here, P_R is a function of transmitter saturated power (P_{sat}), path loss (PL), atmospheric attenuation ($\propto_a (f)$), as shown in Fig. 4(b), transmit ($G_{T,ant}$) and receive ($G_{R,ant}$) antenna array gains, respectively, receiver gain (G_R) and packaging interconnect losses (L_P). These parameters can degrade the power received and consequently, the *BER*. Furthermore, P_{sat} is a key performance metric, which determines the effective isotropic radiated power (*EIRP*) of the transmitter, for this review, it is given by equation (4):

$$EIRP = P_T + G_{T,ant} + 10log_{10}\left(N_{T,ant}\right) \tag{4}$$

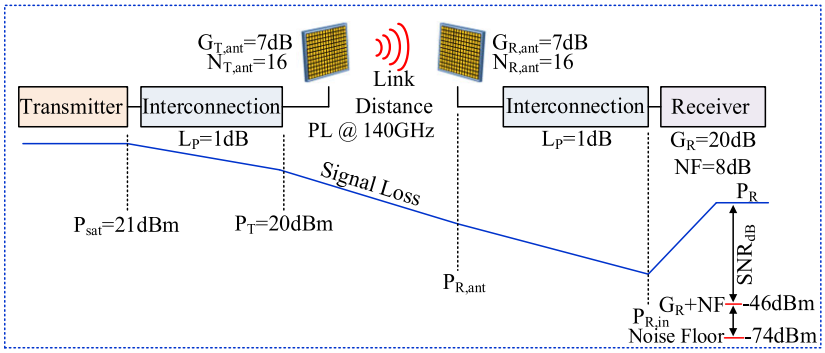
Here, $P_T = P_{sat} - L_P$ corresponds to the maximum transmitted power, and $N_{T,ant}$ denotes the total number of antenna elements in an array. By leveraging a free space wavelength (λ) of 2.2 mm at 140 GHz, multiple $\lambda/2$-spaced radiators can form an antenna array, enhancing the *EIRP* but requiring scalability in both area and power consumption.

Fig. 5 illustrates the wireless link budget of the transceiver, essential design parameters, and incorporation of low to mid-complex modulation schemes. The figure represents each component, including the transmitter, receiver, packaging/interconnects, and antenna array, based on equations (1) to (4) at 140 GHz. Consequently, (a) the modulation scheme, (b) transmitter P_{sat}, (c) interconnect losses define P_T, and (d) G_R and NF play crucial roles in defining the wireless link quality ($SNR_{dB} \rightarrow BER$). Building on this link budget analysis, the article reviews SOTA in *D*-band transmitter building blocks, focusing on achieving high *EIRP*, high data rates, and heterogeneous integration. It is worth noting that the design parameters in the 6G wireless communication link budget, which uses digital/analog domain modulation schemes having variable spectral efficiencies, can be achieved with the circuits designed in existing (silicon/III-V/fused-silica) technologies.



(a) (b)

FIGURE 4. (a) E_b/N_o requirement for bit-error-rate (BER) estimation for various modulation schemes [16], (b) Atmospheric attenuation for mmWave and THz frequency spectrums [12].



Parameter	OOK	8-QAM
Bandwidth	f_b	$f_b/3$
Spectral Density Bit/symbol	1	3
E_b/N_0 for BER=10^{-12}	17	14
SNR_{dB}	17	42
Link Distance (m)	10	1
Path Loss (dB)	95	75
Signal Loss (dB)	63	43
$P_{R,ant}$ (dBm)	-43	-23
$P_{R,in}$ (dBm)	-44	-24
P_R (dBm)	-24	-4

FIGURE 5. Illustration of link budget for D-band wireless transceiver with link distances of 10 m for OOK/ASK and 1 m for 8-QAM modulation schemes.

III. RESEARCH BOTTLENECKS IN D-BAND, HIGH DATA RATE COMMUNICATION SYSTEMS

This section briefly discusses the top-level research challenges that built on the quantitative analysis presented in section II.

A. WIDEBAND DESIGN

According to the Shannon-Hartley theorem, the wireless channel capacity increases with the bandwidth. However, increasing the bandwidth is not straightforward for both passive and active circuits because wireless channels require acceptable performance over a wide frequency range with (i) high-power, high-gain, high-linearity, and low error-vector magnitude (*EVM*) transmitters, (ii) high-gain, high sensitivity, and low *BER* receivers. Additionally, from equations (2) and (3), SNR_{dB} requirements are stringent for wideband systems owing to the rise of in-band noise sources, such as thermal, flicker and shot noises. It degrades the wireless channel performance, which includes (a) link distance and (b) throughput [8], [108], [109].

B. HIGH CARRIER FREQUENCY

Among many limitations of high carrier frequencies (f_c) above 100 GHz, atmospheric attenuation is particularly significant, as shown in Fig. 4(b). While the sub-THz spectrum offers viable communication for indoor environments, outdoor applications are prone to weather conditions such as rain and fog, requiring special consideration [12]. The current solution for mitigating environmental challenges in outdoor settings relies on achieving a high *EIRP*.

C. HIGH-POWER, HIGH-GAIN, AND HIGH-LINEARITY TRANSMITTER

In a wireless communication link, P_{sat} and linearity are linked with power amplifiers, especially the one used as the last gain stage of the transmitter. Therefore, high gain, power, and linearity play a crucial role in defining the quality of wireless links. However, owing to the increase in carrier frequency (f_c >100 GHz), it is challenging to contend with the technological processing limitations related to the transition frequency (f_T) and maximum oscillation frequency (f_{max}) of the active devices and transistors required to obtain high power and linearity [8], [13].

For instance, to reach P_{sat} > 10 dBm, it is suggested that f_c be $f_{max}/3$ to $f_{max}/2$ [8], [62], which is achievable with currently available (compound) semiconductor technologies.

D. HIGH-DATA-RATE MODULATORS

Higher data rates can be achieved by (a) increasing f_c or (b) using higher-order modulation schemes. The former necessitates wide RF bandwidth (>20 GHz). It enables higher data rates by using basic analog-domain modulation schemes, such as on-off keying (OOK), binary-phase shift keying

(BPSK), and quadrature-phase shift keying (QPSK). While the latter uses complex digital-domain modulation schemes such as 2048-QAM and 4096-QAM. To realize 100 Gb/s data rate, analog-domain modulation requires a bandwidth of ∼100 GHz [8]. As a result, a transceiver is needed to maintain the performance over 100 GHz+ bandwidth, which is extremely challenging with in-band noises and distortions. Instead, digital-domain modulation does not require wide bandwidth. Instead, it introduces circuit complications. Also, the modulation performed in the digital domain requires a high peak-to-average-power ratio (*PAPR*) and dynamic range (i.e., transmitter linearity and receiver sensitivity) for efficient data processing [13], [62], [109]. Other shortcomings of this approach include (i) high-resolution ADC/DACs and (ii) low phase-noise LO.

E. HIGH EFFICIENCY, WIDE BAND ANTENNA, AND CHIP-ANTENNA INTEGRATION

High power generation is essential, however, a wide-band, radiation-efficient antenna is equally important in retaining the signal integrity between transmitter and receiver [114]. By leveraging the shorter wavelengths in the sub-THz spectrum, radiators can be designed on-chip. Nonetheless, Antenna-on-Chip (AoC) offers low radiation efficiencies and narrow bandwidths owing to the high permittivity (∼11) and available thicknesses (∼ μm) of the silicon substrates [76], [77]. As an alternative, off-chip antennas have gained attention because of their reduced permittivity, tolerable substrate thicknesses, and low fabrication costs using standard printed circuit board (PCB) processes, thus forming an antenna-on-board (AoB) technique [80], [81]. To further improve radiation efficiency, the antenna-in-package (AiP) technique has been introduced. It mounts discretely fabricated antennas and chips on the same substrate/package, thus reducing interconnection losses and improving overall radiation efficiency [86], [87].

F. MULTI-ANTENNA ARRAY FOR HIGH EIRP

To improve the receiver SNR_{dB} performance and mitigate atmospheric attenuation, a multiple antenna-elements array is essential in creating a high *EIRP* for improved wireless link quality. These arrays achieve spatial power combining through the constructive interference of emitted power from radiators positioned a half-wavelength apart. As given in equation (4), the transmit power (P_T) is enhanced by $10\log_{10}(N_{T,ant})$, where $N_{T,ant}$ corresponds to the number of antennas in the transmitter array. Similarly, the improvement in the minimum detectable signal at the receiver is $10\log_{10}(N_{R,ant})$, where $N_{R,ant}$ is the number of receiver antennas in the antenna array.

G. HETEROGENEOUSLY INTEGRATED PACKAGING DESIGN

Sub-THz wireless communication links demand large arrays with multiple channels to enhance the *EIRP*. The signal routing to each channel in an array architecture introduces insertion losses and complicates the distribution of LO and control signals. Simultaneously, it increases the I/O interconnection density. The redistribution layer (RDL) and embedded wafer-level ball-grid arrays (eWLB) approaches have been adopted to address this issue. Similarly, the excessive heat generated due to multiple active circuitries (e.g., power amplifiers) necessitates thermal management. Hence, by leveraging the new packaging materials, such as Si-interposers and fused silica, a highly efficient antenna, low-loss RDL, and thermally efficient heterogeneously integrated packaging can be realized for sub-THz radios [95], [98], [100].

IV. DEVICE FABRICATION TECHNOLOGIES AND SOTA IN TRANSMITTER ACTIVE COMPONENTS DESIGN

As mentioned before, it is essential to evaluate the capabilities of semiconductor device fabrication technologies while advancing the sub-THz circuit design. The maximum oscillation frequency (f_{max}) and transit frequency (f_T) are the key metrics that drive the operational frequencies of the circuits developed in a particular processing node. The former (f_{max}) is the frequency where unilateral gain becomes unity, while the latter (f_T) refers to the frequency where current gain (h_{21}, with short-circuited output) equals unity. Fig. 6 depicts the f_T vs f_{max} across diverse technologies [6] such as CMOS (Bulk, FinFET, FD-SOI), BiCMOS (SiGe HBT), and III-V (GaN, InP) with their respective processing nodes, ranging from 14 nm [FinFET] upto 300 nm [InP]. The f_T and f_{max} for HBTs and FETs can be calculated by the below equations (5) to (8):

$$f_{T,HBT} = \frac{g_m}{2\pi\,(C_{BE} + C_{BC})} \tag{5}$$

$$f_{T,FET} = \frac{g_m}{2\pi\,(C_{GS} + C_{GD})} \tag{6}$$

$$f_{max,HBT} = \sqrt{\frac{f_{T,HBT}}{8\pi C_{BC} r_B}} \tag{7}$$

$$f_{max,FET} = \sqrt{\frac{f_{T,FET}}{8\pi C_{GD} R_G}} \tag{8}$$

Here, g_m refers to the transconductance, which indicates the device's effectiveness in converting an applied voltage into an output current. Also, $C_{BE,BC}$ indicate the base-emitter and base-collector capacitances, respectively, while r_B corresponds to the internal base resistance of HBTs. Likewise, $C_{GS,GD}$ show gate-source and gate-drain capacitances, respectively, whereas R_G represents the gate resistance of FETs. The capacitances above are insignificant at low frequencies. However, in the sub-THz band, r_B/R_G and metal wiring create a low-pass filtering effect, which significantly decreases the device gain [6], [17]. Thus, a high f_T and smaller $C_{BC,GD}$ are desirable for higher power/gains in the sub-THz spectrum.

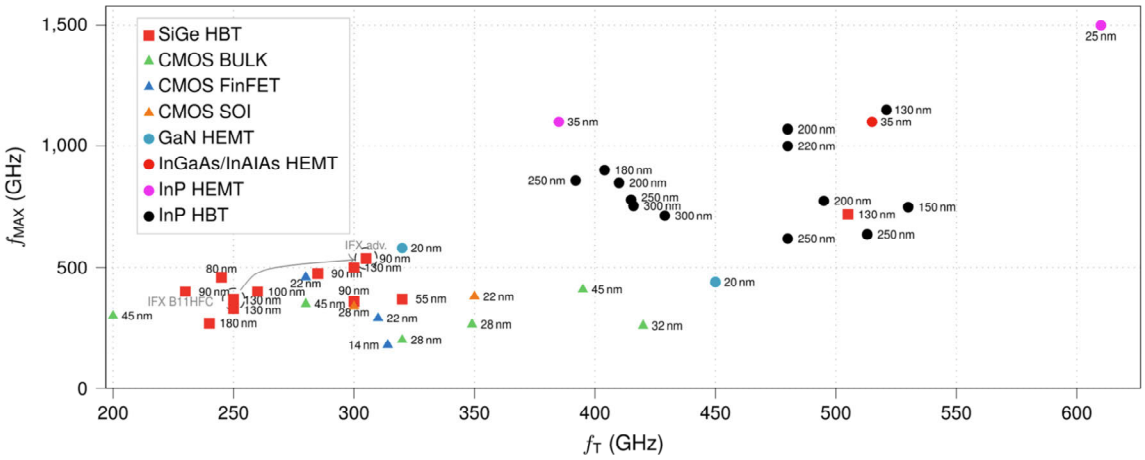


FIGURE 6. Comprehensive illustration of f_t vs f_{max} for various semiconductor fabrication technologies with their diverse process nodes [6].

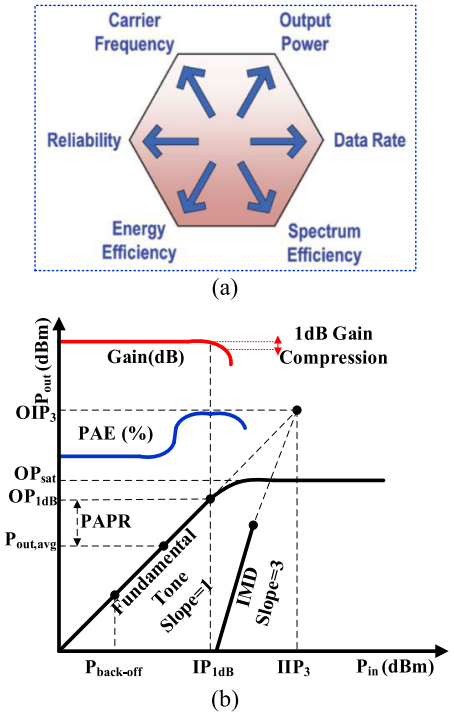


FIGURE 7. (a) Sub-THz power amplifier performance parameters hexagon [18], (b) Overview of power amplifier design specifications.

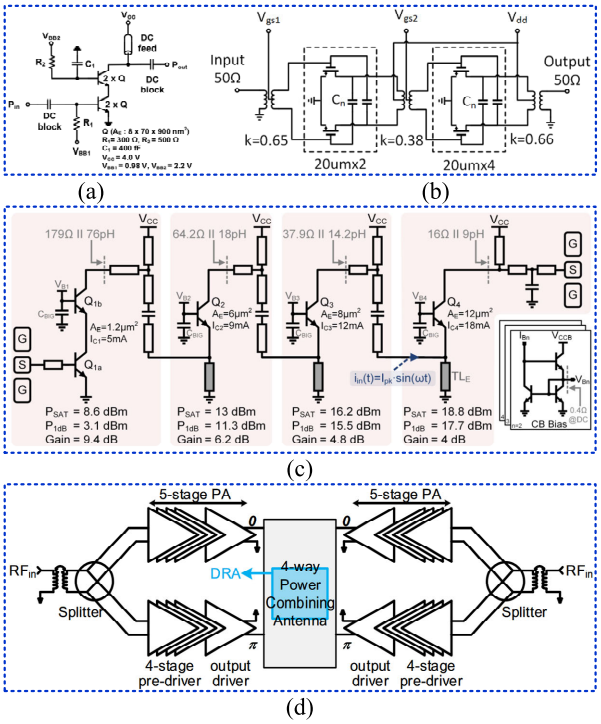


FIGURE 8. (a) Cascode/Stacked CE+CB [20], (b) Balanced CS transistors with neutralization capacitor (C_n) [25], and (c) Cascode first stage with cascade later stages include CE and CB transistors for high-gain and P_{sat} [27], (d) Spatial power combining to improve EIRP [24].

A. HIGH-GAIN, HIGH-LINEARITY POWER AMPLIFIER

The power amplifier (*PA*) is an essential building block for transmitter design. The *PA*s must perform with greater P_{sat}, and linearity to maintain the required SNR_{dB} for the desired modulation scheme. Fig. 7(a) depicts the hexagon with the trade-offs for the sub-THz *PA* design. To discuss the complexity of these trade-offs, the carrier frequency (f_c), P_{sat}, and power-added efficiency (*PAE*) will be addressed. The benefits of high f_c are offset by the degradation of P_{sat} due to f_T/f_{max} of transistor technology, which negatively impacts *PAE*. While increasing the number of gain stages can compensate for the effect of P_{sat}, though degrades the *PAE* owing to the high DC power consumption. It is worth noting that power amplifiers have a greater *PAE* at P_{sat} than at $P_{back-off}$, as shown in Fig. 7(b). However, the *PAE*s at both P_{sat} and $P_{back-off}$ points are designed to be as substantial as possible for the overall energy efficiency.

Common transistor topologies in *PA* design include (a) cascode or stacked common emitter (CE) + common base (CB)

transistors, (b) balanced CE transistors with neutralization capacitor (C_n) at the base-collector junction, and (c) CE and CB cascaded transistor stages, Fig. 8(a)-(d).

The cascode/stacked topology improves the gain-bandwidth product by mitigating the Miller effects [19]. This topology is also implemented in [20], [21], [22], and [23] to provide wide BW_{3dB} of 27 GHz, 40 GHz, 30 GHz, and 80 GHz and higher gains of 23.6 dB, 30.7 dB, 34 dB, and 19 dB, respectively. Balanced transistors have been extensively used with C_n in [19], [22], [24], [25], and [26] to reduce Miller effects created by C_{BC} or C_{GD} parasitic capacitances to obtain a higher gain and stability at sub-THz frequencies.

In the latter technique (with C_n), the first stage is optimized for maximizing the gain, while the later stages are used to improve linearity, as shown in Fig. 8(c). Consequently, CB stages are employed, which increase linearity owing to the inherent emitter degeneration effect. This technique has been demonstrated in [27], [28], [29], and [30] to achieve P_{1dB} of 18.5 dBm, 20.2 dBm, and 14.4 dBm, respectively. These techniques are based on transistor orientations (CB, CE, Cascode, Cascade, and balanced transistors). To further improve the saturated output power and augment the *EIRP*, power combining mechanisms can be used by implementing on-chip power combiners, T-junction, Wilkinson power divider/combiner [115], [116], Marchand balun, and sub-quarter wavelength balun. In addition, the saturated output power of the amplifier can be spatially combined using antenna arrays, as shown in Fig. 8(d).

The specifications of the SOTA power amplifiers in *D*-band using different semiconductor technologies are shown in Fig. 9. Of the bulk CMOS [31], [32], [33] technologies, FD-SOIs provide the highest P_{sat} with a reasonable *PAE* of 16.5%, whereas FinFETs exhibit the highest *PAE* of 22.6%. Furthermore, BiCMOS SiGe [34] offers a maximum P_{sat} of 22 dBm with a *PAE* of only 3.6%. The maximum reported *PAE* in SiGe was 13.8%, with a P_{sat} of 18 dBm. In contrast, III-V [35], [36], and [37] semiconductors provide the highest P_{sat} of 24 dBm among all available technologies with a *PAE* of 7%. The maximum reported *PAE* for III-V technologies is 32% with a P_{sat} of 15.3 dBm. The *PAE* at P_{sat} trend shows that BiCMOS and III-V technologies are well suited for 100-200 GHz power amplifier designs.

Fig. 9(a)-(c) summarizes the *PAE* at P_{sat}, *PAE* at $P_{back-off}$, and figure-of-merit (FOM_1) performance metrics for the SOTA 100-200 GHz *PAs*. The former (*PAE* at P_{sat}) represents the power-delivering capabilities of a *PA*, while the latter (*PAE* at $P_{back-off}$) represents the linearity of the *PA*. Although III-V *PAs* can deliver more power with high linearity, BiCMOS offers optimum performance in the 130-180 GHz frequency range. *PAs* have also been implemented in multi-stage configurations using passive combiner networks for gain boosting. FOM_1 is $P_{sat}/Area$ and shows the area efficiency with higher desired values. Except for the 16 nm FinFET technology (>500), the other *PAs* are clustered below an FOM_1 of 100.

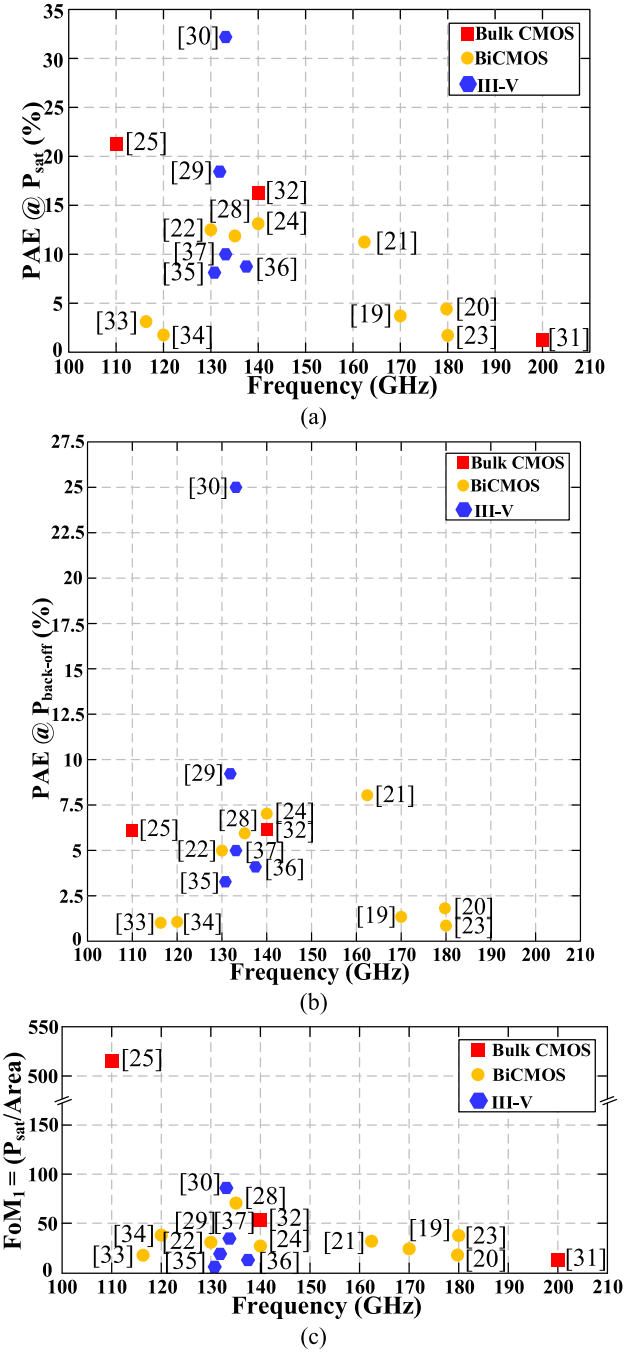


FIGURE 9. Frequency vs (a) PAE at P_{sat}, (b) PAE at $P_{back-off}$, (c) FoM_1 for SOTA 100-200 GHz power amplifiers using different fabrication technologies.

In the *PA* design equation, while targeting the high data rates, the peak-to-average power ratio (*PAPR*) is mainly associated with the desired modulation scheme. As *EVM* is the key driver in determining the efficiency and effectiveness of the wireless link. A lower received *EVM* means the proficient demodulation of transmitted data on the receiving side. However, as shown in Table 1, the required *EVM* varied from one modulation scheme to another based on

TABLE 1. PAPR and EVM requirements for various digital modulation schemes [6], [18].

PAPR					
QPSK SC	16-QAM SC	64-QAM SC	QPSK OFDM	16-QAM OFDM	64-QAM OFDM
5dB	6.9dB	7.1dB	9.7dB	10.4dB	11dB
EVM					
BPSK	QPSK	16QAM	64QAM	256QAM	
30 %	17.5 %	12.5 %	8 %	3.5 %	

TABLE 2. Characteristics of state-of-the-art power amplifiers (100-200 GHz) using various fabrication technologies.

Ref./Yr./ Technology	f_c (GHz)	P_{sat} (dBm)	OP_{1dB} (dBm)	PAE @ P_{sat} (%)	PAE @ $P_{back-off}$ (%)	BW_{3dB} (GHz)	Gain (dB)	Area (mm^2)	Topology/Power Combiner
[31]/2021/ 65nm-CMOS	200	9.4	6.3	1.03	Linear	14	19.5	0.92	8-Diff-Stages 2-Way-Combiner
[25]/2022/ 16nm-FinFET	110	11.8	9.2	22.6	6	-	17	0.023	2-Diff-Stages
[32]/2022/ 22nm-FD-SOI	140	17.5	-	16.5	7	38	13.5	0.372	3-Diff-Stages 4-Way Combiner
[21]/2022/ 130nm-SiGe	161	18.1	16.5	12.4	8	40	30.7	0.42	3-Stacked-Stages 4-Way Combiner
[33]/2014/ 90nm-SiGe	116	20.8	17	4	1.2	24	15	4.95	4-CE-Stages 8-Way Combiner
[28]/2021/ 55nm-SiGe	135	19.3	18.5	12	6.7	25	22.4	0.25	4-Diff-Stages
[24]/2020/ 130nm-SiGe	140	18	16	13.8	7	38	31	2.4	5-Diff-Stages 4-Way-Spatial-Combiner
[22]/2019/ 130nm-SiGe	130	17	14	13	5	30	34	1.06	5-Diff-Stages 2-Way Combiner
[34]/2018/ 90nm-SiGe	120	22	21.5	3.6	1.2	35	9	0.62	2-Stage Stacked 8-Way Combiner
[19]/2019/ 130nm-SiGe	170	18	15.6	4	1.5	25	30.2	0.85	3-Diff-Stages 4-Way Combiner
[20]/2020/ 130nm-SiGe	180	18.7	16	4.4	1.5	27	23.6	1.35	3-Stacked-Stages 4-Way Combiner
[23]/2020/ 130nm-SiGe	180	15	13	2.3	1.3	80	19	0.92	3-Diff-Stages 2-Way Combiner
[29]/2021/ 250nm-InP	131	23	20.2	17.8	9.4	24	16.5	1.34	3-Stages 8-Way Combiner
[35]/2022/ 40nm-GaN HEMT	136	23.5	19.7	7.9	3	5	10.5	4.25	3-Stages 2-Way Combiner
[30]/2020/ 250nm-InP	133	15.3	14.4	32	25	30	7	0.2	1-CB Stage SQWL Balun
[36]/2019/ 250nm-InP	130	24	20	7	4	35.6	25	1.86	5-Diff Stages 4-Way Combiner
[37]/2019/ 250nm-InP	132	21	19	10.5	5	34.8	22	0.75	5-Stages 2-Way Combiner

the number of amplitude and phase-modulated waveforms it carries.

For example, 16-QAM requires 12.5%, while 64-QAM needs 8% *EVM* to efficiently devise constellation points owing to their different numbers of amplitude and phase waveforms. Due to this, the required *EVM* places stringent constraints on *PAPR*, further complicating *PA* design. It necessitates a *PA* with (i) high linearity and (ii) a high *PAE* at$P_{back-off}$. However, as discussed before, typically, the *PAs* exhibit low *PAE* in the *back-off* region. Therefore, several techniques for *PAE* at *back-off* and linearity enhancement have been reported in the literature and are given in [18], including (a) out phasing, (b) Doherty-amplifier (c) supply/polar modulation, and RF power DAC [outside the scope of this review]. Like the required *EVM*, the single-carrier-waveform-based modulation scheme (such as 64-QAM-SC) requires a low *PAPR* of 7.1 dB. In comparison, its orthogonal counterpart (64-QAM-OFDM) necessitates 11 dB (high) due to its multi-carrier (with diverse amplitude and phase information) properties. Because of the constructive interference of multiple amplitudes, high-linearity *PAs* are required to avoid signal clipping in the saturation region. In case the *PAPR* requirement is not fulfilled, the transmitted signal quality degrades, ultimately affecting the received *EVM* of a desired modulation.

A summary of this section is presented in Table. 2, which compares the SOTA in power amplifier (*PA*) designs across various semiconductor technologies, highlighting key performance metrics. It includes CMOS, BiCMOS SiGe, and III-V technologies with operational frequencies from 100 GHz to 220 GHz. Key parameters include P_{sat}, *PAE* at P_{sat}, $P_{back-off}$, gain, BW_{3dB}, area efficiency, and power-combining methods. CMOS and FD-SOI technologies achieve moderate P_{sat} and *PAE* with compact designs. On the other hand, BiCMOS SiGe provides higher P_{sat} and gain but lowers efficiency at P_{sat}. III-V semiconductors deliver the highest P_{sat} and substantial *PAE*, making them suitable for sub-THz applications, though their area efficiency varies. Power-combining approaches include 2-way/4-way power combiners and stacked/differential stages, enabling design performance optimization.

B. SPECTRALLY-PURE LO SIGNAL GENERATION

The design shortcomings of high-frequency LO signal sources, which represent a vital transmitter block, must be addressed. High-frequency circuits demand a spectrally pure signal with acceptable output power levels (P_{out}) to operate efficiently. A phase-locked loop (PLL) serves as a significant LO signal source. However, it introduces VCO-instability and phase noise [123] (due to low Q varactors) which is challenging at sub-THz frequencies. Also, the PLL necessitates a frequency divider that further enhances (i) power consumption and (ii) design complexity [38]. Therefore, frequency multiplication is an appropriate method for high-frequency signal generation. The *PN* and P_{out} of the frequency multipliers are functions of the multiplication order (N), which induces another critical aspect, phase multiplication, that causes phase deviation. The minimum degradation introduced by the frequency multiplier in the carrier-to-noise ratio (*CNR*) is given by equation (9) [6]:

$$\Delta CNR = 20\,log\,(N) \tag{9}$$

As a result, a higher N leads to higher *CNR* degradation. For instance, a conventional crystal oscillator with 10 MHz exhibits -170 dBc/Hz at an offset of 100 kHz. While integrating it with a frequency multiplier chain to get 2.4 GHz degrades *PN* by -170 dBc/Hz + 20log(10∗24) = -122 dBc/Hz at a 100 kHz offset. In contrast, a traditionally used direct frequency generator includes an LC tank oscillator, showing a *PN* of -100 dBc/Hz at a 100 kHz offset. Moreover, commonly used multiplication orders include $N = 2$, 3, 4, 6, and 9, depending on the application. Similarly, the frequently used methods include passive varactor or diode-based [39], and active balanced or unbalanced biased FETs [40], [41] frequency multiplication circuits. The former utilizes high input power, while the latter consumes DC power and area due to passive baluns for differential signal generation.

The fundamental circuits from which a frequency multiplier forms are shown in Fig. 10, including a doubler (x2), tripler (x3), and quadruple (x4). Additionally, higher orders of frequency multiplications can be accomplished by cascading these blocks; for instance, $N = 6$, $N = 8$, and $N = 9$ can be implemented by cascading x3+x2, x2+x4, and x3+x3 frequency multipliers, respectively. The MOS varactor passive frequency multiplier [110], [111], shown in Fig. 10(a), leverages the voltage-based junction capacitance (C_v), given in [39] and [111] and equation (10) as:

$$C_v = \frac{C_o}{\left(1 - \frac{v_m(t)}{V_{bi}}\right)^m} \tag{10}$$

$$= a_o + a_1 v_m(t) + a_2 v_m^2(t) + \cdots \tag{11}$$

Here, $a_0 = C_o$, $a_1 = \frac{mC_o}{V_{bi}}$, and $a_2 = \frac{m(m-1)C_o}{2V_{bi}^2}$, and C_o is the zero-bias junction capacitance, where V_{bi} is the built-in potential, and m is the junction grading coefficient, which is the dominant factor, defining the conversion loss of the circuit [39]. The 2nd harmonic current can be extracted from the Taylor and Volterra series simplification [111], which comprises the effect of the time-varying small-signal sinusoidal voltage $v_m(t) = V_m sin\omega t$ in equation (12) as:

$$I_2 = \frac{d}{dt}\left[C_v(t) * v_m(t)\right] \sim \omega K_2 V_m^2 Sin2\omega t \tag{12}$$

Here K_2 corresponds to the circuit's second-order non-linearity coefficient. Furthermore, the input and output matching networks are essential for maximizing the voltage swing at the varactor's node to maximize 2nd harmonic current generation [109], [110], [111]. Similarly, for FET-based active frequency multipliers, as shown in Fig. 10(b)-(d), the Taylor series can be expanded for the gate-source voltage (v_{GS}) and dependent drain current (I_{DS}), as shown in [44] and [111] and given in equations (13) to (14):

$$I_{DS}(v_{GS}) = I_{DS}(V_{GS}) + a_1 v_{GS} + a_2 v_{GS}^2 + a_3 v_{GS}^3 + \cdots \tag{13}$$

$$a_n = \frac{1}{n!}\frac{d^n I_{DS}(v)}{dv^n}|_{v=V_{GS}} \tag{14}$$

Equations (10) to (14) demonstrate the generation of harmonic currents that are crucial for frequency multiplication. However, appropriate varactor/FET device biasing is essential to maximize non-linearity [108], which usually includes class-B, class-AB, class-C, and class-F amplifier operations, where class-F amplifiers exhibit the greatest non-linearity. Moreover, input/output matching conditions for applying a suitable voltage level to the device are indispensable for harmonic generation and extraction. Thus, a balanced input signal (created by Balun) has been used in [45], [46], and [47] for 2nd harmonic generation (x2), which inherently mitigates the odd-harmonics at the output. The former two [45], [46] employ class-B and class-C amplifiers, respectively, while the latter [47] employs class-F amplifier biasing conditions to maximize non-linearity.

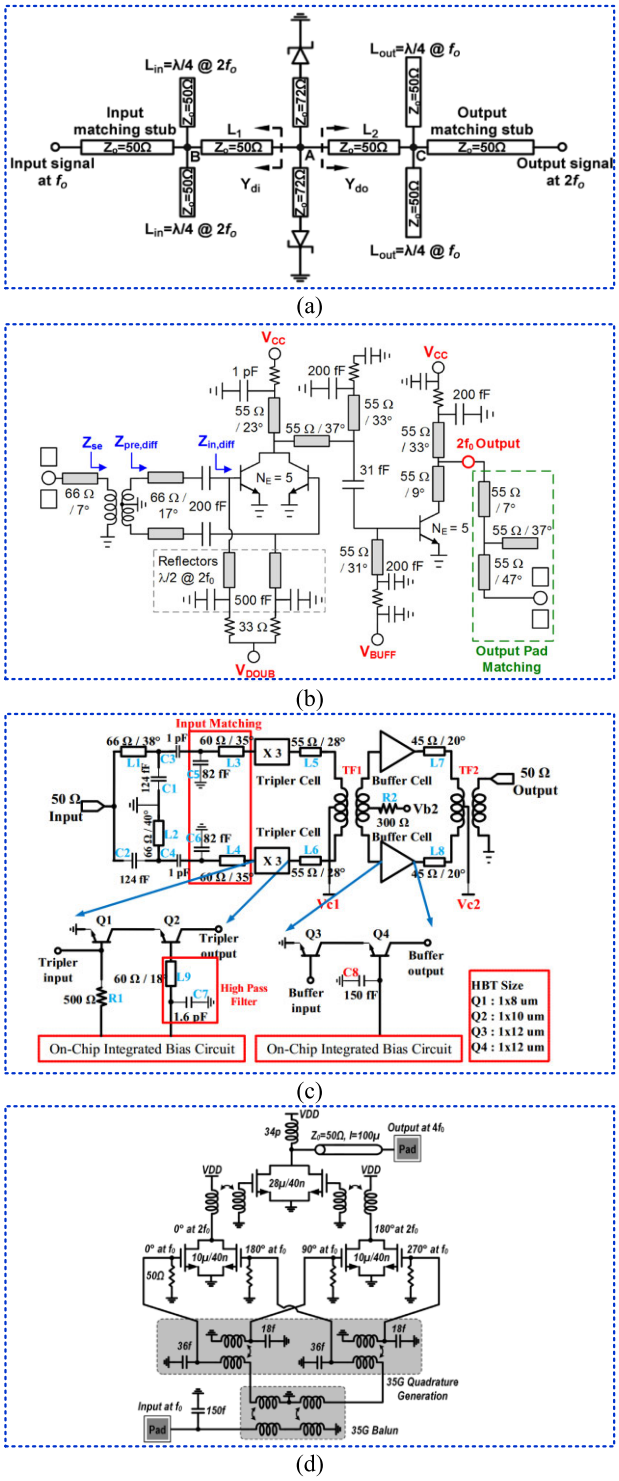


FIGURE 10. mmWave/sub-THz frequency multipliers, (a) Varactor-based passive multiplier [39], (b) Active balanced FET multiplier (x2) [41], (c) tripler (x3) [42] and (d) quadruple (x4) [43].

Similarly, [42], [48], and [49] demonstrate input matching for a fundamental tone and output matching for the 3rd harmonic, with transistors biased to maximize 3rd-order non-linearity to accomplish a frequency tripler. The benefit of

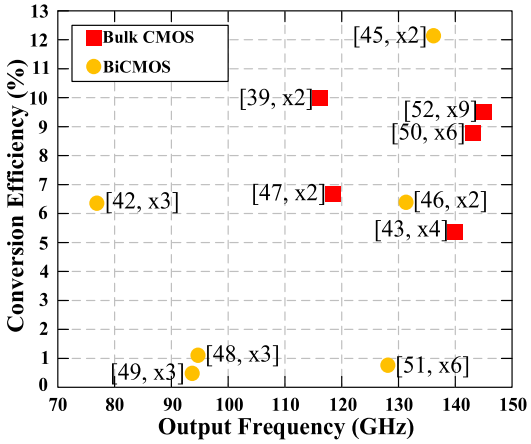


FIGURE 11. Output frequency vs conversion efficiency of mmWave and sub-THz frequency multipliers (x2, x3, x4, x6 and x9) using (Bi) CMOS technologies.

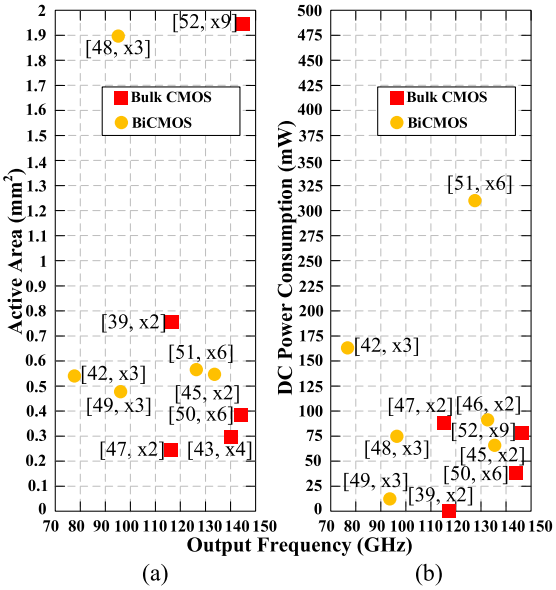


FIGURE 12. (a) Active area, (b) DC power consumption of mmWave/sub-THz multipliers (x2, x3, x4, x6, and x9) with different output frequencies using (Bi) CMOS technologies.

a frequency tripler is that the 3rd harmonic is far from the fundamental tone, which mitigates nonlinear intermodulation products [42]. Likewise, it is possible to use higher multiplication orders. However, the device does not exhibit strong non-linearity for $N > 3$, thus increasing the conversion loss.

As discussed earlier, cascaded topologies have been used to achieve higher-frequency multiplications. For instance, in [43], a miniaturized x4 was presented based on a two-stage cascaded doubler biased in the class-C region with 0°, 90°, 180°, and 270° phase shifts at the input. It still shows a high conversion loss of −21 dB due to the lack of power gain stage. To mitigate the conversion loss that occurs owing to cascaded multiplication stages, x6 frequency multipliers in [50], [51], and [52] are used as interstage driver amplifiers and power amplifiers in the last stage, but at the cost of high DC power consumption.

Fig. 11 shows the conversion efficiencies of various frequency multipliers with BiCMOS doubler (x2), with the maximum efficiency reported at 12.1%. Similarly, Fig. 12(a)-(b) illustrates active area and DC power consumption, showing that higher multiplication orders tend to use more area and DC power due to multiple gain stages necessary for lowering conversion losses. Conclusively, higher-order frequency multiplication with high efficiency is essential for generating spectrally pure signals while reducing complexity in scalable array development.

Table 3 summarizes the highlights of advancements in sub-THz frequency multipliers, driven by technology scaling and architectural improvements. The downscaling of technology nodes from 180nm (SiGe) to 22nm (FD-SOI) has enabled higher output frequencies, lower power consumption, and more compact designs. Architectural improvements, such as incorporating driver amplifiers (*DAs*), *PAs*, and antennas, improve performance metrics like conversion gain and efficiency but often increase power consumption. Efficiency has improved substantially, reaching up to 12.1%, and chip area decreased to as small as 0.21 mm^2. Recent designs

TABLE 3. Specifications of mmWave/sub-THz frequency multipliers (70-150 GHz).

Ref./Yr./ Technology	Architecture	f_c (GHz)	P_{in} (dBm)	P_{out} (dBm)	P_{DC} (mW)	Conversion Gain (dB)	Efficiency (%)	Area (mm^2)
[39]/2009/ 130nm-CMOS	x2	117.5	8.5	-1.5	0	-10	10	0.76
[45]/2021/ 90nm-SiGe	x2	134	16/10	9.4/4	72	0.87	12.1	0.57
[46]/2021/ 55nm-SiGe	Buffer+x2	131.5	-6	8.1	97.5	13.1	6.3	N/A
[47]/2023/ 55nm-CMOS	x2	118.5	10	7.8	88	-0.46	6.8	0.21
[48]/2012/ 180nm-SiGe	x3+Buffer	95.5	0	-10.5	75	-10.5	1.05	1.9
[49]/2013/ 90nm-SiGe	x3	94	6	-28	3	-34	0.05	0.49
[42]/2018/ 130nm-SiGe	x3+Buffer	77.5	2	9.9	158	7.9	6.14	0.53
[43]/2015/ 32nm-SOI	x4	140	26	2.3	-	-21	5.3	0.3
[50]/2022/ 22nm-FD-SOI	x3+DA+x2+PA (x6)	144.5	1	5.1	47	6.85	8.49	0.46
[51]/2018/ 120nm-SiGe	x3+DA+x2+PA (x6)	128	4.3	4.5	310	0.2	0.9	0.55
[52]/2021/ 28nm-CMOS	x3+x3+PA+Ant (x9)	145	6	7.1*	76.7	1.2	9.7	2.03**

*de-embedded antenna gain, **with antenna

demonstrate a balance between power and area efficiencies, which align well with the demands of scalable 6G systems.

C. HIGH DATA RATE MODULATORS

Modulators are another essential building block that can take advantage of the higher operating frequencies. Recalling the Shannon-Hartley theorem, the bandwidth and signal power determine the signal capacity. An increase in the bandwidth necessitates higher frequencies, but the power amplification at these frequencies is limited because of the active device's f_T/f_{max}, as mentioned earlier. Therefore, it is recommended to operate at $\sim f_{max}/2$ of the semiconductor device fabrication technology node with spectrally efficient modulation schemes to realize a practical and energy-efficient solution using commercially available silicon technologies [8], [13], [53]. Thus, increasing bandwidth and operational frequency

is not always a viable solution for mmWave/sub-THz high-data-rate system design.

An alternative solution includes higher-order modulation schemes with spectral efficiency (i.e., QPSK, 2^N-QAM, 4-ASK, and 8-PSK) to improve data rates. Although digital modulation techniques are spectrally efficient and allow higher data rates, they require power-hungry DACs and ADCs. As discussed in the link budget analysis, high linearity and signal-to-noise ratio (SNR) requirements are needed for mmWave *PA*s and *LNA*s. Consequently, these techniques increase the complexity of the system and the DC power consumption. In contrast, analog modulation schemes (e.g., OOK and Binary-Phase OOK) are spectrally less efficient but deliver compact and energy-efficient solutions with high data rates of up to 25 Gb/s [54], [55], [108], [109].

To execute the modulation conventionally, there are two main architectures used, such as (a) heterodyne and (b) homodyne, as shown in Fig. 13(a)-(b). The former uses a complex-modulated intermediate frequency (IF) signal, which compensates for amplitude and phase information. The latter incorporates a multi-level baseband (BB) I/Q signal. The previously mentioned architectures use backend digital signal processing (DSP), including (i) digital pre-distortion (DPD), (ii) pulse shaping (PS), and (iii) equalization (EQ) functionalities [56]. These functionalities are then applied to the up-conversion mixer through digital-to-analog (DAC) converters, which consume high DC power and enhance the system complexity [13], [56]. To mitigate system complexities, direct-digital (DD) modulation has been introduced to realize a compact and energy-efficient architecture, as shown in Fig. 13(c).

Unlike traditional heterodyne/homodyne schemes, DD modulators use mixed-signal circuitry to perform DPD, PS, and EQ operations. For example, as shown in Fig. 13(c), the amplitude and phase of the incoming LO signal are modified by employing switches that can be controlled by using binary data bits.

As mentioned above, DD architecture mitigates the need for multi-bit data converters (ADCs/DACs), thus improving the area and power efficiencies of the system for lower-to-higher-order modulation schemes. For instance, [55], [57], [58], [108], [109] employed digital-direct OOK modulators [Fig. 13(d)]. Also, [108], [109] uniquely present the co-design of the modulator and frequency multiplier, which further reduces the component count and improves scalability. However, the above DD modulators still exhibit less spectral-efficient techniques, such as OOK, ASK, and BPSK, thus, limiting the data rates for a given RF bandwidth.

Meanwhile, [16], [59], [60], and [61] employ mid-level spectral-efficient DD modulators such as QPSK, 4-FSK, and PAM-4, as shown in Fig. 13(e) and (f). Moreover, the highest spectrally efficient DD modulator, which utilizes 16-QAM, has been implemented in [56].

The summary of modulation architectures, presented in Table 4, shows that the traditional modulator architectures

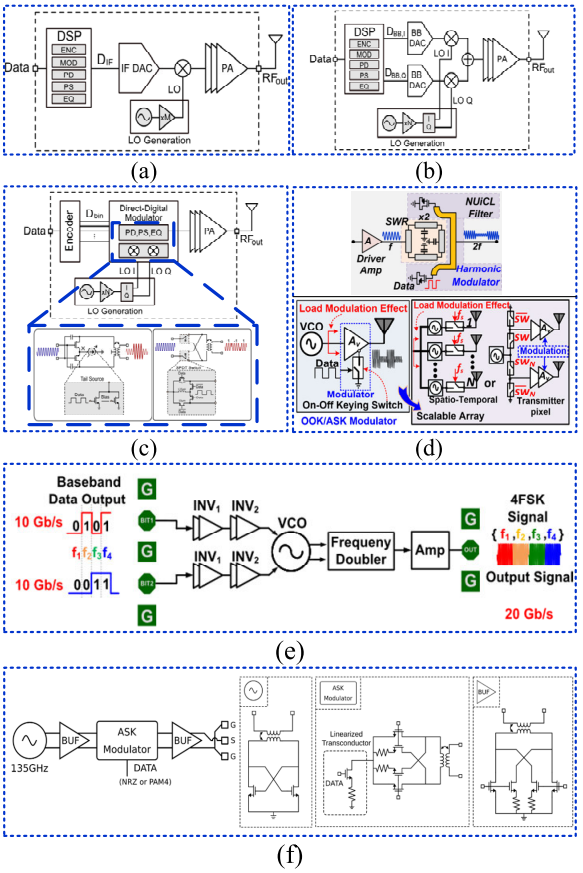


FIGURE 13. Modulation architectures, (a) Heterodyne, (b) Homodyne, (c) Direct-Digital architecture with ASK and PSK switches controlled using binary data bits, generate 16-QAM [56], (d) DD, OOK modulators cum frequency multipliers, employs non-uniform impedance coupled-line (NUiCL) filtering [109], and common-node switching to mitigate the load-modulation effects [108], (e) DD, FSK modulator architecture [16], and (f) Direct-Digital architecture based PAM-4 modulator [60].

generally offer higher data rates by utilizing the more complex modulation schemes, such as 16-QAM and 64-QAM. These architectures are well-suited for high-performance, high-speed communication. However, they necessitate higher power dissipation and larger active areas. In contrast, direct-digital (DD) modulator architectures provide more power-efficient solutions with lower power dissipation and smaller active regions. However, they support lower data rates (up to 50 Gb/s) and modulation schemes up to 16-QAM. Fig. 14 shows the bit-efficiencies of the aforementioned modulation architectures, a significant metric for power consumption analysis in return for data transfer. DD architectures balance performance and efficiency, while homodyne/heterodyne designs prioritize high data rates and modulation complexity. Thus, DD modulators could potentially offer high data rates in the future by implementing 2^N-QAM (N>4) with less complex and power-efficient architectures, which are necessary for sub-THz scalable transmitter array designs.

TABLE 4. Specifications of SOTA high data-rate modulators up to 240 GHz.

Ref./Yr./ Technology	f_c (GHz)	LO+Modulation Architecture	Modulation Type	Data-Rate (Gb/s)	BER	EVM (%)	[E]Power Dissipation(mW)	[E]Active Area (mm^2)
[57]/2013/ 40nm-CMOS	135	Harmonic VCO+ DD Modulation	ASK	10	10^{-11}	-	17.9	0.32
[63]/2014 32nm-SOI	210	HarmonicVCO+Buffer+Conv. Hetero/Homo-dyne Modulation	OOK	10	10^{-5}	-	42	0.04
[108]/2024/ 65nm-CMOS	140	DD Modulation	OOK	10	10^{-6}	-	11-14	0.18
[109]/2024/ 90nm-SiGe	120	DD Modulation	OOK	10	10^{-9}	-	4	0.065
[58]/2016/ 130nm-SiGe	240	VCO+ DD Modulation	OOK	13	-	-	30	0.36
[64]/2017/ 130nm-SiGe	190	LO Buffer+Homodyne Modulation	BPSK	40	10^{-8}	-	32	0.7
[55]/2021/ 55nm-SiGe	220	Harmonic VCO+ DD Modulation	OOK	20	-	-	63	0.25
[65]/2014/ 45nm-SOI	155	VCO+Buffer+ DD Modulation	BPSK/QPSK	20	10^{-12}	16.9	-	-
[60]/2021/ 28nm-CMOS	135	VCO+Buffer+ DD Modulation	PAM-4	50	10^{-6}	-	43.2	0.56
[59]/2016/ 250nm-InP	140	x3+PS+ Hetero/Homodyne Modulation	QPSK/ 64-QAM	48/18	10^{-3}	6.8	78	0.24
[61]/2016 40nm-CMOS	120	VCO+Buffer+DD Modulation	CP-FSK	17	10^{-12}	-	11.1	0.025
[16]/2023/ 65nm-CMOS	165	VCO+x2+DD Modulation	4-FSK	17	10^{-12}	-	47	0.5
[66]/2018/ 65nm-CMOS	87.5	x2/x3+Buffer+ Homodyne Modulation	16-QAM	120	10^{-3}	14	40	0.98
[67]/2019/ 130nm-SiGe	230	x16+Homodyne Modulation	16-QAM	100	10^{-3}	17	1410	-
[68]/2020/ 28nm-CMOS	113	x2+VCO+x2+ Homodyne Modulation	QPSK/ 16-QAM	80	-	25/17	-	-
[69]/2019/ 180nm-SiGe	115	Buffer+x6+Buffer+ Homodyne Modulation	16-QAM	20	10^{-3}	17	228	2.8
[70]/2022/ 22nm-FinFET	140	PLL+x3+Buffer+ Homodyne Modulation	16-QAM	160	10^{-3}	12	80	0.4
[71]/2022/ 16nm-FinFET	109/ 135	x2+Heterodyne Modulation	16-QAM	120	10^{-4}	15.85	292	-
[56]/2024/ 28nm-CMOS	135	x3+x3+LO Buffer+ DD Modulation	16-QAM	32	10^{-6}	11.2	108	0.4

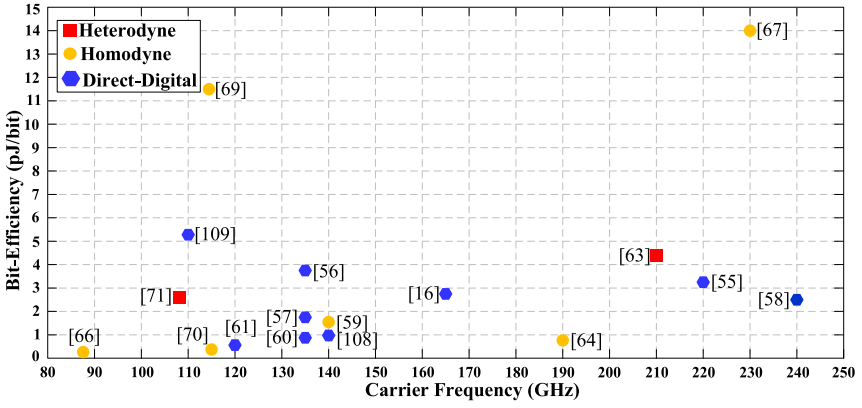


FIGURE 14. Bit-efficiency of various modulation architectures over the carrier frequencies up to 240 GHz.

V. WIDEBAND, HIGH-EFFICIENCY ANTENNA DESIGN WITH CHIP-ANTENNA INTEGRATION TECHNIQUES

This section emphasizes the AoC, AoB, and AiP techniques, focusing on bandwidth, radiation efficiency, and scalability for sub-THz transmitter design. As discussed earlier, the sub-THz spectrum provides a wider bandwidth for enabling higher data rates, which necessitates wideband antenna designs. Similarly, high-efficiency antenna structures

are required to effectively radiate power from the chip. The antenna dimensions are comparable to the chip sizes at high frequencies, making them suitable for implementation in arrays, enabling higher *EIRP* and beamforming capabilities. However, maintaining an inter-element spacing of $\lambda/2$ at the operational frequency is required to avoid aliasing and grating lobes [72], highlighting the importance of a scalable antenna array.

A. ANTENNA ON CHIP (AOC)

This section discusses AoC's shortcomings and future potential as a wideband and high-efficiency antenna in scalable array systems. AoC antennas are widely used for mmWave/sub-THz wireless communication. It features miniaturized form factors, high yields, reproducibility, and a lack of additional packaging steps that avoid chip-antenna interconnection losses (e.g., bond wire and flip-chip). The AoC execution involves back-end-of-line (BEOL) metallization in the standard CMOS fabrication process. Although the manufacturing of on-chip antennas incurs excessive costs owing to the expensive wafer area, it provides the closest chip-antenna integration, reducing packaging costs and wire bonding losses. Technologies such as bulk CMOS, FinFET, FDSOI, and SiGe BiCMOS are commonly used. These antennas have low-to-moderate radiation efficiencies owing to the low resistivity of the bulk silicon (Ω-cm), which allows for the propagation of surface waves confined within the substrate. Also, chip fabricators impose metallization restrictions to avoid density issues, which affect the radiation performance of the antenna and further decrease radiation efficiency.

$$Bandwidth \propto \frac{\varepsilon_r - 1}{\varepsilon_r^2 + 1} \frac{WH}{L} \tag{15}$$

Here, ε_r is the relative permittivity of the dielectric, W and L are the width and length of the antenna, respectively, and H is the height of the dielectric substrate. In addition to the high permittivity of bulk silicon, the height of the substrate (restricted to a few μm) limits the bandwidth of the on-chip antennas, as given in equation (15). Therefore, radiation efficiency and bandwidth are two primary performance metrics that are distorted in on-chip antenna configurations. Methodologies have been introduced in the literature to improve performance metrics. For instance, the substrate shielding mechanism has been explored in the literature to shield the bulk silicon from the top antenna metal. This enhances the antenna gain/directivity but causes destructive interference and reflections from the ground owing to the small H.

An on-chip bond wire dipole antenna was implemented in [73] to avoid chip grounding effects, which exhibited the simulated efficiency of 69%, as shown in Fig. 15(a). Furthermore, the artificial magnetic conductor (AMC) surfaces have been implemented under the antenna structure to suppress unwanted substrate waves and improve impedance bandwidth. Reference [74] shows 19% fractional bandwidth by employing an AMC in the 28 nm CMOS technology process, as shown in Fig. 15(b).

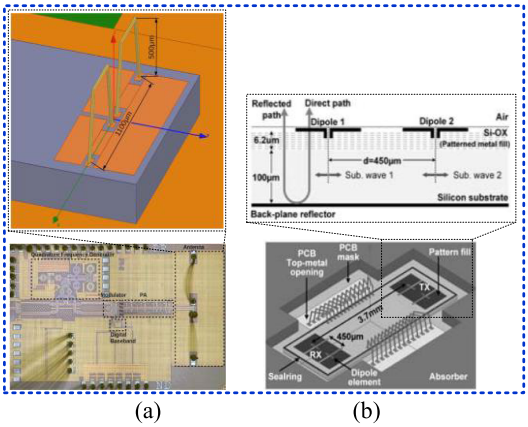


FIGURE 15. (a) Implementation of wire-bonded AoC to improve efficiency [73], (b) AMC-based AoC to enhance bandwidth [74].

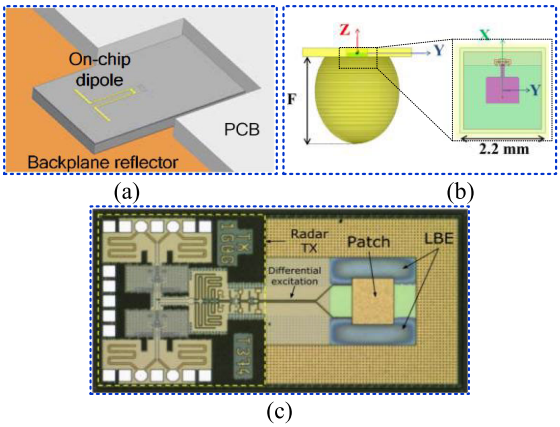


FIGURE 16. (a) Substrate-tuned dipole antenna with back place reflector [75], (b) IPD-based patch antenna with lens [76], (c) LBE antenna [77].

In addition to creating a metallic shield between the antenna and the silicon bulk, other methods to improve antenna performance metrics (e.g., gain, bandwidth, and efficiency) have been developed. One method is to change the bulk silicon to prevent substrate loss by increasing its resistivity using ion irradiation or by reducing the bulk thickness by etching. For instance, in [75], silicon thickness was optimized to improve the gain of the on-chip antenna, achieving a wide bandwidth of 120-140 GHz using a backplane reflector, as shown in Fig. 16(a).

Another method is to use integrated passive device technology to improve the efficiency, as demonstrated in [76], which achieved 50-60% efficiency at 125 GHz, as shown in Fig. 16(b). Localized back-side etching (LBE) is a widely known improvement technique. In this technique, silicon is selectively etched or removed from specific locations to reduce substrate loss. For example, [77] exhibits 60% simulated efficiency with a 10 GHz bandwidth using an LBE-based patch antenna, as shown in Fig. 16(c).

As discussed, the low-resistivity silicon substrate in the AoC design traps surface waves inside the substrate and

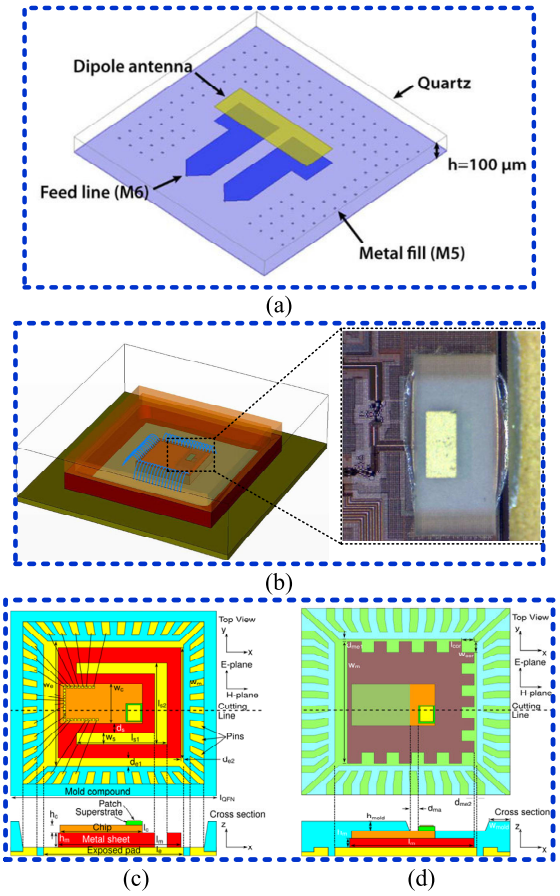


FIGURE 17. (a), (b) AoC with quartz superstrate [78], [79] and Modified QFN package using (c) Metallic U-slot, (d) Introduced molding compound inside QFN package to improve radiation pattern [80].

reduces the antenna's radiation efficiency. To address this, another approach in the literature for on-chip antennas to guide radiation energy toward free space has been developed. It includes an additional assembly process to deposit a superstrate (with a secondary resonating element) on top of an on-chip antenna.

For instance, in [78], the feedlines were designed on-chip while the dipole patch was designed on a quartz superstrate ($\varepsilon_r = 3.8$ and $H = 100\ \mu$m) and aligned later with on-chip feedlines, as shown in Fig. 17(a). It shows an efficiency of 45% (5)-10% better than standard on-chip antennas) with a comparatively wide bandwidth of 106-114 GHz.

Similarly, [79] used the same approach with a quartz superstrate to achieve 50% efficiency over a bandwidth of 115-123 GHz, as shown in Fig. 17(b). This technique improves the on-chip antenna efficiency but is more prone to misalignment while placing the superstrate on the chip. Additionally, [80] introduced modifications to the standard QFN packaging to improve the radiation pattern of the on-chip antenna, as shown in Fig. 17(c), achieving a maximum demonstrated radiation efficiency for an on-chip antenna of 62% at 160 GHz.

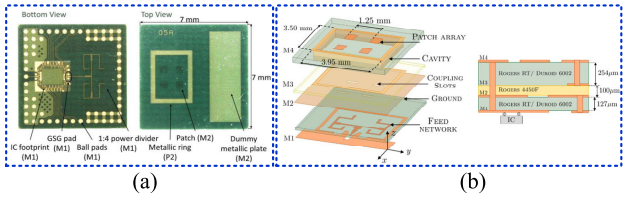


FIGURE 18. (a) 2 × 2 antenna array build-up using high-density-interface (HDI) processing [81], (b) 2 × 2 antenna array using low permittivity Roger's substrates [82].

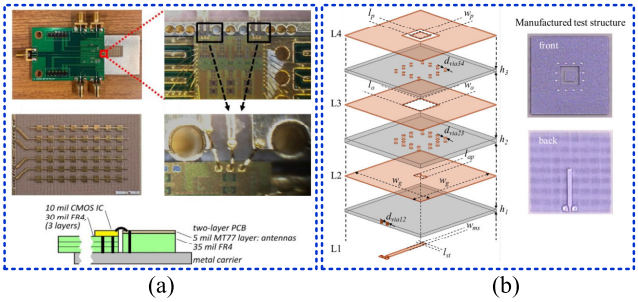


FIGURE 19. (a) 8-elements series-feed microstrip patch antenna array for MIMO applications [83], (b) Aperture feed cavity-backed patch antenna build-up using semi-additive processing (mSAP) [84].

B. ANTENNA ON BOARD (AOB)

PCB technology is widely known for its well-established manufacturing process. It is common to design circuits and antennas for applications ranging from sub-6 GHz to terahertz using PCB technologies. Therefore, AoB leverages low cost, simplicity in manufacturing, and fast time to market with various available PCB materials and processes. In contrast to AoC technology, PCBs have thick metal and dielectric layers. The thick metal reduces ohmic losses and offers better radiation efficiency. In contrast, the thick dielectric improves the bandwidth as the electric fields are not tightly confined between the top and bottom metals, as shown in equation (15).

For instance, a 20% fractional bandwidth was achieved in [81] using a 2 × 2 antenna array on Mitsubishi substrates CCL-HL972 and GHPL-970 ($\varepsilon_r = 3.4$ and $Tan\zeta = 0.005$, $H = 200\ \mu$m) with a High-Density-Interconnect (HDI) PCB process, as shown in Fig. 18(a). Likewise, in [82], the same technique of aperture coupled feeding as in [81] was implemented on low-cost Roger's substrates, including RO4450F ($\varepsilon_r = 3.52$ and $Tan\zeta = 0.004$, $H = 100\ \mu$m) and RT Duroid 6002 ($\varepsilon_r = 2.94$ and $Tan\zeta = 0.0012$, $H = 381\ \mu$m), achieving a bandwidth of 114-144 GHz, as shown in Fig. 18(b).

While the HDI process produced 55% efficiency, the latter used low-cost PCB stacking technology. Both designs use a plastic lens to enhance directivity, which makes the structures bulky and non-ideal for scalable large antenna arrays. In [83], a low-cost antenna and packaging were presented by implementing an 8-element series-fed patch array on an Isola Astra MT77 ($\varepsilon_r = 3$ and $Tan\zeta = 0.0017$, $H = 127\ \mu$m) substrate, which shows a narrow fractional bandwidth of 6.8%, as shown in Fig. 19(a).

Overall, AoB is cheaper but relies on PCB technology (i.e., HDI, Semi-Additive mSAP, and standard stacking). PCB processing technology limits the etching tolerances, that is the minimum line width, spacing, and minimum via diameter, impacting the realized impedances. For instance, the laser etching technology in HDI and other advanced processing provides 40/40/75 μm width/spacing/via-diameter, while in the standard PCB process, it is 50/50/90 μm. As a solution, semi-additive processing, which electroplates copper instead of etching copper as in the standard method, has been adopted to achieve a minimum spacing of 50 μm while keeping the design costs low.

As an example in [84], a cavity-back stacked antenna with aperture-coupled feeding, shown in Fig. 19(b), was developed using mSAP on Panasonic Megtron 7N ($\varepsilon_r = 3.2$ and $Tan\zeta = 0.003$, $H = 373$ μm) substrates. It exhibited a fractional bandwidth of 14% with an efficiency of 71%. PCBs offer a diversity of options, including rigid and flexible substrates. In [85] an antenna design for flexible substrates was proposed. It uses a stacked patch topology with an aperture-coupled feeding mechanism on a flexible substrate ($\varepsilon_r = 3.1$ and $Tan\zeta = 0.003$, $H > 500$ μm) as shown in Fig. 20. It demonstrated a fractional bandwidth of 35.8% and efficiency of 89% in the simulations. This is the highest reported for an off-chip antenna in the sub-THz spectrum.

In summary, the AoB approach supports a wider bandwidth than on-chip antennas, essential for 6G high-data-rate radio design. Moreover, it offers a variety of processing technologies based on the minimum tolerances (trace width, spacing, and via-diameter) necessary to meet the mmWave signal impedance and transmission requirements, that is standard, HDI, and mSAP. Although low-loss substrates (Rogers and Isola Astra MT77) have been used to improve the transmission bandwidth, the surface roughness and other losses associated with substrates are still in the order of dB/cm, [83], [84]. These degrade the signal transmission and add loss to the distribution network, degrading the overall system efficiency, as given in [81], [82], and [84].

C. ANTENNA IN PACKAGE (AIP)

Unlike the AoB technology, antenna-in-package (AiP) accommodates the antenna and die/chip in a single-surface-mount package. Fig. 21 illustrates the various configurations of AiP technology that have been demonstrated using horizontal (Fig. 21(a) and (d)) and vertical (Fig. 21(b) and (c)) antenna-chip integrations. Like the AoB technique, wire bonding is a low-cost standard solution for AiP, as shown in Fig. 22(a). However, the bond-wire length plays a critical role in defining the impedance and can lead to impedance mismatch, transmission loss, and bandwidth degradation due to parasitic effects. An alteration in the standard package and circuit is required to compensate for parasitic effects.

For example, the low-cost wire-bonded AiP solution presented in [86] uses a Liquid Crystal Polymer (LCP) substrate ($\varepsilon_r = 3.16$ and $Tan\zeta = 0.0049$, $H = 100$ μm). The

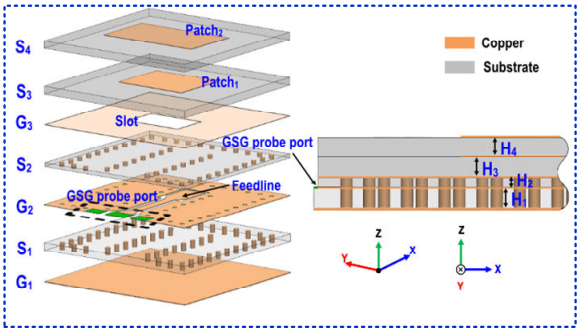


FIGURE 20. Single-element stacked patch antenna on flexible PCB substrate [85].

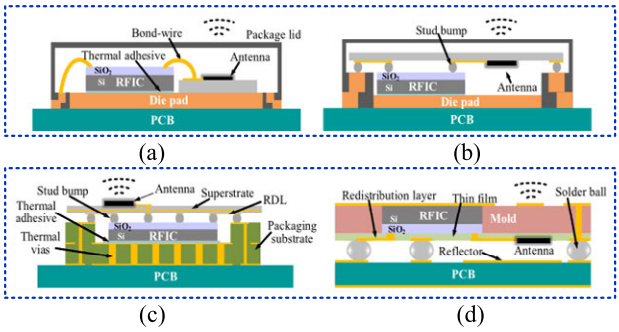


FIGURE 21. Implementational topologies for Antenna-in-Package (AiP) using (a) Wire bonding, (b) Flip-Chip integration, (c) Panel-Level Fan-Out (PLFO) package with flip-chip integration, and (d) Embedded Wafer-Level Ball Grid (eWLB).

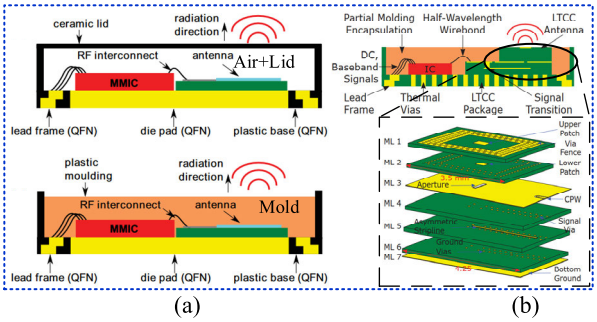


FIGURE 22. AiP technology with wire bonding (a) Liquid Crystal Polymer based antenna wire bonded with the chip using a package with Air+Lid and molding material, (b) LTCC-based aperture-coupled stacked-patch antenna with partial molding [86], [87].

design uses bond wires with $\lambda/2$ length at 122 GHz, offers self-compensation in impedance transformation from chip to antenna, and shows insertion losses of approximately 2 dB. To improve the impedance bandwidth from 10% to 20%, the bond wires were covered with a molding compound called Polytec TC430-T and Stycast 1266 [Fig. 22(a)].

Likewise, a low-temperature co-fired ceramic (LTCC) substrate, DuPont Green Tape 9K7V ($\varepsilon_r = 7$ and $Tan\zeta = 0.0012$, $H = 530$ μm), has been used to realize an aperture-coupled stacked-patch antenna in [87], Fig. 22(b). It uses a half-wavelength bond wire for self-compensation and

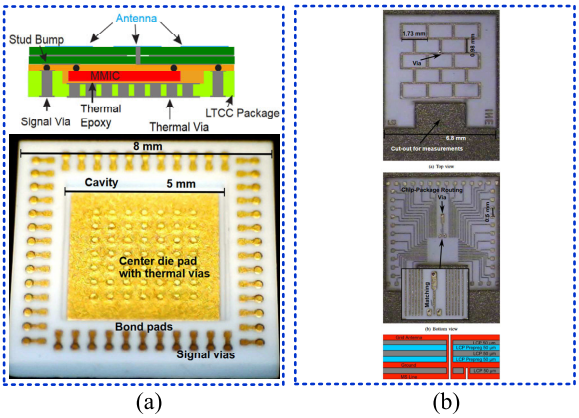


FIGURE 23. AiP realization using flip-chip integration technique (a) Design concept of chip-antenna integration using flip-chip and LTCC package with thermal vias and connection pads, (b) LCP-based grid antenna array used as the lid of LTCC package [88].

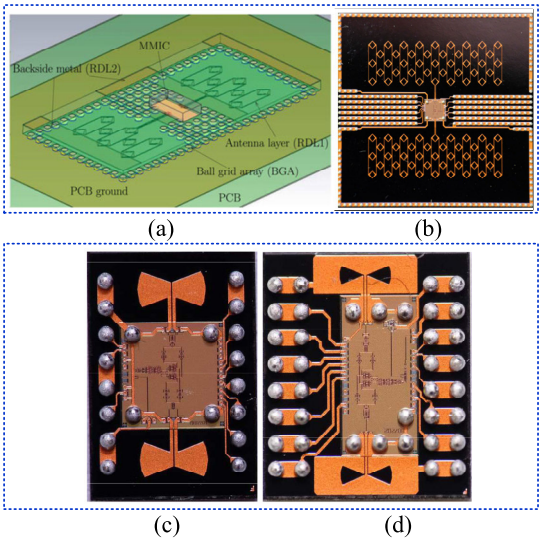


FIGURE 24. AiP realization using eWLB integration technique (a) 3D view of eWLB integration with MMIC, RDL, BGA, and antenna array, (b) 43-elements antenna array realized in eWLB package, (c) D-band eWLB package with bow-tie antenna, (d) J-band eWLB package with slot bow-tie antenna [89], [90], [91].

partially molds a dummy chip and antenna using Polytec TC 430-T material. It shows a 1.86 dB loss for the bond wire, 11.2% impedance bandwidth, and a simulated antenna efficiency of 86%.

Moreover, the flip-chip integration shown in Fig. 21(b) is an alternative to wire bonding with reduced interconnection lengths and better performance owing to the reduced parasitic effects. The implementation involves affixing the radio frequency integrated circuit (RFIC) using an adhesive to the package and flip-chipping the mounted antenna to its top. The concept of a flip-chip can be further extended towards panel-level fan-out (PLFO) packaging.

The flip-chip AiP concept involves the integration of an RFIC within the package. At the same time, the antenna and redistribution network are separately designed on a superstrate and later mounted with the bottom package in a flip-chip configuration. As shown in Fig. 23(a), Hirai Precision, Japan, developed a 300 μm deep cavity for MMIC on an LTCC tape material CS71 (Thickness = 400 μm). The cavity included thermal vias to conduct heat from the die to the ambient environment. Moreover, the grid antenna array was designed on a multilayer LCP superstrate with routed transmission lines and a flip-chip mounted on the LTCC package as a lid, Fig. 23(b). It exhibits an efficiency of 83% with a low-fractional bandwidth of 4.6% at a center frequency of 128 GHz.

Unlike wire bonding, the flip-chip method is not limited to connections from chip edges only; it can accommodate antenna-chip integration from any side of the chip to support densely populated packaging. One of the latest integration techniques in AiP technology is the embedded wafer-level ball grid (eWLB) introduced by Infineon AG, as shown in Fig. 24(a)-(d).

In eWLB technology, the MMIC is first embedded into a mold compound facing downwards. A redistribution layer (RDL) composed of dielectric and metal for antennas and transmission lines surrounds the MMIC and fans out the chip pads and connections. Finally, solder balls connected the chip antenna assembly to the PCB. Moreover, in eWLB integration technology, the PCB plays a critical role by providing a reflector for the antenna to improve its directivity while supporting the baseband and DC signaling. The eWLB technology offers several benefits including better RF performance, reduced chip-antenna interconnect length, a small form factor, and high I/O density.

The designs included in [89], [90], [91], and [92] exhibited simulated antenna efficiencies of 60-85% with fractional bandwidths ranging from 9.9% to 31%. Fig. 25(a)-(b) summarizes antennas' radiation efficiency and fractional bandwidth performance using various topologies. This shows that AoBs and AiPs provide better bandwidth and efficiency than AoCs. Furthermore, the AiP leverages the benefits of integrating multiple high-efficiency system components using heterogeneous integration.

Table 5 presents a range of antenna designs with efficiencies ranging from 45% to 89%. The table reflects the use of diverse technological approaches and materials. High-efficiency (>80%) antennas employ advanced substrates such as LTCC, LCP, and flexible PCBs which are typically associated with technologies like AoB and AiP. To enhance performance, these antennas use sophisticated integration techniques, including wire bonding, flip-chip, eWLB, and mold compound integration. Substrates like Si, Glass, and LCP are commonly utilized to achieve optimal functionality. In contrast, the AoC*s* have lower efficiencies but still incorporate specialized features such as AMC, IPD, and QFN packaging modifications to improve efficiency performance.

VI. HETEROGENEOUS INTEGRATION

This section discusses the fully packaged heterogeneously integrated arrays for next-generation communication

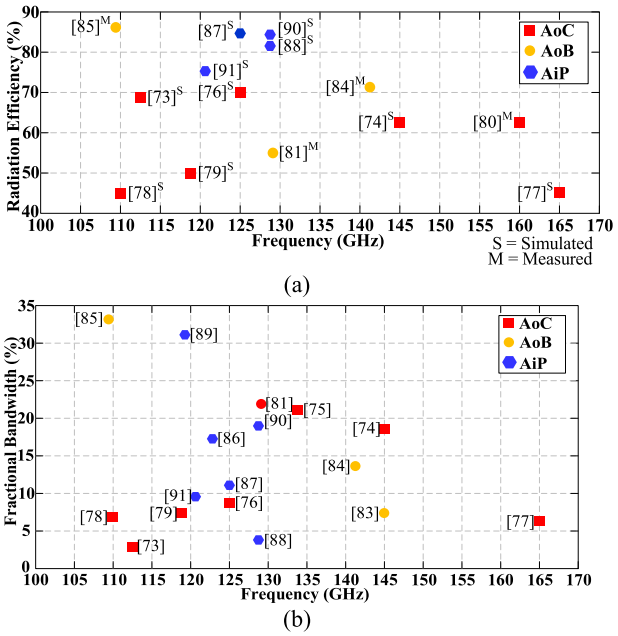


FIGURE 25. (a) Radiation efficiencies of various antenna implementation topologies over the operational frequency, (b) Fractional bandwidth of the antennas from different topologies to evaluate wide bandwidth characteristics.

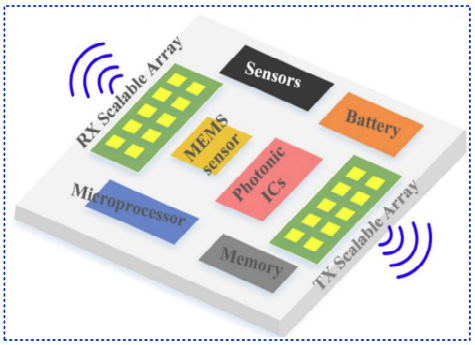


FIGURE 26. Conceptual illustration of heterogeneous integration comprises different technologies RF-TRX, MEMS, photonics, memory, and microprocessors on shared substrate/platform to improve system functional density [96].

TABLE 5. Specifications of state-of-the-art D-band antenna technologies.

Reference /Year	Antenna Type	Size [mm²]	Gain [dBi]	Efficiency (%)	f$_c$/BW (GHz)	Technology/ Substrate	Feature
[73]/2014	Bond wire	1.2x0.5	4.4	^{S}69	114/3	AoC/CMOS	
[74]/2019	Dipole Patch	1.2x0.65	^{S}2.5	^{S}62	145/27	AoC/CMOS	AMC structures
[75]/2014	Rectangular Patch	1.2x0.9	4		133/28	AoC/SiGe	Ground Reflector
[76]/2014	Dipole Patch	2.2x2.2	^{S}1.6	^{S}70	125/10	AoC/Glass	Integrated Passive Device (IPD)
[77]/2019	Folded Dipole Patch	1.3x1.3	3	^{S}45	165/10	AoC/SiGe	Localized Backside Etching (LBE)
[78]/2013	Differential Dipole Patch Array	5.5x5.5	^{S}13.5	^{S}45	110/8	AoC/SiGe	Quartz Superstrate
[79]/2012	Rectangular Patch	1.3x0.8	6	^{S}50	119/8	AoC/SiGe	Quartz Superstrate+Parasitic Patch
[80]/2018	Dielectric Resonator Patch	^{P}5x5	6	62	160/-	AoC/SiGe	Modify standard QFN package
[81]/2017	2x2 Aperture Coupled Array	7x7	^{L}28	55	129/30	AoB/CCL-HL972	High-Density Interface Ball-Grid-Array
[82]/2019	2x2 Aperture Coupled Array	^{T}42x42	^{L}29.5	55	129/30	AoB/RT Duroid 6002	Conventional Low-Cost PCB Processing
[83]/2020	8-elements Series Feed Patch Array	10x1.1	13.6	-	145/10	AoB/ Isola MT77	Integration: Wire bond
[84]/2020	4x4 Aperture Coupled Feed Array	4.2x4.2	14	71	143/20	AoB/ Megtron 7N	Semi-Additive Processing
[85]/2022	Aperture Coupled Stacked Patch	1.3x1.3	7.95	89	109/38	AoB/ MFLEX	Flexible PCB
[86]/2016	Patch+Parasitic Patches	3x3	4.8	-	122/21	AiP/LCP	Integration: Wire bond with Mold Compound
[87]/2018	3x3 Aperture Coupled Stacked Patch	3x3	10.1	^{S}86	125/14	AiP/LTCC	Integration: Wire bond with Mold Compound
[88]/2013	18-Elements Grid Array	5.3x5	15	^{S}83	128/6	AiP/LTCC	Integration: Flip-Chip
[89]/2017	8-Elements Rhombic	3.9x2.7	11	-	119/37	AiP/eWLB	Integration: Flip-Chip + Redistribution Layer
[90]/2018	Bow-Tie	2x2	5.8	^{S}85	128/25	AiP/eWLB	Integration: Flip-Chip + Redistribution Layer
[91]/2018	43-Elements Rhombic	13.7x4.9	15.5	^{S}75	121/12	AiP/eWLB	Integration: Flip-Chip + Redistribution Layer

S=Simulated, P=Package Size, L=With Plastic Lens, T=Transmit array (40x40)

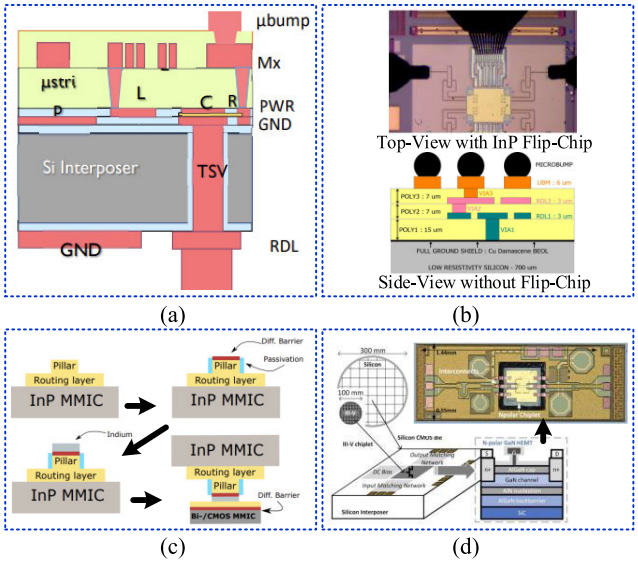


FIGURE 27. (a) Silicon Interposer from IMEC [117], Hetero-Integration of (b) IMEC Si-Interposer with InP PA for 140 GHz [118], (c) Direct InP-to-BiCMOS chips [119], and (d) GaN/InP and Standard Silicon [120].

systems. Thus, heterogeneous integration is a key technology that enables advanced wireless communication. It paves the way for ''More Than Moore'' (MtM) by recasting the technological epicenter from transistor-level innovations to the package and system levels. Consequently, it advances the functional density of the system by integrating (a) RF TRX, (b) MEMS, and (c) Microprocessors and Photonic Sensors, as shown in Fig. 26, to realize System-In-Package (SiP) in 2D, 2.5D and 3D configurations [87].

A challenge arises when selecting a common platform or substrate for packaging and integrating active and passive circuits with antenna arrays. Thus, a substrate with (a) low ε_r and tanδ, (b) low coefficient of thermal expansion (CTE), and (c) the ability to support multilayer designs with fine pitch and high I/O densities [93]. Conventionally, low-temperature cofired ceramics (LTCC) and liquid crystal polymers (LCP) have been extensively used for high-frequency packaging. However, the former is limited owing to high processing temperatures, thick substrates for stacking, and a significant CTE mismatch with PCB technologies. The latter is limited because of the surface roughness of the polymer substrates, leading to unacceptable losses at high frequencies and inapt CTE profiling in the z-direction. Both technologies face reliability challenges and difficulties in forming large arrays [93], [94], [95].

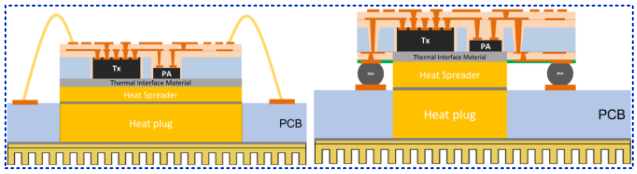


FIGURE 28. Conceptualization of 2.5D heterogeneous integration of RF front end module along with Die embedded in the glass, (a) Wire-bonding transition, (b) Flip-Chip transition [99].

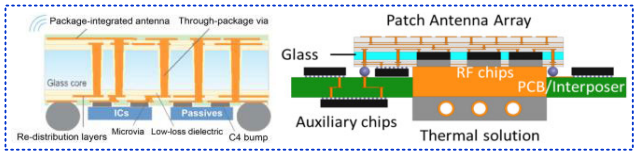


FIGURE 29. (a) Illustration of glass-based RDL with TSVs, antenna, and chips, (b) Integration of glass-based RDL with other interposer technologies [100].

InFO from TSMC, embedded wafer-level ball grid array (eWLB) from Infineon, and Si-interposer from IMEC offer substitutes by using redistribution layers (RDL) with an ultra-fine pitch for sub-THz frequencies [90], [97], [117]. Here, the latter most, [117], has been presented particularly for high-frequency applications, having an insertion loss of less than 0.3 dB/mm, as shown in Fig. 27(a). Likewise, the work presented in [117] has been later extended in [118] by integrating Si-interposer and indium phosphide (InP) *PA*, which paves the way for cost-effective heterogeneous integration in the future, as shown in Fig. 27(b). Although the silicon interposers offer dense integration, however, they are limited by the high ε_r of silicon which causes signal integrity and radiation efficiency (of the antennas) challenges. In addition, through-silicon vias (TSVs) have more significant insertion losses, fabrication costs, and complexity [98]. An interesting heterogenous-integration technique is presented in [119], which directly integrates the InP-on-BiCMOS chip, as shown in Fig. 27(c). Likewise, [120] presents the hetero-integration of the standard silicon process and GaN/InP *PA*. It utilizes the BEOL metal layers of the silicon technology for in/out matching network designs [which comprises high Q factor components] and GaN/InP for power amplification, as shown in Fig. 27(d).

In recent years, glass-based packaging technology has laid the foundation for low-loss passive circuits and high-efficiency antenna designs, which are vital for a 6G scalable array development [94], [95]. It incorporates silicon-like fine-pitch and large-panel processing capabilities, thus reducing fabrication costs and enabling large arrays. It also supports front and backside low-loss metallization solutions to form high-density RDLs. Moreover, the low CTE of glass makes it a suitable candidate for co-integration with other technologies, i.e., laminates, LTCC, and LCP, to realize 2.5D or 3D heterogeneous integration [95]. The conceptualization

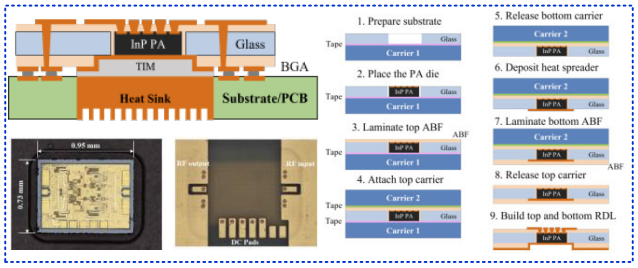


FIGURE 30. Description of InP PA, Glass interposer, and PCB technologies heterogeneous integration with process flow diagram and embedded InP chip picture [121].

TABLE 6. Summary of SOTA *D*-band fully packaged arrays.

Ref./ Year	Freq. (GHz)	Antenna Technology	RFIC Technology	Modulator IC	Packaging Scheme	EIRP @ P_{sat} (dBm)	RFIC-Antenna	RFIC-Modulator
[68]/ 2020	113	1x2/AoB	28nm-CMOS		1D-Heterogeneous Integration	0	Flip-Chip	Same-Chip
[103]/ 2020	130-170	8x16/AiP/ Glass	130nm-SiGe		2D-Heterogeneous Integration	–	Flip-Chip	Same-Chip
[105]/ 2020	130	2x2/AiP/ eWLB with Lens	55nm-SiGe		2D-Heterogeneous Integration	28	eWLB	Same-Chip
[106]/ 2021	139-156	2x2/AoB/ Astra MT77	45nm-PD-SOI		1D-Heterogeneous Integration	5	Flip-Chip	Same-Chip
[107]/ 2021	144	16x8/AiP/ Astra MT77	45nm-FD-SOI		2D-Heterogeneous Integration	27	Wire-bond	Same-Chip
[101]/ 2022	136-147	4x2/AoC	45nm-FDSOI		2D-Homogenous Integration	32	Same-Chip	
[102]/ 2022	130-140	8x8/AiP/ Kyocera Ceramic Interposer	III-V	22nm-FD-SOI	2D-Heterogeneous Integration	27.5	Wire-bond	Flip-Chip
[104]/ 2022	130-164	16x16/AiP/ Glass	130nm-SiGe		2D-Heterogenous Integration	58	Flip-Chip	Same-Chip
[112]/ 2024	140	8x8/AiP/ Panasonic Organic Laminate	45nm-RFSOI		2D-Heterogenous Integration	34-37.5	Flip-Chip	Same-Chip

of 2.5D heterogeneous integration based on glass interposer can be seen in Fig. 28(a)-(b). The silicon/III-V dies were embedded inside the glass wafer, and a heat spreader was incorporated to manage the temperature. Moreover, through-glass-vias (TGVs) have been employed for chip-antenna integration. The signal transition from the outside/PCB can be realized by either wire bonding or flip-chips. Furthermore, the glass-based redistribution layers (RDL) are illustrated in Fig. 29(a)-(b) to show fan-out wafer-level packaging along with an antenna array-on-glass and its integration with a laminate-based substrate.

Thus, the radio-on-glass, presented in [121], utilizes a flip-chip connection (with a package loss of 1 dB), though it does not show thermal management. The glass-interposer-based concepts [Fig. 28 and 29] are realized in [122], where the InP die is embedded inside the glass substrate with the growth of vertical interconnections and TSVs. The package shows an insertion loss of 1 dB. However, it offers a backside metal layer deposition as a heat-spreader, as shown in Fig. 30, which is particularly vital for high-power circuits.

Table 6 presents SOTA in *D*-band arrays based on the packaging schemes [Homo/Heterogenous], antenna design methodologies [AoC, AoB, and AiP] with chip-antenna integration techniques [wire bond, flip-chip, eWLB], modulator-IC [CMOS, SiGe], and RF front end/RFIC [III-V] fabrication technologies. Most of the designs use the AiP/AoB packaging

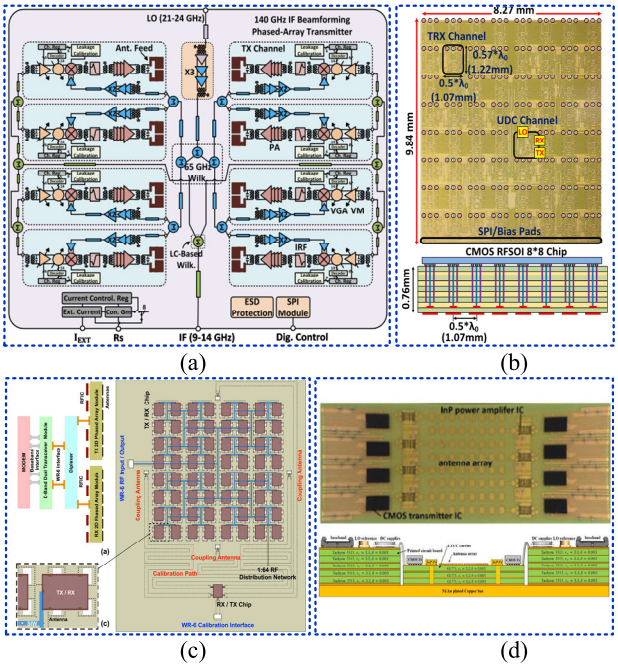


FIGURE 31. Applications of homogenous integration comprise (a) on-chip antenna [101] and heterogeneous integration by using (b) In-package antenna technique for CMOS and laminate [112], (c) Glass-interposer based antenna [104], and (d) Laminate antenna, CMOS beamformer, and III-V PA [102].

approaches, instead [101] as shown in Fig. 31(a), which uses an on-chip antenna-based packaged array in CMOS 45nm FD-SOI technology. Additionally, the silicon chip is integrated with a laminate-based AiP solution [112], as shown in Fig. 31(b), which reduces packaging costs due to standard PCB processing. Similarly, in another attempt to realize HI, SiGe BiCMOS has been integrated with antenna-on-glass in [103] and [104], as shown in Fig. 31(c), which leverages the benefits of glass-based interposer and also delivers wide bandwidth. Besides, [102] established a proper heterogeneous integration by employing silicon, III-V, and ceramic interposer technologies together, as shown in Fig. 31(d). It harnesses the benefits of (a) modulation by using CMOS FD-SOI, (b) high output power from III-V, and (c) low-cost antenna design by using LTCC carrier, collectively paving the way toward future HI.

VII. SUB-THZ MEASUREMENTS

Until now, the focus has been on evaluating the shortcomings of the circuit-level implementation of sub-THz communication systems. However, this section discusses the methods and challenges associated with sub-THz system measurements. There are two commonly used measurement approaches: (a) on-wafer measurements and (b) wireless measurements. The former comprises the characterization of on-wafer dies using sophisticated probing mechanisms. While the latter uses on or off-chip antennas to measure the over-the-air (OTA) performance of the transceiver.

Furthermore, the on-wafer characterization comprises (i) small-signal measurements that include scattering parameters (s-parameters), (ii) large-signal power measurements, such as P_{in} vs P_{out}, $IIP3$, $OIP3$, and Gain, (iii) noise measurements that are noise floor/noise figure, and (iv) modulation performance measurement. Fig. 32 shows the measurement mechanisms. As illustrated in Fig. 32(a), to mitigate the loss associated with coaxial cables in the D-band, waveguide transitions have been used that also provide good out-of-the-band rejection. The waveguide standard for the D-band is WR-6/WR6.5. Furthermore, vector network analyzers (VNA) or power network analyzers (PNAx) from Keysight and other vendors are usually used for small signal measurements, as shown in Fig. 32(b).

However, most VNA/PNAX variants cover up to 26.5 GHz, 40 GHz, or 67 GHz. Therefore, Virginia Diode Incorporation (VDI) frequency extenders have been integrated into the network analyzer output to extend to frequencies that cover the sub-THz/THz spectrum. The other challenges include accurate broadband calibration using off-wafer thru, open, short, reflect, and load standards. This challenge can be overcome by employing on-wafer thru-reflect-load (TRL) standards that provide accurate broadband calibration [6], [113]. Similarly, power measurements can be carried out using a PNAx or vector signal generator (VSG) as an input power source, both of which utilize frequency extenders. Power sensor PM5 from the VDI is widely known to measure the output power with a dynamic range of −30 dBm to 25 dBm, as shown in Fig. 32(c).

Furthermore, one of the complex measurements includes the modulation performance characterization. This necessitates synchronization between the signal source and sink components. Other measurement equipment used in addition to the signal source/sink is an arbitrary waveform generator (AWG) or a carrier board with pseudorandom binary sequence (PRBS) generators. The oscilloscope has been employed to capture the modulated waveform, plot BER, and eye diagram to analyze communication quality as shown in Fig. 32(d). The above-mentioned setups have been illustrated for the wired characterization of the communication system.

Moreover, wireless measurement plays a vital role in characterizing the performance of antennas and the overall quality of communication links. Fig. 33(a) shows a typical setup for measuring the far-field radiation characteristics of an antenna module. The standard gain horn antenna was employed at the receiving end to calculate the gain/efficiency/radiation of the antenna under test (AUT). It is challenging to measure the AUT performance accurately because of reflections from closely spaced metals, which can be mitigated using absorbers.

A spatial power combining measurement is depicted in Fig. 33(b). It includes an RF power splitter to distribute the signal to be fed from the right and left sides of the chip/antenna equally and captures the spatially combined signal using a horn antenna at the receiving end. As discussed earlier, the basic specifications of measurement equipment

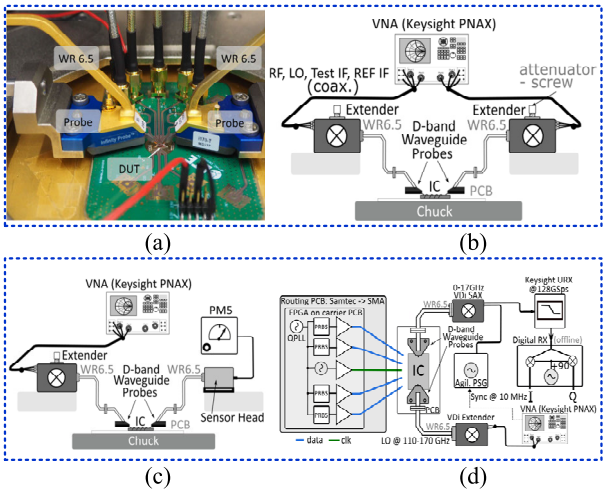


FIGURE 32. (a) WR 6.5 waveguide probes for on-wafer circuit characterization, measurement setups for (b) S-Parameter, (c) Power measurements, and (d) Modulation performance measurements [6].

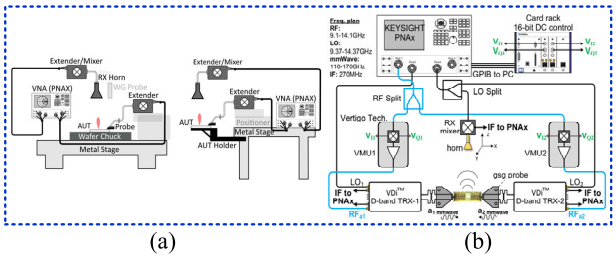


FIGURE 33. Wireless measurement setups, (a) Far-field radiation measurements [6], (b) Spatial power-combining measurements [24].

are limited to cover the *D-band* spectrum, which necessitates the use of frequency/power extenders. These extenders employ non-linear components for frequency up-conversion, which can affect the measurement accuracy and require careful calibration. While integrating test equipment from multiple vendors, compatibility issues sometimes arise that require careful consideration.

VIII. CONCLUSION

This review article presents essential literature for overcoming the challenges associated with realizing next-generation communication systems. By outlining the significance of the sub-THz frequency spectrum, it presents the key performance indicators indispensable from 1G to 6G communication technologies. To understand system-level challenges, a link budget analysis, comprising low to mid-spectral-efficient modulation schemes, is performed which distinguishes the characteristics of each working block of communication radio, specifically for *D*-band applications. The semiconductor device technology plays a vital role in achieving the link-budget specifications, thus, the existing semiconductor technologies along with research opportunities are also discussed in the context of radio transmitters. This is followed by an in-depth analysis of the current SOTA in transmitter building blocks. The circuit-level study reveals the significant take-ons, which include (i) the III-V PA has the potential to deliver high *PAE* among the existing technologies, (ii) the frequency multiplier is an ideal LO signal source owing to its low *PN* and conversion loss when compared with PLLs and VCOs, (iii) the DD modulators tends to be an excellent choice, with its compact, less complex, energy-efficient and high-data-rate architectures, essential for *D*-band scalable phased arrays. DD modulators integrate *bits-on-RF*, which controls the PS and EQ through binary data sequences while eliminating the need for high-power DACs and high-resolution ADCs. Likewise, signal generation, amplification and modulation blocks, and signal radiation using an antenna array require special attention owing to the circuit-antenna comparable size for *D*-band wavelength. Thus, antenna substrate and circuit-antenna integration play critical roles in defining the (a) bandwidth, (b) radiation efficiency, and (c) packaging interconnect loss, critical for communication link performance. This review explores various SOTA antenna designs and integration methods (e.g., AoC, AoB, and AiP) and reveals that the AiP/AoB demonstrate tolerable performance regarding bandwidth and radiation efficiency. Owing to the (a) large *PAE* requirements -that can be achieved by III-V *PA*s, (b) cost reductions -which can be accomplished by commercial Silicon RFICs, and (c) high radiation efficiency -by using AiP solutions, heterogenous-integration gained attention in the past decade. This review presents SOTA in fully packaged *D*-band phased arrays equipped with homogenous and heterogeneous integration architectures, revealing that packaging trends favor heterogeneous integration because it could yield the benefits of the abovementioned semiconductor devices and packaging technologies. The last but essential aspect of sub-THz communication system design is physical verification through measurements. This necessitates the integration of non-linear frequency extenders alongside the base models of the equipment; thus, careful calibration is required. Careful considerations of the aspects outlined above are expected to fuel the efficient designs of *D*-band transmitter architectures and heterogeneously integrated solutions in the near future.

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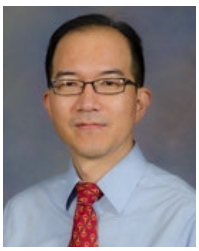

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