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Detailed low frequency noise assessment on GAA NW n-channel FETs

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Detailed low frequency noise assessment on n-channel GAA NW FETs

Abstract

Low frequency noise (LFN) studies are carried out on n-channel gate all around nanowire (GAA NW) FETs. Measurements both as a function of applied polarisation at fixed temperature and conserving the same drain current bias points as a function of temperature are performed, to investigate the predominant flicker noise fluctuation mechanism and to execute low frequency noise spectroscopy allowing to identify the active traps in the depletion area of the devices. The good correlation between the normalized drain current noise S_{Id} / I_d^2 and the transconductance to drain current ratio squared $(g_m/I_d)^2$ enables to establish that the $1/f$ noise is related to the carrier number fluctuations mechanisms for all investigated temperatures. The study of the generation recombination (GR) noise as a function of temperature confirms the presence of a GR component for which the characteristic frequency is independent on the applied voltage and present variation with the temperature, suggesting that they are related to active traps located in the Si film. Active traps related to hydrogen and divacancies were identified.

I. Introduction

It is widely known that nanowire transistors are the best candidates instead of FinFETs for the ultimate scaled CMOS technological nodes. This investigation enrols in the framework of low frequency noise studies performed in order to investigate the performances of GAA NW FETs which are designed using the same technological steps as for superlattice I/O FinFETs [1].

The tested devices are from wafer D19 of AL508339 lot fabricated at imec, presenting four lateral nanowires with a fixed width of 40 nm and having a metal gate length of 250 nm. The gate oxide stack has an equivalent oxide thickness (EOT) of 5.6 nm (2 nm high-k dielectric (HfSiO) on top of a 5 nm SiO_2 interfacial layer). More details of the process fabrication steps of the transistors is given in [1].

The LFN measurements are performed as a function of the applied gate voltage for each fixed temperature in the 300 K – 340 K range, using a temperature step of 5 K, by keeping the same drain current biases. Details on the LFN noise set-up may be found in [2].

The flicker noise level evolution as a function of the gate bias enables to determine the 1/*f* fluctuation mechanism. The obtained results evidenced that carrier number fluctuations completely explain the 1/*f* behaviour allowing to get information on the quality of the insulator-silicon interface of the devices.

The evolution of the characteristic frequency of the GR component observed in the total noise with the applied polarisation at fixed temperature and with temperature at fixed drain current bias indicates the presence of traps located in the depletion area, giving information on the quality of the depleted Si nanowire. The existence of two processing-induced types of active traps, related to hydrogen and divacancies, has been highlighted.

II. Methodology

The following equation models the input-referred power spectral density [2]:

$$S_{v_g}(f) = \frac{S_{id}}{{g_m}^2} = W_n + \frac{K_f}{f} + \sum_{i=1}^{N} S_{GR_i} = W_n + \frac{K_f}{f} + \sum_{i=1}^{N} \frac{A_i}{1+\left(\frac{f}{f_{0i}}\right)^2} \qquad (1)$$

in which are considered the contributions of three uncorrelated noise sources : the white noise (W_n), the flicker noise (K_f) and the GR noise contributions (S_{GR}), each GR noise contribution being characterized by its characteristic frequency (f_{0i}) and its plateau (A_i).

The methodology to estimate the LFN parameters assuming Equation 1 is the same as described in [3]. An example of LFN noise parameter extraction is given in Figure 1a and b.

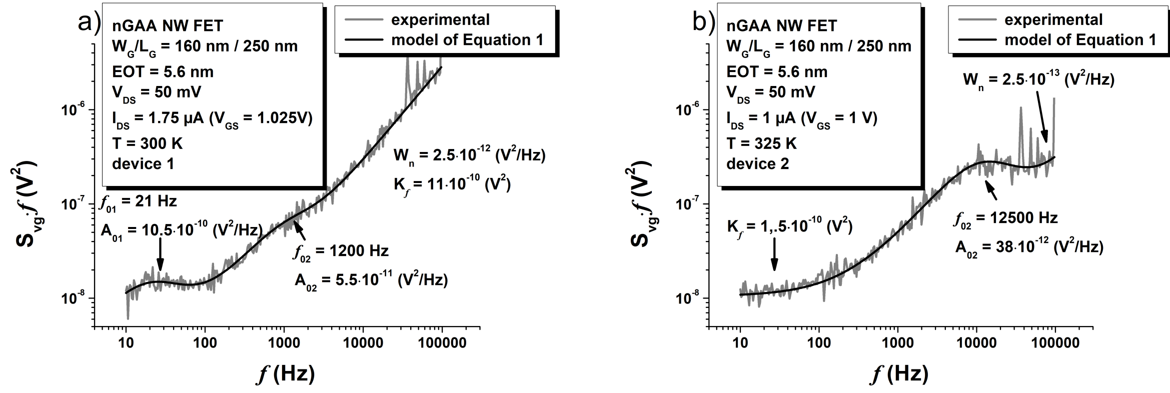

Figure 1. Noise measurement and model using Equation 1: additional to flicker noise and white noise, two GR contributions are considered in a), while only one GR is necessary in b) to obtain the best agreement between measurements and model.

The study of the evolution of the $1/f$ noise level K_f (equal to the $1/f$ noise level at 1 Hz) with the applied polarization at fixed temperature allows to determine the dominatant fluctuation mechanism: mobility fluctuations [4], carrier number fluctuations or carrier number fluctuations correlated to mobility fluctuations [5]. The GR contributions are related to the presence of active traps. The analysis of GR parameters, in particular the behaviour of the characteristic relaxation time constant ($\tau_{0i} = 1/(2\pi f_{0i})$) with the applied gate bias allows to localize these traps [6].

As the Fermi level changes with the applied gate bias, a maximum GR noise is produced when the Fermi level and the traps level cross in the bandgap. Since the energy level of a point defect located in the depletion region is discrete and unique, and when the applied gate bias changes, the Fermi level scans the same trap, but for increasing depth in the depletion zone [6,7]. The characteristic time constant of the GR noise associated with this trap will not change with gate bias variation but should only vary with temperature [6,7]. To keep a quasi-constant Fermi level over the targeted temperature range implies to operate at the same constant drain current polarization. To perform low frequency noise spectroscopy consist of keeping a constant drain current polarization by adjusting the gate voltage at a fixed drain bias for each different temperature.

The temperature variation of the τ_{0i} related to traps located in the depleted area permits to construct an Arrhenius diagram [6,7]:

$$\ln\left(\tau_i T^2\right) = \frac{\Delta E}{k_B T} + \ln\left(\frac{const.}{\sigma_n}\right) \tag{2}$$

where T is the temperature and k_B is the Boltzmann constant.

A least-squares linear fit with the experimental data permits to estimate the energy difference between the conduction band energy and the trap energy ($\Delta E = E_C - E_T$) (from the slope) and the capture cross-section σ_n (from the y-intercept). Furthermore, by comparing the obtained ΔE and σ_n with those reported from Deep-Level Transient Spectroscopy (DLTS) studies, the physical nature of the identified traps may be established.

Each generation-recombination contribution is characterized by a plateau level A_i and a time constant τ_{0i} [4-6]:

$$A_i = \frac{q^2 N_{eff}}{WLC_{ox}^2}\tau_{0i} = \frac{q^2 B W_d N_T}{WLC_{ox}^2}\tau_{0i} \tag{3}$$

where q is the absolute electron charge, W and L are the effective channel width and length, C_{ox} is the gate capacitance per unit of area, W_d is the silicon depletion depth, and N_{eff} and N_T are the surface and the volume trap density.

Equation 3 clearly indicates that a linear dependency between the GR plateau (A_i) and the GR characteristic relaxation time constant (τ_{0i}) should exist. As a consequence, the A_i versus τ_{0i} plot may additionally be used in order to confirm the trap identification. Moreover, Equation 3, from the slope of A_i versus τ_{0i}, permits to estimate without any other assumption the surface trap density (N_{eff}). However, GR noise related to traps in the depletion zone being a volume phenomenon, generally a volume trap density (N_T) value is expected to be reported. The common way to calculate N_T is to take into account in Equation 3 the theoretical value of the B coefficient estimated to be 1/3 (named Method I). A second method consists to use the maximum of the GR contribution at fixed frequency $S_{GR}(f_0,T)$ versus the temperature. $S_{GR}(f_0,T)$ for traps located in the depletion zone depend on $\tau_{0i}(T)/\{1 + [2\pi f\tau_{0i}(T)]^2\}$ (see Equations 1 and 3). For a given frequency f_0, if $2\pi f_0\tau_{0i}(T) \gg 1$, $S_{GR}(f_0,T) \propto \tau_{0i}(T)]^{-1}$, and $S_{GR}(f_0,T)$ will increase with increasing temperature as τ_{0i} decreases. If $2\pi f_0\tau_{0i}(T) \ll 1$, then $S_{GR}(f_0,T) \propto \tau_{0i}(T)$ and $S_{GR}(f_0,T)$ will decrease with increasing temperature [6]. The expression of N_T using this method (named Method II) is given by [6]:

$$N_T = \frac{12\pi\left[S_{GR_i}\left(f_0,T\right)\right]_{max} f_0 C_{ox}^2 WL}{q^2 W_d} \tag{4}$$

By comparing the N_T values obtained using Method 1 with the N_{eff}, an experimental B coefficient may be calculated, expressed as

$$B_{\exp} = \frac{N_{eff}}{N_T W_d} \tag{5}$$

Unphysical values of the estimated B_{exp} were already reported in particular for multi-gate devices (e.g. FinFETs) [8] suggesting that the utilization of N_T as a figure of merit may be not accurate.

III. Results and discussion

Typical normalized drain current noise levels (S_{id}/Id^2) are plotted in Figure 2 as a function of the applied current polarisation, for all investigated devices (named device 1, device 2 and device 3, respectively) at room temperature operation.

For all devices it may be noticed that the S_{id}/Id^2 does not agree with a $1/I_d$ variation with the applied gate polarisation, while a good agreement may be observed between the S_{id}/Id^2 and the transconductance to drain current ratio squared $(g_m/I_d)^2$ behaviours. This clearly indicates that the flicker noise responsible mechanism is the carrier number fluctuations. Furthermore, this allow to estimate from the flatband noise the interface traps density [5]. The obtained values between 1.24 up to $2.7 \cdot 10^{17}$ $cm^{-3}eV^{-1}$ indicate a good quality of the Si/dielectric interface for the studied devices.

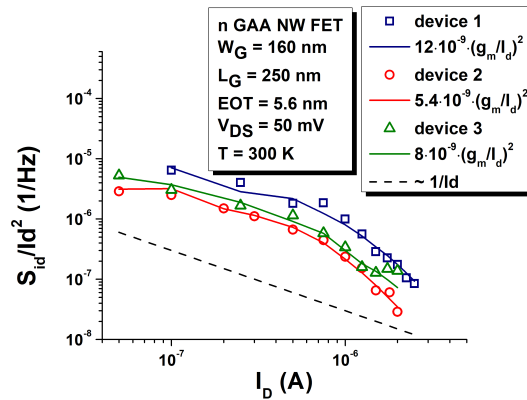

Figure 2. Normalized drain current noise as a function of the current polarisation. Good agreement is observed between the S_{id}/Id^2 and the transconductance to drain current ratio squared $(g_m/I_d)^2$ behaviours.

The noise measurements at fixed temperature as a function of the applied gate bias permit to plot the extracted characteristic frequency of each GR noise contribution. As the same bias points are kept when the noise measurements are made at different temperatures, Figure 3 represents the estimated f_{0i} as a function of the applied drain current at room temperature operation for device 1. It may be observed that the group of frequencies represented using "square" symbols present an important variation with the applied bias: from around 27 Hz up to around 3.8 kHz; the "group" of frequencies represented using "circle" symbols present a slight variation with the applied bias: from around 1.2 kHz up to around 1.75 kHz; while the "triangle" group is quasi-independent on the applied bias: around 20 Hz.

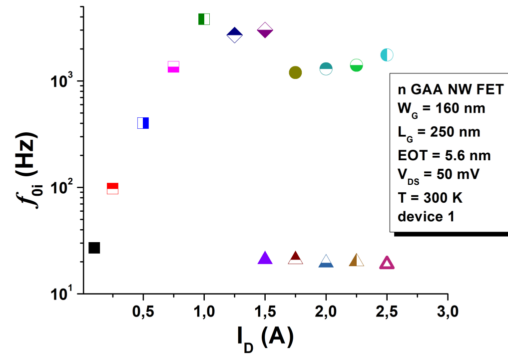

Figure 3. Estimated characteristic frequencies of GR contribution as a function of the applied drain current at 300 K.

In order to have a better view, for each group of characteristic frequencies, of the observed GR contribution to the noise spectra the corresponding characteristic relaxation time constant (τ_{0i}) as a function of the corresponding applied gate voltage bias is plotted separately in Figure 4. It may be observed that for the "square" symbols data the τ_{0i} present an exponential behaviour with the applied gate polarisation $\tau_{0i} \sim \exp(\beta \cdot V_{Gi})$, with an exponential factor β of about -35 V^{-1}, suggesting that these GR contributions may be related to the traps located at the Si/dielectric interface. For the "circle" symbols data β is found to be around -3.7 V^{-1}. This small value of β indicates that these GR contributions are most likely related to traps located in the depleted Si film near the Si/dielectric interface [6,9]. As the "triangle" symbols data are quasi-independent on the applied bias, this suggests that the corresponding GR contribution originates from traps located in the depleted Si film [6,9].

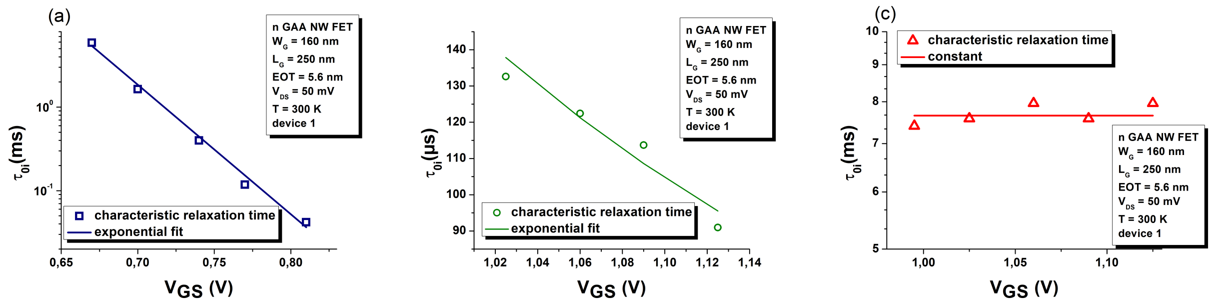

Figure 4. Estimated characteristic relaxation time constants as a function of the applied gate voltage at room temperature a) for "square b) for "circle" and c) for "triangle" symbols group of data.

Further, in this work we focus only on the study of traps located in the depletion zone of the transistors for which the characteristic relaxation time constant does not depend on the applied polarisation. As a consequence, Figure 5 represents the temperature evolution of τ_{0i} corresponding to the "triangle" symbols group of data evidenced at room temperature (from Figure 4c). One may remark that at each fixed temperature, in the range 1.75 μA up to 2.25 μA, τ_{0i} is quasi-constant with the applied drain current polarisation; and at fixed drain current polarisation, τ_{0i} decreases with increasing temperature. This behaviour allows to conclude that this GR contribution is related to traps located in the depletion area (Si film) of the device [6].

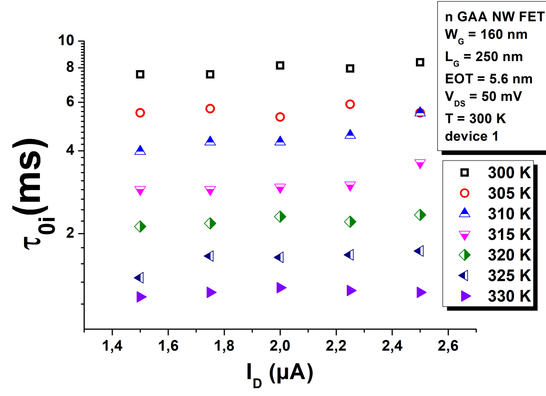

Figure 5. Estimated characteristic frequencies of the GR contribution as a function of the applied drain current at 300 K.

From the temperature evolution of τ_{0i} which is confirmed to be related to traps located in the Si film, the corresponding Arrhenius plots are built up for device 1 and device 2 (Figure 6). No evidence of traps located in the depletion zone of the transistor may be confirmed for device 3.

From the slope and the y-intercept of the Arrhenius diagrams the trap parameters are the following: ΔE of 0.45 eV and σ_n of $1.6\cdot10^{-17}$ cm^2 for the trap identified for device 1 and ΔE of 0.42 eV and σ_n of $6.7\cdot10^{-16}$ cm^2 for the trap identified for device 2, respectively.

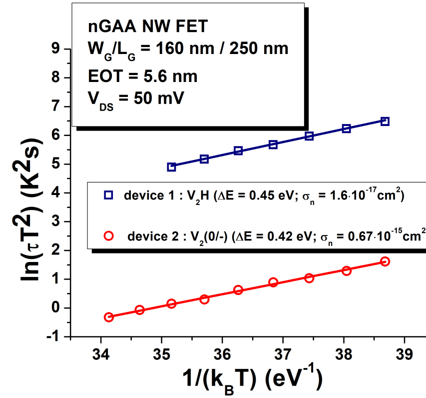

Figure 6. Arrhenius plot constructed using Equation 2 [6,7].

It may be reminded that DLTS measurements report for a divancancy – hydrogen V_2H trap a ΔE of 0.45 eV and σ_n in the 10^{-17} cm^2 range [10, 11], and for a single negatively charged acceptor state (0/-) of the divacancy (V_2) trap a ΔE of 0.42 eV and σ_n in the 10^{-15} cm^2 range [10,12]. As a consequence, the nature of the identified traps is related to V_2H for device 1 and V_2(0/-) for device 2.

The V_2H trap may appear because of the presence of residual hydrogen after annealing, while the V_2(0/-) trap may emerge during an ion implantation process step, and can be explained by the recombination or the evolution to a stable state of unstable defects like Frenkel pairs.

The linear evolution of the GR plateau A_i versus τ_{0i} plotted in Figure 7 additionally confirms the trap identification and allows to estimate the effective trap density (N_{eff}): $3\cdot10^9$ cm^{-2} for the V_2H trap and $1.7\cdot10^{10}$ cm^{-2} for the V_2(0/-) trap, respectively.

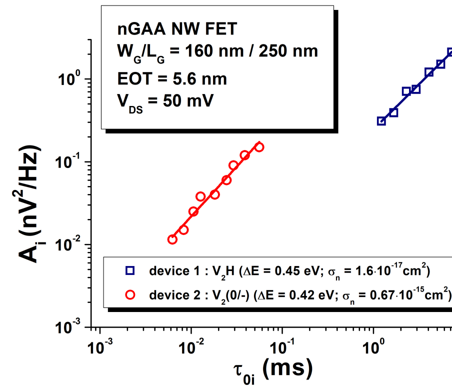

Figure 7. The extracted A_i versus τ_{0i} showing a linear behaviour.

These values are about one decade lower than similar identified traps in the superlattice I/O FinFETs [3], suggesting a better control/quality of the Si film for the studied GAA NW devices.

From the measured $S_{vg}(f_0, T)$, the $S_{GR}(f_0, T)$ may by easily estimated using Equation 1. In Figure 8 the $S_{GR}(f_0, T)$ is plotted for a fixed f_0 versus the temperature for the V_2H trap. f_0 is chosen in order to respect both conditions $2\pi f_0\tau_i(T)$ 1 and $2\pi f_0\tau_i(T) >> 1$. $S_{GR}(f_0, T)$ presents a bell-shaped behaviour (the same trend is observed for the $V_2(0/-)$ trap) so that the effective trap density may be extracted. The estimated B_{exp} is about 0.57 for the V_2H trap and about 0.17 for the $V_2(0/-)$ trap.

This discrepancy compared to the theoretical value of a B coefficient of 1/3 confirms again that the utilization of the volume trap density N_T as a figure of merit may be no longer accurate for traps located in the Si film of multi-gate devices.

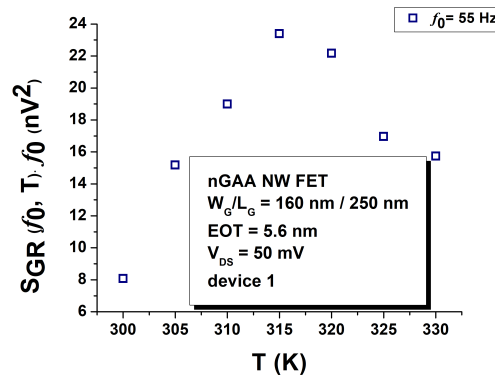

Figure 8. $S_{GR}(f_0, T){\cdot}f_0$ versus the temperature for a V_2H trap.

IV. Conclusion

An in-depth low frequency noise analysis was performed. The carrier number fluctuations are confirmed as the responsible mechanism of the flicker noise.

The evolution of the characteristic relaxation time constant of the generation-recombination components on the total noise as a function of the polarization at fixed temperature and at fixed drain current bias as a function of temperature prove the presence of traps located in the Si film in the investigated n-channel GAA NW FETs. Traps related to divacancy-hydrogen V_2H and the single negatively charged acceptor state (0/-) of the divacancy (V_2) have been identified.

Even for a volume phenomenon, the confirmed discrepancy between the experimental and theoretical B coefficients clearly shows that it is more safe to use the effective trap density instead of the volume trap density as a figure of merit for the traps located in the depletion region of the transistors.

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