HIGH DENSITY AND HIGH BANDWIDTH CHIP-TO-CHIP CONNECTIONS WITH 20µm PITCH FLIP-CHIP ON FAN-OUT WAFER LEVEL PACKAGE

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ABSTRACT
Various Fan-Out Wafer Level Packaging (FO-WLP) approaches have been developed and established over the past years to answer the increasing need for high data rates, wide I/O count and the demand for increase function integration on package.

Imec has been working on a novel 300mm FO-WLP concept that enables 20μm pitch interconnect density: Flip-Chip on FO-WLP. Major challenges and solutions are reported in this paper. Results demonstrate die placement alignment of <3μm, which is suitable to allow stacking for high density interconnect. Connections between the assembled dies were intact before and after molding.

Key words: Fan-Out, Wafer Level Package, Heterogenous Integration, Flip Chip, warpage, die shift, wafer molding, ultra-high density

INTRODUCTION
The electronic industry is approaching the limit of traditional CMOS scaling therefore requiring further innovations in assembly and packaging. In this regard, packaging transcends its traditional function of providing electronic connections and protecting the chip against mechanical and environmental stresses : it becomes an integration platform enabling functional diversification through heterogeneous integration to meet the market demands for more functionality, increase I/O count, smaller/thinner form and cost reduction. FO-WLP approaches have been developed to answer these demands [1-3].
There are two basic process flows for Fan-Out Wafer Level Package (FO-WLP): the one that encountered the "Mold first" and the other that encountered the "RDL first". In the "mold first" approach, large die shift occurring during or after the wafer overmolding that limits the scalability of the bump pitch interconnect [4,7]. This is posing a great challenge for RDL layer lithography whilst the reconstructed substrates are distorted. On the other hand, the "RDL first" approach is limited by the line and space resolution achievable by organic RDL [5].

To address these challenges, imec has been working on a novel 300mm FO-WLP concept that enables 20μm pitch interconnect density. Contrary to "mold first" approach where interconnects are built after wafer overmolding, hence susceptible to die shift, in the proposed approach the dies are overmolded after the formation of the chip to chip link through an interconnecting bridge chip. In this case, the critical assembly step with tight alignment tolerance is formed prior to molding.
By combining imec's approach with the development of novel mold materials, it has been possible to demonstrate wafer bow below 500μm after molding on silicon substrate and die shift as low as average of 10μm across the whole 300mm wafer [14]. Such value is orders of magnitude below reported in literature [7-9,10] and have major implications on the processing of overmolded substrates as they can now access more standard silicon BEOL processing equipment and do not require dedicated equipment due to wafer bow. Another very important assessment in this development is that the bump to bump connection remained intact after molding.

This paper introduces the novel Fan-Out concept for ultra-high chip-to-chip interconnect density with 20μm bump pitch. Furthermore, the results of initial build along with challenges and solutions are presented.

NOVEL FAN-OUT CONCEPT
Design and Structure
Figure 1 shows the Fan-Out concept/architecture for ultra-high chip-to-chip interconnect density with 20μm pitch. There are seven (7) different chip components: wide I/O DRAM, flash memory, logic, two high density Through Package Vias (TPVs), and the two Si bridges (high density fan-out interconnects chip-to-TSV). The TPV and Si bridge connecting the wide I/O DRAM to Logic with 20μm bump pitch are the key components to achieve ultra-high density interconnect.



Figure 1. Novel Fan-Out Concept for Ultra-High Chip-to-Chip Interconnect with 20μm pitch

In the actual test vehicle, used to obtain practical learnings regarding the assembly process of this concept, the wide I/O DRAM, Flash Memory and Logic chips to be used are not fully functional chip. They are passive components that will be used to test the electrical continuity between the bump connections.
The TPVs are Si dies with 5x50μm TSV and bumps of 40μm pitch on the front and back side of the die. The Si bridges are 20-30μm thin with bumps of 40μm and 20μm pitch: 40μm pitch bumps are attached to TPV side and right side of Logic die. The 20μm pitch bumps are attached to the left side of logic die.
The mimic memory dies contain one metal layer and bumps with 40µm pitch. "Memory' dies are 50µm thin. The mimic logic dies contain one metal layer, 50μm tall Cu pillars, and bumps of 40μm pitch on the right side and 20μm pitch on the left side. These dies are 55μm thin.
The total thickness of the package body (excluding solder balls) is 0.3-0.4mm.
This platform can be used more broadly for high performance computing system applications, wherein partition is integrated in bottom FO-WLP with TPV, interconnect bridges, front and backside RDL. On top can be high bandwidth wide I/O memory flip-chip stacked on FO-WLP, compute and optical communication blocks.

Assembly Process Flow

The proposed assembly process flow is shown in Figure 2. The first step (1) is to do pre-bond test on individual chips followed by (2) placing the TPV and logic dies on Si carrier coated with Temporary Bond Material (TBM). Step (3) is stacking of Si bridge onto the TPV and continuity test after Si bridge attach, (4) wafer level compression molding, grinding to expose the Cu pillar, and continuity test after molding by probing on the pillars. In step number (5) the thinned reconstructed wafer is flipped to second carrier, the first carrier is removed and continuity test is performed by probing on the bumps. Flip-chip assembly of the memory dies is done in step (6), followed by (7) second wafer level molding, and (8) removal of the carrier and final test. For in house assembly, the final assembly test can be done by probing on the Cu pillars at wafer level. This makes the solder ball attach process as an option.
This paper will deal with the following challenges : tilt of TPV and logic dies, pick and place of dies with Cu pillar (logic die), die placement, mold fill under the bridge, and bump to bump connectivity between bridge-TPV-logic.
Apart from processing challenges, there are also material and metrology challenges. One material challenge is to obtain a mold material that can deliver a very low warpage and very small die shift without issues on molding performance. Secondly, a TBM material that can allow good placement and handling of dies on step 2, that is also compatible with the stacking process and allows successful debonding. The interaction between the mold compound and TBM material plays an important role to ensure successful carrier wafer debond.
On the metrology side, it is very challenging to measure the die tilt when TBM is present below the die. Since the TBM material is transparent, a consistent bottom reference is missing. Another challenge is, getting the overlay measurement between the die and the carrier (die shift) before/after mold and after grinding plus delivering the data in a wafer map form.
To address process and material challenges, initial experiments were done focusing mainly on determining the mold compound material to be used, warpage evolution, die tilt and die shift. The results from these experiments are discussed in separate publications [14-16].

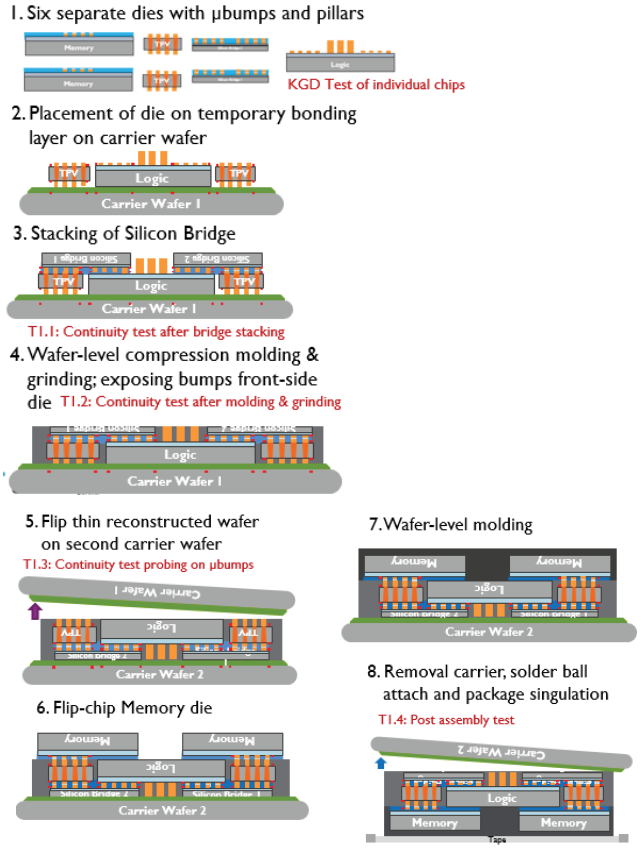


Figure 2. Assembly Process Flow

OVERCOMING CHALLENGES

As previously mentioned, this paper will deal with the following challenges : tilt of TPV and logic dies, pick and place of dies with Cu pillar (logic dies), die placement, and bump to bump connectivity between logic-bridge-TPV.

Tilting of the dies

Illustrated below in Figure 3 is one of the challenges that can be encountered during assembly : die tilt. It was previously observed from initial experiments that there was no tilt on the bottom dies (as reported in [14]). However, this might not be the case for the TPV dies due to the narrow, long and thin size (width : 2mm, length : 7mm, thickness : 50μm). Given the die dimension, tilt calibration/correction was not possible to be performed in the placement/stacking tool. Furthermore, the presence of a transparent TBM layer makes the tilt measurement not straightforward.
To assess whether and when die tilting can be observed, the TPV placement was done with different placement forces : 4.9N, 7.4N, 9.8N and 12.3N. Tilting of the die after placement was measured using a high resolution profiler. Placement and measurement method is shown in Figure 4.

A very small tilt (<<0.5μm) can be observed from the profiler scans even at the maximum placement force (12.3N), shown in Figure 5.

Pick and Place of 'Logic' dies

Shown in Figure 6 is the schematic of the 'logic' die. The presence of Cu pillars on the 'logic' dies make it difficult during pick and place step due to vacuum loss.

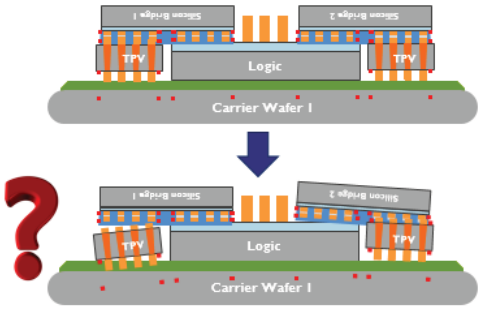


Figure 3. One of the assembly challenges identified : die tilt after die placement and stacking

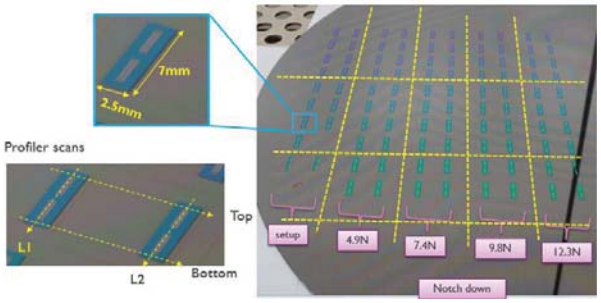


Figure 4. TPV placement with different placement forces and locations of profiler scans

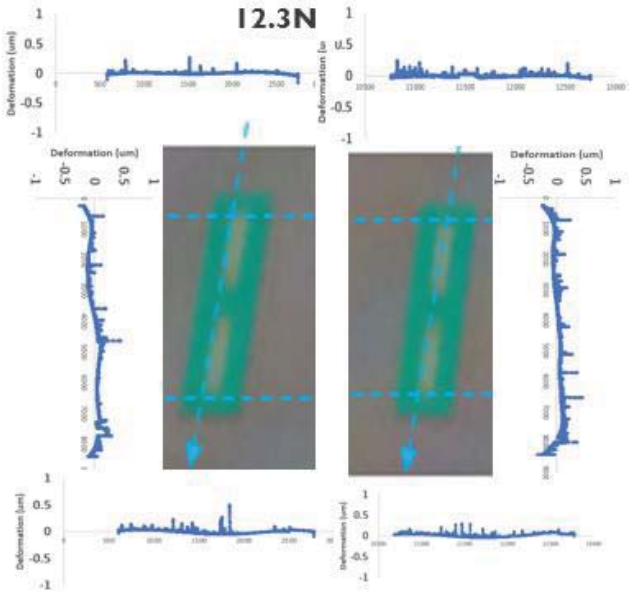


Figure 5. Deformation and tilt data obtained from profiler scan on dies placed at maximum force of 12.3N. Very small deformation and tilt observed (<<5μm).

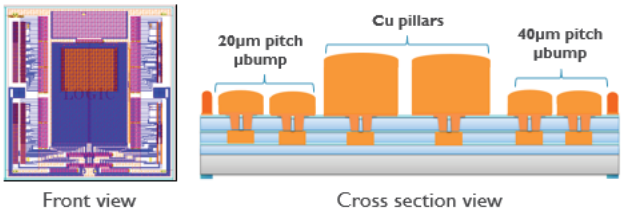


Figure 6. Schematic of 'logic' die : front and cross section view.

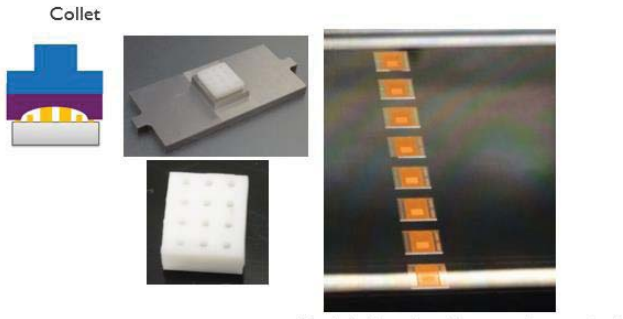


Figure 7. Soft collet used for 'logic' pick and place (left). Photo showing a successful placement of dies (right)

To enable successful pick and place of logic die, a specifically designed soft collet was used (Figure 7). Die placement was done at room temperature, which is an advantage for alignment pattern recognition when aligning the dies on the placement sites of the carrier wafers.

Alignment between 'Logic' and TPV dies

One of the key differentiator and enabler of Imec's ultra-high density interconnect FO-WLP is the accurate placement of the 'logic' and TPV dies followed by thermocompression bonding (TCB) of the bridge connector before wafer level overmolding (Figure 8). Accurate placement was made possible by incorporating alignment marks into the carrier and die designs and use of high accuracy placement & stacking TCB tool.



Figure 8. Achieving high density interconnects in a Fan-Out technology context

Taking into considerations the different contributing factors to misalignment (i.e. alignment marks quality, tool signature placement error, recipe level placement error etc), TPV to 'logic' placement error was given extra attention. This is to ensure that the TPV and Logic are in-sync to allow proper bridge stacking later on. Logic dies were first aligned to the carrier. Overlay data after logic placement is shown in Figure 9. Misalignment is ≤3µm, which is good enough to enable 40μm and 20μm bump pitch stacking.
TPV dies were placed next aligned to the carrier and also aligned to placed logic dies. Figure 10, shows the TPVs (left and right) to logic placement error of ≤3µm, suitable for the targetted bump pitch stacking.

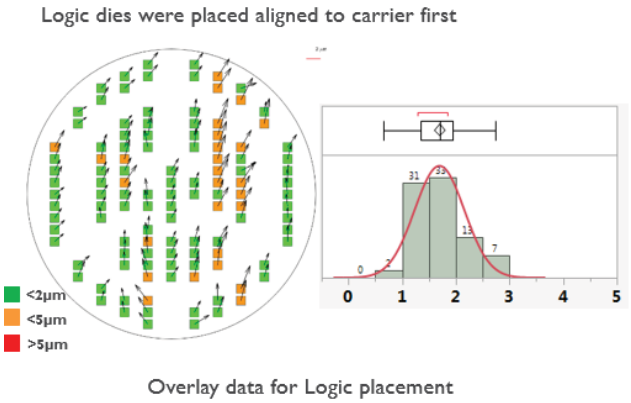


Figure 9. Overlay measurement data after 'logic' dies placement. Placement was done aligned to carrier. Misalignment of ≤3µm was obtained

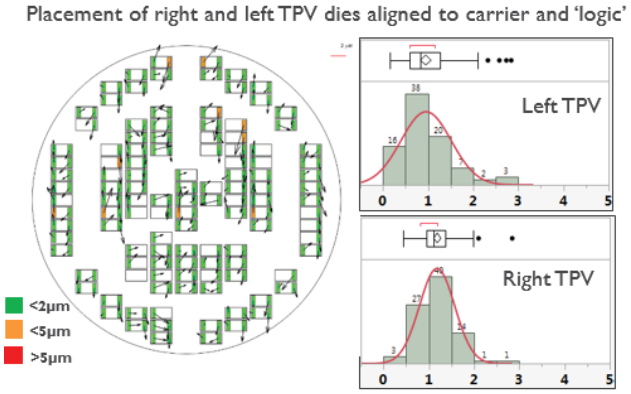


Figure 10. TPV to logic placement error data. Left and right TPV was placed aligned to carrier and to logic die. Both left and right TPV to logic placement error is ≤3µm, which is suitable for 40μm and 20μm bump pitch stacking

Complete mold fill under the silicon bridge

Another identified challenge that can occur is the incomplete mold fill under bridge (figure 11). Note that during molding process the mold material has to fill in a narrow and long 'tunnel' (320µm wide and 7mm long). Scanning acoustic microscope (SAM) inspection and cross sectioning of a few of the assembled units were done to check if there are voids or incomplete mold material filling under the bridge area.

Based from the SAM images (shown in figure 12) and representative cross section (figure 13) results, the area under the bridge is completely filled with mold material.

The mold process parameters have not been changed from baseline parameters. Further study is to be conducted to determine mold process failure point along with different 'tunnel' dimensions.

Bump connection between logic-bridge-TPV

Electrical test for continuity was done after bridge stacking (before molding) and after molding. The latter is to check whether the die shift induced by the molding process damages or breaks the bump connections between TPV-bridge and Logic-bridge. Detailed explanation on test procedures can be found in separate publication [17]. For this initial build, there were six (6) units tested before and after molding. Test schematics and material tested are shown in Figure 14. Test results are shown in Figure 15.

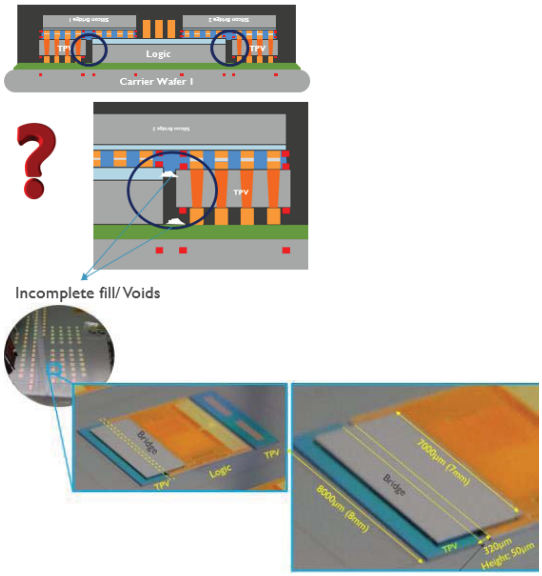


Figure 11. Illustration showing another one of assembly challenges : mold fill in area under the bridge

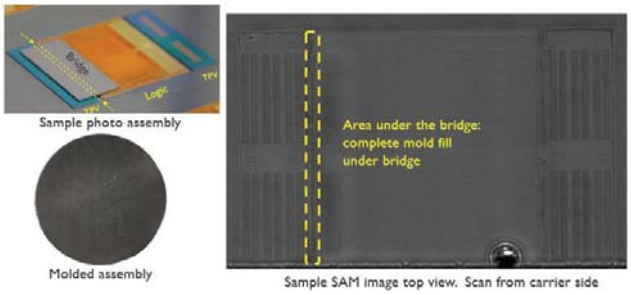


Figure 12. SAM on area under bridge. No voids or incomplete fill of mold material on area under bridge

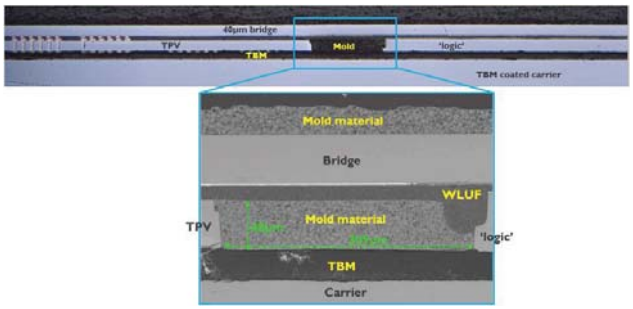


Figure 13. Representative cross sectioned units. All samples cross sectioned and polished indicated that are under the bridge is filled with mold material

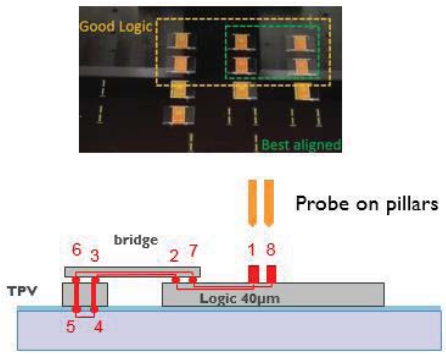


Figure 14. Assembled units tested enclosed in bigger dotted area (top). Test schematics (bottom). Test was done probing on pillars



Figure15. Electrical results before (top) and after (bottom) molding. Left and center tables are kelvin interconnect results. All tables on the right side are daisy chains results. Good bump connectivity before and after molding

From Figure 15, it is shown that prior to molding micro-bump connection between logic-bridge and the bridge itself are good based on the kelvin interconnects (left and center table) and daisy chains (right most table). It is also shown that after molding, the integrity of the connections were maintained.

SUMMARY

Some of the processing, material and metrology challenges of a novel Flip-Chip FOWLP flow are demonstrated in this paper. It is shown that the TPV components are placed on a TBM coated carrier wafer with controlled tilt. Using a soft collet in the pick and place tool allows for successful placement of the Logic die with height variation between the microbump/micropilar structures. Also the relative placement of the TPV and Logic dies on the carrier wafer was well aligned to allow the assembly of the Si bridge. Post mold inspection shows successful filling of the spacing among the different dies. The electrical connections between the assembled dies has been successfully tested both before and after the overmolding process.

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