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Low frequency noise spectroscopy methodology for identifying traps located in the Si film of advanced mosfets

B Cretu[1,*], A Tahiat[1], A Veloso[2] and E Simoen[3]

[1] Normandie Univ, ENSICAEN, UNICAEN, CNRS, GREYC, 14000 Caen, France
[2] Imec Kapeldreef, 75 B-3001 Leuven, Belgium
[3] Solid-State Physics Department, Ghent University, 9000 Gent, Belgium
[*] Author to whom any correspondence should be addressed.

E-mail: bogdan.cretu@ensicaen.fr

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Abstract

The low frequency noise spectroscopy theory for the identification of traps located in the depletion region of a field-effect transistor is reviewed. The hypothesis, which provides the generally accepted expression of the input-referred voltage noise power spectral density related to generation-recombination (GR) phenomena, is questioned. It is evidenced that the GR noise formulation should be revisited in order to be physically consistent and consequently the voltage GR noise plateau should include the impact of the ratio between the dynamic channel resistance and the dynamic total resistance. It is demonstrated that in order to maintain a lower shift of the quasi-Fermi level with the temperature in the strong inversion operation mode it is better to maintain a constant drain current polarization over the temperature range. Considering low frequency noise measurements performed in gate-all-around nano wire FET devices, it is also highlighted that performing only measurements over the temperature at fixed polarization is not enough to be able to properly estimate the identified trap parameters. The measurements for different polarizations at fixed temperature performed for all investigated temperatures are mandatory in order to gain a deeper insight, in particular concerning the 'trapping' GR noise phenomenon.

1. Introduction

The study of low-frequency noise has been proposed in many research works as a non-destructive diagnostic tool to predict the quality and reliability of components [1–20]: it provides information on both process and application optimization, as it allows us to trace the physical sources of fluctuations and to better understand certain physical phenomena present in MOS transistors. The analysis of intrinsic noise at low frequencies may therefore be a mandatory study from the point of view of the intrinsic performance of the transistor and the characterization of the quality of the gate dielectric and of the depletion region of the transistors.

Low frequency noise spectroscopy consists of a function of temperature at fixed biasing of the generation-recombination (GR) noise corresponding to a Lorentzian type of spectrum. This kind of study may be used to obtain information on the nature of the traps responsible for the GR noise [6, 8, 12–20]. The GR noise contribution to the total noise is described by the following expression:

$$S_{\mathrm{GR}}(f) = \frac{A_0}{1+(2\pi f\tau_0)^2} = \frac{A_0}{1+(f/f_0)^2} \tag{1}$$

where $S_{\mathrm{GR}}(f)$ is the noise spectral density of the GR noise, A_0 is the plateau of the GR noise representing the frequency independent part of the GR noise which may be observed for $f \ll f_0 = 1/(2\pi\tau_0)$, f_0 and τ_0 being the characteristic frequency and characteristic relaxation time of the GR noise, respectively.

Firstly, the detailed input-referred noise power spectral density expression related to GR noise ($S_{v,\mathrm{GR}}$) is reviewed [6, 13]. The necessary assumptions are discussed. It is highlighted that, in order to be

physically consistent, the $1/f$ noise formulation [21] expression should include the impact of the ratio between the dynamic channel resistance (r_{ch}) and the dynamic total resistance (r_t) of a MOSFET.

This work will focus only on traps located in the depletion region of the transistor. The necessary methodology steps which ensure that the same type of trap is scanned over the temperature range at a fixed polarization are reviewed. Of course, given the variations of the mobility and of the threshold voltage with temperature, imposing a constant drain current is not equivalent to maintaining a constant gate voltage or a constant gate voltage overdrive. However, using a first-order analytical model, it is demonstrated that in order to keep the quasi-Fermi level shift with temperature as low as possible, it would be preferable to maintain a constant drain current polarization rather than a constant gate voltage or a constant gate voltage overdrive polarization in strong inversion operation mode.

The study of the GR noise parameters as a function of the applied bias at fixed temperature can be used to find the location of the involved traps, i.e. situated in the oxide, at the dielectric/channel interface or in the depletion zone of the transistor. In this work, we focus only on traps located in the depletion zone for which the characteristic relaxation time (τ_0) is independent of the applied gate polarization [6, 12–14]. The evolution of the GR plateau (A_0) with the applied polarization can be used to discriminate whether it is a 'generation' or a 'trapping' GR process [13]. Indeed, in strong inversion operation, an independence of the GR noise plateau with the applied polarization can be used to conclude that it is a 'generation' process, while if the GR noise plateau exhibits a logarithmic dependence on the applied gate voltage one can conclude that it is a 'trapping' GR process [6, 13]. The dependence between the plateau and the characteristic relaxation time of the GR noise provides information on the effective (surface) trap density (N_{eff}). By comparison with the volume trap density N_T estimated using a method presented in [13], information about a geometric coefficient B [6, 13] may be obtained. The independence or the evolution with the applied gate voltage of the B coefficient may additionally confirm whether the identified trap is related to a 'generation' or a 'trapping' GR process [13].

A low-frequency noise spectroscopy methodology is employed to investigate previously studied gate-all-around (GAA) nano wire (NW) FETs from imec [20] over the temperature range 300 K—340 K, with a step of 5 K. They present a nanowire width and height of 10 nm, four nanowires in parallel giving a total width of 160 nm, a metal gate length of 250 nm and an equivalent oxide thickness (EOT) of 5.6 nm. Details on the process fabrication process may be found in [22]. It is evidenced that the identified traps, the divacancy-hydrogen V_2H and the single negatively charged acceptor state (0/−) of the divacancy V_2 are related to 'trapping' GR process.

The DC and low frequency noise measurements were performed at wafer level using a TTP4 probe station coupled with a Lakeshore 336 temperature controller. The DC measurements are performed using an Agilent 4156B semiconductor parameter analyzer. The noise measurement set-up consists of an I to V converter, a low noise voltage amplifier having a bandwidth of 200 kHz and a HP3562A spectral analyzer which is used to obtain the noise spectral density from 1 Hz to 100 kHz. A detailed description of the noise setup may be found in [23]. Finally, the noise spectral density is calculated at the input of the device by dividing the measured noise voltage by the square of the measured voltage gain between the gate and the output, canceling the setup bandwidth limitation.

2. Theory—reminder and discussion

For GR phenomena, the spectral density of carrier number fluctuation δS_N for traps of an energy level E_T and of volume density N_T, having a unique characteristic relaxation time τ_0 and independent of z (depth) in an elementary surface δS, is described by [24, 25]:

$$\delta S_N(f) = N_T(E_T) f_t(E_T)\left[1 - f_t(E_T)\right] \frac{4\tau_0}{1 + (2\pi f \tau_0)^2} \delta E_T \delta S \tag{2}$$

where $f_t(E_T)$ is the Fermi–Dirac probability function defined as:

$$f_t(E_T) = \frac{1}{1 + e^{\frac{E_T - E_F}{k_B T}}} \tag{3}$$

and $f_t(E_T)\left[1 - f_t(E_T)\right]$ expresses that the traps that contribute to the GR noise are those located energetically close to the Fermi energy level E_F, k_B being the Boltzmann constant and T the temperature. By integrating (2) one obtains [13]:

$$S_N(f) = \frac{\tau_0}{1 + (2\pi f \tau_0)^2} N_{eff} WL \tag{4}$$

where W and L represent the effective channel width and length. If the traps are located at the dielectric/channel interface $N_{\text{eff}} = 4k_BTN_{it}$ (N_{it} being the interface traps density expressed in $\text{cm}^{-2}\text{eV}^{-1}$), whereas, if the traps are located in the depletion layer of the transistor, $N_{\text{eff}} = N_T W_D B$. W_D represents the depletion thickness and B is a geometrical factor. B is equal to 1/3 for a 'generation' GR process and lower than 1 for a 'trapping' GR process [13].

Based on [26], it may be assumed that:

$$\frac{S_N}{N^2} = \frac{S_{i,\text{GR}}}{{I_D}^2} \tag{5}$$

where N is the total number of electrons in the channel and I_D is the drain current. Hence, one obtains for the GR current noise power spectral density:

$$S_{i,\text{GR}}(f) = \frac{q^2 N_{\text{eff}}\tau_0}{WLC_{ox}^2}\frac{{I_D}^2}{(Q_i/C_{ox})^2}\frac{1}{1+(2\pi f\tau_0)^2} \tag{6}$$

where Q_i is the inversion charge density and C_{ox} is the gate capacitance per unit of area. Consequently, the input referred to as GR voltage noise power spectral density becomes:

$$S_{v,\text{GR}}(f) = \frac{q^2 N_{\text{eff}}\tau_0}{WLC_{ox}^2}\frac{{I_D}^2}{(g_m)^2(Q_i/C_{ox})^2}\frac{1}{1+(2\pi f\tau_0)^2} \tag{7}$$

g_m being the device transconductance.

However, the generally assumed expression of the GR voltage noise power spectral density may be expressed as [13]

$$S_{v,\text{GR}}(f) = \frac{q^2 N_{\text{eff}}\tau_0}{WLC_{ox}^2}\frac{1}{1+(2\pi f\tau_0)^2}. \tag{8}$$

It is obvious that in order to obtain (8) in linear operation, it was assumed in the first approximation:

$$g_m = \frac{\partial I_D}{\partial V_{\text{GS}}}\Big|_{V_{\text{DS}}=\text{const}} = \frac{\partial\left(\frac{W}{L}\mu_{\text{eff}}Q_iV_{\text{DS}}\right)}{\partial V_{\text{GS}}}\Big|_{V_{\text{DS}}=\text{const}} = \frac{I_D}{(Q_i/C_{ox})} \tag{9}$$

where μ_{eff} is the effective mobility and V_{DS} is the drain-to-source applied voltage. Knowing that in linear operation the transconductance may be expressed as [21, 27]:

$$g_m = \frac{WV_{\text{DS}}}{L}\frac{C_{ox}C_i}{C_{ox}+C_d+C_{it}+C_i}\frac{\partial(\mu_{\text{eff}}Q_i)}{\partial Q_i} \tag{10}$$

where C_d, C_{it} and C_i are the depletion, interface and inversion charge capacitances per unit of area, by identification with (10), the approximation of (9) assume that:

$$\frac{C_i}{C_{ox}+C_d+C_{it}+C_i}\frac{\partial(\mu_{\text{eff}}Q_i)}{\partial Q_i} = \mu_{\text{eff}}. \tag{11}$$

Let us consider the generally assumed mobility law expressed as below [28]:

$$\mu_{\text{eff}} = \frac{\mu_0}{1+\theta_1 Q_i/C_{ox}+\theta_2 {Q_i}^2/{C_{ox}}^2} \tag{12}$$

where μ_0 is the low field mobility and θ_1 and θ_2 are the first and the second mobility attenuation coefficients.

In weak inversion, as $\mu_{\text{eff}} = \mu_0$, the approximation in (11) assumes that:

$$C_{ox}+C_d+C_{it} = 0. \tag{13}$$

While in strong inversion, as $C_i \gg C_{ox} + C_d + C_{it}$, the approximation in (11) assumes that

$$\frac{\partial\mu_{\text{eff}}}{\partial Q_i} = 0. \tag{14}$$

Both (13) and (14) assumptions are unphysical.

Moreover, the GR noise fluctuations are intrinsic, channel-related fluctuations. In order to calculate the total output current fluctuations, if the linear operation region is considered, the fluctuations may be calculated directly from the variations of the channel (R_{ch}) and total resistance (R_t). As $R_t = R_{ch} + R_{access}$, where R_{access} represents the access resistances, it is obvious that $\delta R_t = \delta R_{ch} + \delta R_{access}$, and this is independent of the origin of the fluctuations. Assuming that the channel and the access resistance noise sources are uncorrelated, let us consider for simplicity that only the channel resistance is noisy and that the access resistances are noiseless. Hence:

$$\delta R_t = \delta R_{ch}. \tag{15}$$

The drain current fluctuations may be evaluated as:

$$\delta I_D = \delta\left(\frac{V_{DS}}{R_t}\right) = \frac{R_t \delta V_{DS} - V_{DS}\delta R_t}{{R_t}^2} = -\frac{V_{DS}\delta R_t}{{R_t}^2}. \tag{16}$$

In (16) it was considered that $\delta V_{DS} = 0$. Further, the channel fluctuations may be calculated as

$$\delta I_{ch} = \delta\left(\frac{V_{ds}}{R_{ch}}\right) = \frac{R_{ch}\delta V_{ds} - V_{ds}\delta R_{ch}}{{R_{ch}}^2} \tag{17}$$

where V_{ds} is the voltage across the channel $V_{ds} = V_{DS} - I_D R_{access}$. As $\delta I_D \neq 0$, the voltage across the channel fluctuation is not equal to zero but as $\delta V_{ds} = -R_{access}\delta I_D$. Assuming (15) and (16), (17) becomes:

$$\delta I_{ch} = \frac{-R_{ch}R_{access}\delta I_D - V_{ds}\delta R_{ch}}{{R_{ch}}^2} = \frac{-R_{ch}R_{access}\delta I_D + \frac{R_{ch}}{R_t}V_{DS}\frac{{R_t}^2}{V_{DS}}\delta I_D}{{R_{ch}}^2} = R_{ch}\frac{-R_{access} + R_t}{{R_{ch}}^2}\delta I_D = \delta I_D. \tag{18}$$

Assuming $\delta I_D \neq 0$ it results that $\delta V_{ds} \neq 0$ and $\delta I_{ch} = \delta I_D$. As it is about an active device (i.e. current generator), at fixed gate voltage the channel fluctuations will indirectly lead to voltage across the channel fluctuation $\delta V_{ds} \neq 0$ [10, 29, 30]. Of course, if in (17) it is considered that $\delta V_{ds} = 0$, then δI_{ch} will read:

$$\delta I_{ch} = \frac{R_t}{R_{ch}}\delta I_D. \tag{19}$$

Using Kirchhoff's law in the channel-to-source contact (s) or channel-to-drain contact (d) it may be derived, using the strategies of figure 6 of [10] or figure 3–5 of [29], assuming noise-free access resistances; then, the output total current fluctuations may be expressed as:

$$\delta i_t = \delta i_{ch} + \frac{\delta V_{ds}}{R_{ch}} = \delta i_{ch} + \frac{\delta\left(V_{DS} - i_t R_{access}\right)}{R_{ch}} = \delta i_{ch} - \frac{R_{access}}{R_{ch}}\delta i_t. \tag{20}$$

Hence:

$$\delta i_t = \frac{R_{ch}}{R_{ch} + R_{access}}\,\delta i_{ch} = \frac{R_{ch}}{R_t}\,\delta i_{ch}. \tag{21}$$

Assuming that δi_t represents the drain current fluctuation δI_D, by comparing (19) with (21), it may be observed that employing the strategy of [10, 29] gives the same result as when V_{ds} was considered constant (i.e. $\delta V_{ds} = 0$). This is a contradictory result because it is shown that the same result for the output total current fluctuations (δi_t) is obtained whether or not δV_{ds} is equal to zero.

However, it may be suggested that this strategy [10, 30] already considers that $\delta I_{ch} = \delta I_D$ as evidenced by (18). This hypothesis agrees with the small signal equivalent circuit of a MOSFET, as shown in [10, 29, 30], where the $S_{i,ch}$ corresponding to δI_{ch} is in parallel with a current noise generator $g_m V_{Gs}$ (g_m being the measured/extrinsic transconductance) instead of $g_{m,i}V_{Gs}$ ($g_{m,i}$ being the intrinsic transconductance).

It may also be observed that (5) considers that the $\delta V_{ds} = 0$ and then it is not physical if the channel is considered as a current source generator. In other words, (5) treats the channel as a piece of semiconductor equivalent to a passive component, while the channel is part of an active component.

Hence, considering the previous suggestion, or following a similar approach as in [21], and along the same way as in [31] considering the Matthiessen rule, it may be assumed that μ_{eff} should read the change of Q_i when the applied gate voltage changes, but for each polarization the GR fluctuation does

not induce a variation of the intrinsic effective mobility. Therefore, the expression of the GR voltage noise power spectral density may be derived as:

$$S_{v,GR}(f) = \frac{{R_{ch}}^2}{{R_t}^2}\frac{q^2 N_{\text{eff}}\tau_0}{WLC_{ox}^2}\frac{1}{1+(2\pi f\tau_0)^2}. \tag{22}$$

In (22) it was already assumed that, as demonstrated in [21] for the linear operation regime, the dynamic channel resistance to the dynamic total resistance ratio is equal to the channel resistance to the total resistance ratio.

However, if it is not assumed that for each polarization the GR fluctuation does not induce variation of the intrinsic effective mobility, the expression of the GR voltage noise power density will read:

$$S_{v,GR}(f) = \frac{{R_{ch}}^2}{{R_t}^2}\frac{{I_D}^2}{(g_m)^2(Q_i/C_{ox})^2}\frac{q^2 N_{\text{eff}}\tau_0}{WLC_{ox}^2}\frac{1}{1+(2\pi f\tau_0)^2}. \tag{23}$$

Using analytical expressions in linear operation of I_D and g_m (e.g. (2) and (5) of [32], which are valid from weak to strong inversion) (23) becomes:

$$S_{v,GR}(f) = \left(\frac{\text{SS}/\ln(10)+\text{Q}_\text{i}/\text{C}_\text{ox}}{\text{Q}_\text{i}/\text{C}_\text{ox}}\frac{1+\theta_{10}\text{Q}_\text{i}/\text{C}_\text{ox}+\theta_2{\text{Q}_\text{i}}^2/{\text{C}_\text{ox}}^2}{1-\theta_2(\text{Q}_\text{i}/\text{C}_\text{ox})^2}\right)^2\frac{q^2 N_{\text{eff}}\tau_0}{WLC_{ox}^2}\frac{1}{1+(2\pi f\tau_0)^2} \tag{24}$$

where SS is the subthreshold swing and θ_{10} is the intrinsic first order mobility attenuation coefficient.

Of course, if $R_{\text{ch}}/R_{\text{t}} \approx 1$ (22) becomes as (8). In strong inversion, if the θ_{10} and θ_2 impact may be neglected, (24) also becomes as (8). However, even if these latter assumptions may be generally true for old planar technologies, it may not be valid for today's 3D nanometric technologies [21]. It may be concluded that the GR noise plateau dependence with the applied bias depends on the considered initial hypothesis.

As the $1/f$ noise may arise from the addition of the GR noise spectra [33–35] this conclusion may also have an impact on the physical interpretation of the input referred 1/f voltage-noise power spectral density dependence on the applied bias, but this point will be discussed in a future work.

However, as the low frequency noise spectroscopy studies are performed at fixed polarization, employing (8) instead of (22) or (24) may have a more limited impact, leading to an underestimation or an overestimation of the effective trap densities for all temperatures investigated.

The study is performed in the linear operating regime and in the 10–100 kHz frequency range, where the impact of parasitic capacitances is negligible since the unity-gain frequency is in the GHz range [36]. This justifies the use of a resistive model and of the noise equivalent circuit as in [10, 21, 29, 30].

3. Low frequency noise spectroscopy for traps located in the depletion region

At fixed temperature, the characteristic relaxation time for traps located in the depletion region of the transistor, following the Shockley-Read-Hall model, does not vary with the polarization if a cross-point between the trap energy level and the Fermi level exists [13, 16]. With the increase in the applied gate voltage, the Fermi level will scan the same trap but at an increased depth in the bandgap. If there is no cross-point between the trap energy level and the Fermi level, the characteristic relaxation time will vary with the applied gate voltage, but with an exponential factor (β) significantly lower (i.e. β less than 10 V^{-1}) [16] than in the case of the traps located near the dielectric/channel interface (i.e. β between around 20–35 V^{-1}) [13].

The GR voltage noise plateau increases as $(\Psi_S)^{1/2}$ in the subthreshold operation with the increase in the applied gate voltage and becomes independent of the applied polarization in strong inversion for a 'generation' GR noise process [13]; Ψ_S being the surface potential. For the 'trapping' GR noise process, the GR voltage noise plateau in the subthreshold operation decreases as $(\Psi_S)^{-1/2}$ for majority carrier trapping or as $(\Psi_S)^{-1}$ for minority carrier trapping, respectively. In strong inversion the GR plateau increases as INT(V_{GT}) (logarithmic increase) corresponding to the value of the integral over the channel potential [6, 13].

The temperature evolution of the characteristic relaxation time of a trap situated in the depletion region allows the construction of an Arrhenius diagram [6, 12, 13]:

Table 1. Quasi–Fermi shift with temperature (300 K to 250 K), using (26) and considering a first-order calculation the following reference parameter values: the inversion layer thickness is equal to 2 nm for a device having an EOT (equivalent oxide thickness) of 1 nm, assuming a threshold voltage of 0.3 V, a threshold voltage rate of -1 mV K^{-1}, the intrinsic carrier concentration n_i at 300 K of $1 \cdot 10^{10}$ cm^{-3}. I_D was calculated using e.g. (2) of [32], assuming that the inversion charge may be determined using the Lambert-W approach with an ideality factor of 1 and that the phonon scattering prevails in the mobility law as $\mu_0(T) = \mu_{0\,300K}(T/300)^{-3/2}$. For temperature shift from 300 K to 250 K the I_D correspond to an applied V_{GS} of 1.3 V at 300 K, i.e. ∼8.4 μA; while for the temperature shift from 300 K to 350 K, the I_D corresponds to an applied V_{GS} of 1 V at 300 K, i.e. ∼7 μA (other considered parameters: $W/L = 0.2$ μm/0.2 μm, $\mu_{300K} = 100$ cm^2/(Vs), $\theta_1 = 0.6$ V^{-1}, $\theta_2 = 0.4$ V^{-2}). In first-order approximation the inversion layer thickness, θ_1 and θ_2 are assumed constants over the considered temperature range.

Temperature shift	Quasi-Fermi shift (meV)		
	V_{GS} = const.	V_{GT} = 1 V	I_D = constant
300 K to 250 K	−11.6	−13.7	−0.6
300 K to 350 K	14.6	10.9	0.7

if $E_T - E_i > 0$

$$\ln\left(\tau_0 T^2\right) = \frac{E_C - E_T}{k_B T} + \ln\left(\frac{h^3}{4{k_B}^2 \sigma\sqrt{6\pi^3 M_c m_e^{*1/2} m_h^{*3/2}}}\right) \tag{25a}$$

if $E_T - E_i < 0$

$$\ln\left(\tau_0 T^2\right) = \frac{E_T - E_V}{k_B T} + \ln\left(\frac{h^3}{4{k_B}^2 \sigma\sqrt{6\pi^3 M_c m_e^{*3/2} m_h^{*1/2}}}\right) \tag{25b}$$

where h is the Planck constant, M_c is the number of conduction band energy minima and m_e^* and m_h^* are the effective mass of electrons and of holes, respectively.

In order to perform low frequency noise spectroscopy, the same polarization should be imposed over the entire investigated temperature range. There are three possibilities: to maintain the same applied gate voltage, the same gate overdrive or the same applied drain current.

The advantage of keeping the same applied gate voltage or gate overdrive is that the same operating regime is maintained over the temperature range. As a drawback, the quasi-Fermi level will obviously change with temperature, in particular because of the threshold voltage variation with temperature. If the quasi-Fermi level changes with the temperature, obviously it is no longer guaranteed that the same trap is scanned.

Keeping the same applied drain current may lead to a much lower variation of the quasi-Fermi level, as the threshold variation may be partially compensated by the mobility variation with temperature. Hence, since a lower variation of the quasi-Fermi level change with the temperature is induced, there are more chances to scan the same trap over the temperature; and if a cross-point exists between the trap energy and the Fermi level to may keep tracking it over a large temperature range than in the case of the constant applied gate voltage or gate overdrive. As a minus, for a very wide investigated temperature range, the operation regime may change.

The quasi-Fermi level may be expressed as [37]:

$$E_{Fn} - E_i = k_B T ln\left(\frac{n_{inv}}{n_i}\right) = k_B T ln\left(\frac{|Q_{inv}|}{q n_i}\right). \tag{26}$$

In (26) Q_{inv} represents the volume inversion charge density. The quasi-Fermi level shift with temperature, considering the intrinsic carrier density variation and the Fermi level variation with temperature, may be calculated using (26) and some reference parameters. The results of first-order calculations, shown in table 1, prove that imposing a constant drain current leads to lower variation of the quasi-Fermi level shift with temperature under strong inversion operation. This trend is maintained regardless of which reference parameter values in the table 1 legend are considered.

It was already proposed to use the GR noise plateau versus GR noise relaxation time as an additional criterion to confirm that the considered characteristic relaxation time employed in the construction of the Arrhenius diagram using (25) are related to the same type of trap [20]. Considering (22) or (24) it

is obvious that the GR noise plateau (A_0) versus the GR relaxation time (τ_0) presents, under some conditions, a quasi-linear dependency, particularly when a constant drain current polarization is imposed. Indeed, considering (22), as I_D is constant, if the access resistance presents a slight variation in the considered temperature interval the $R_{ch}/R_t = (V_{DS}-I_D R_{access})/V_{DS}$ ratio will present also a slight variation with temperature. Hence, it may be considered that the A_0 and τ_0 evolution with temperature may still present a quasi-linear dependence even if $R_{ch}/R_t \neq 1$. The same conclusion also holds if (24) is considered, when the temperature range is not wide and when the mobility attenuation factors do not present significant variation in the considered temperature interval.

Considering the evolution of the GR voltage noise plateau with the applied polarization at fixed temperature, it may be suggested that for a narrow-investigated temperature range the slope of A_0 versus τ_0 may still be used to estimate the surface trap density, irrespective of the 'generation' or 'trapping' GR noise process and of the constant polarization imposed over the temperature range (constant applied I_D or constant V_{GS} or V_{GT}). For the extraction of the volume trap density one may use [13]

$$N_T = \frac{4\pi \left[S_{v,GR}(f_0,T)\right]_{max} f_0 C_{ox}^2 WL}{q^2 W_D B} \tag{27}$$

where B should be equal to 1/3 for the 'generation' GR process or $B < 1$ but exhibiting a logarithmic dependence with the applied voltage for the 'trapping' GR process; $S_{v,GR}(f_0,T)$ being the GR voltage noise level at fixed frequency f_0 and temperature T.

Indeed, from e.g. (7) or (8), one can observe that for a given frequency f_0, $S_{v,GR}(f_0,T)$ is proportional to $\tau_0(T)/(1+(2\pi f_0 \tau_0(T))^2$. For $2\pi f_0 \tau_0(T) \gg 1$, $S_{v,GR}(f_0,T)$ is proportional with $\tau_0(T)^{-1}$, and hence $S_{v,GR}(f_0,T)$ will increase with increasing temperature because τ_0 decreases. For $2\pi f_0 \tau(T) \ll 1$, $S_{v,GR}(f_0,T)$ is proportional with $\tau_0(T)$, and consequently $S_{v,GR}(f_0,T)$ will decrease with increasing temperature [13]. This means that the measured $S_{v,GR}(f_0,T)$ dependence with temperature passes through a maximum which may be used to estimate the volume trap density. The comparison between the surface trap density and volume trap density values may provide us with the B evolution with the applied voltage and consequently, additional confirmation of whether it is a 'generation' or a 'trapping' GR noise phenomenon.

4. Results and discussion

Typical $I_D(V_{GS})$ and $g_m(V_{GS})$ are plotted in figures 1 and 2 for two devices having the same geometric dimensions. Significant device-to-device variability can be observed by comparing the behavior of device #1 and device #2. The device dimensions are indicated in the legend of figure 1. The methodology presented in [32] is employed for the parameter extraction. Good agreement may be observed from weak to strong inversion operation between the experimental and the modeled $I_D(V_{GS})$ and $g_m(V_{GS})$ behavior using their analytical expression described e.g. in (2) and (5) of [32]. In general, the access resistance may be estimated using θ_1 versus G_M (gain factor) for different devices having different gate length or width dimensions. However, if significant device-to-device variability exists, this method may lead to important errors in the extracted access resistance value. Hence, in the first order approximation, the access resistance is estimated as θ_1/G_M by neglecting the impact of the intrinsic first mobility attenuation factor θ_{10}. The extracted values of R_{access} over the temperature range for both devices are plotted in figure 3. At room temperature, a value of about 1940 Ω for device #1 and of 3480 Ω for device #2 are found. The apparently higher values of the access resistances lead in strong inversion to a R_{ch}/R_t of about 91% for device #1 for a bias of 2.5 μA, and of about 89% for device #2 for a bias of 1.5 μA, suggesting, however, very good electrostatic control of the devices. It may be observed that for both devices the access resistance slightly increases with temperature.

In figure 4, typical examples of input-referred voltage power spectral densities multiplied by frequency versus the frequency are illustrated for different applied drain current polarization at a fixed temperature. GR noise contributions related to traps located in the depletion region of the devices may be observed for both devices.

Indeed, for device #1 operated at 320 K, clear GR noise having a characteristic frequency independent of the applied polarization may be evidenced at about 75 Hz. The noise behavior for frequencies higher than 1 kHz, even if $S_v \cdot f$ increases proportionally with the frequency increase, it should more likely be attributed to the addition of different GR noise contributions instead of the white noise. This hypothesis may corroborate with the noise spectra of device #2, which exhibit a clear GR noise contribution which presents comparable $S_v \cdot f$ level for frequencies higher than 1 kHz. Moreover, for device #2,

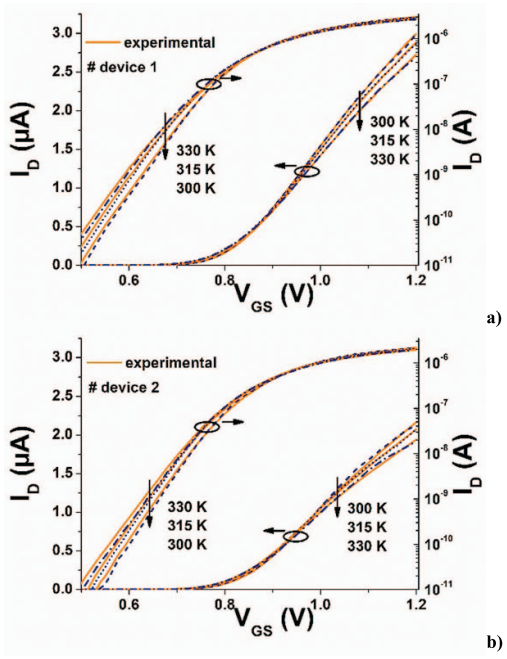

Figure 1. Comparison between the experimental and modeled drain current at different temperatures (a) for device #1; (b) for device #2. Geometric dimension: $W_{\text{fin}} = H_{\text{fin}} = 10$ nm, 4 fins in parallel (N), $W = 160$ nm, $L = 250$ nm, EOT = 5.6 nm, $V_{DS} = 50$ mV.

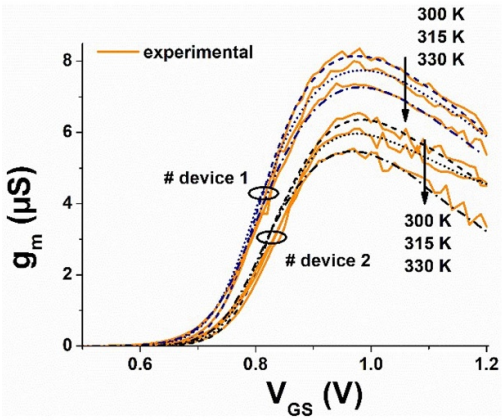

Figure 2. Comparison between the experimental and modelled transconductance at different temperatures (a) for device #1; (b) for device #2.

the impact of a trap located in the depletion region may be observed for a characteristic frequency independent of the applied polarization of about 13 kHz.

Each noise spectrum is modeled by considering the contributions of three uncorrelated noise sources: white noise (W_n), flicker noise (K_f) and GR noise ($S_{v,\text{GR}}$) contributions:

$$S_v(f) = W_n + \frac{K_f}{f} + \sum_{i=1}^{N} \frac{A_{0i}}{1 + \left(\frac{f}{f_{0i}}\right)^2}. \tag{28}$$

In figure 5, a typical comparison between the experimental data and the model of (28) is illustrated. For frequencies higher than 1 kHz, the $S_v \cdot f$ increases almost linearly with frequency. Even if this trend is generally attributed to a white noise contribution, the value required to fit the experimental data is much higher than the theoretical Johnson–Nyquist value. Therefore, this trend can be adjusted by using two or more GR noise contributions. However, the parameters of these GR contributions may not be accurately estimated. In any case, a clear GR noise contribution may be evidenced in the low frequency range. Hence, as the study is focused only on contributions for which the GR parameters (A_0 and f_0)

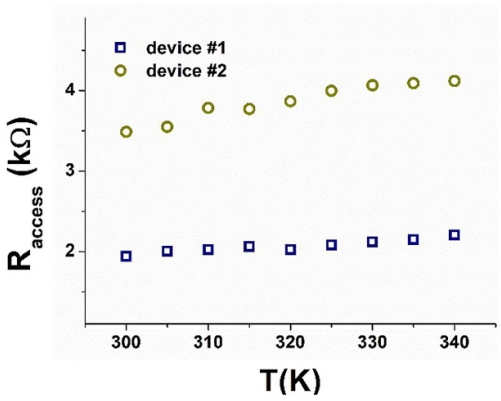

Figure 3. Estimated access resistance versus temperature.

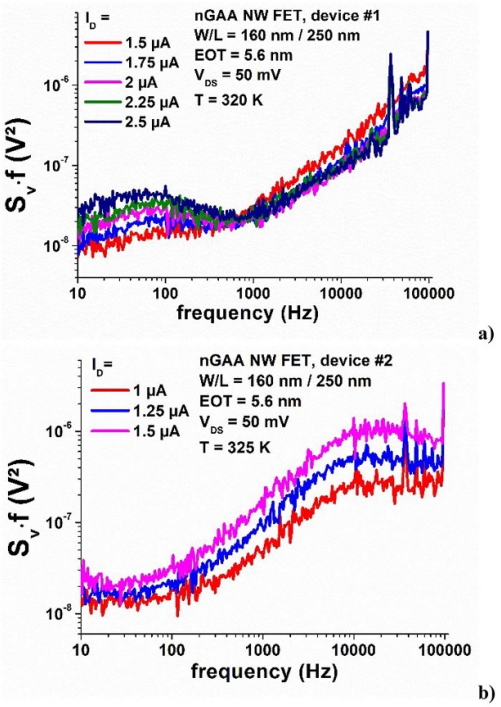

Figure 4. Example of input referred voltage power density spectra noise for different applied drain current polarization (a) at 320 K for device #1; (b) at 325 K for device #2. Clear GR noise contribution may be evidenced at around 75 Hz for device #1 and around 13 kHz for device #2. In the low frequencies range, $1/f$ contribution to the total noise may be evidenced only for lower applied polarization, e.g. for device #2 at $I_D = 1$ μA and 325 K operation.

may be identifiable without ambiguity, for the case illustrated in figure 5, only the GR contribution at 72 Hz is considered.

The evolution of the characteristic frequency of the GR noise contribution with the applied polarization for device #1 operated at 320 K is plotted in figure 6(a). The increase of the applied gate voltage does not affect the characteristic frequency value, suggesting that the GR noise should be related to a trap located in the Si film (the depleted region of the device) for which a cross-point between the trap energy level and the Fermi level exists. The GR noise plateau exhibits a logarithmic increase with the applied polarization in strong inversion, suggesting that the GR noise contribution should be related to a 'trapping' process.

Hence, an Arrhenius diagram may be constructed as described in [6, 12, 13] using the model of (25). Using a least-squares linear fit of $\ln(t_0 T^2)$ versus $1/k_B T$ the capture cross-section may be estimated from the y-intercept while the energy difference (ΔE) between the band energy (E_C or E_V) and the trap energy E_T can be extracted from the slope. In our case of a 'trapping' GR noise process the energy difference should be calculated between the valence band energy (E_V) and the trap energy E_T.

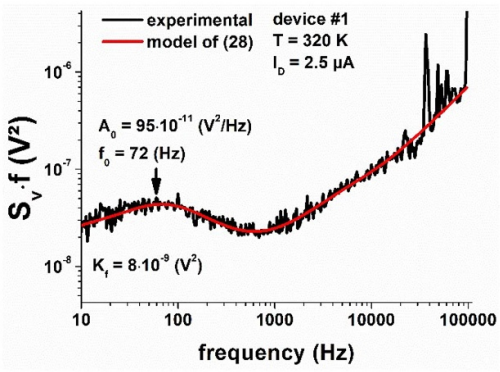

Figure 5. Best agreement between the experimental data and the model of (28) is obtained considering flicker noise and several GR noise contributions. Only the parameters of the clearly identified GR contribution at 72 Hz are shown.

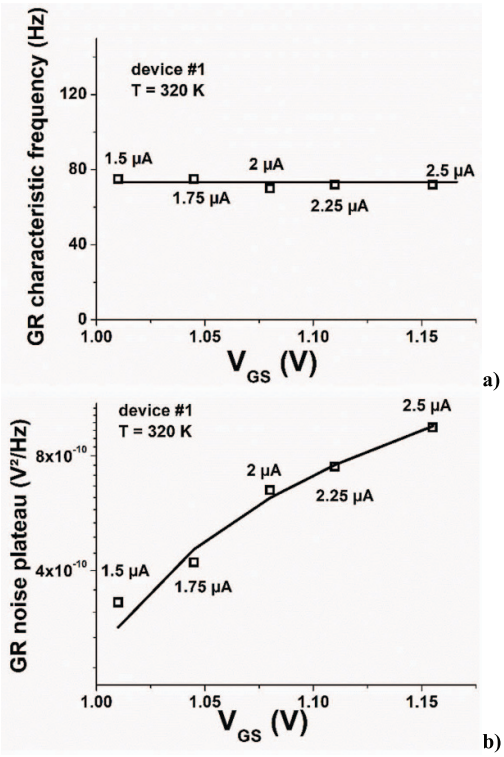

Figure 6. Evolution with the applied polarization at fixed temperature of 320 K for device #1: (a) of the GR characteristic frequency; (b) of the GR plateau.

It may be noticed that a non-negligible error on the capture cross-section value may be observed if (25a) is employed instead of (25b). By comparing the estimated ΔE and σ to previous results from deep-level transient spectroscopy studies, the physical nature of the identified traps may be specified.

In figure 7, the ln $(\tau_0 T^2)$ versus $1/k_B T$ evolution constructed for both devices is illustrated for all drain current polarization at which the GR noise may be attributed to a trap located in the depletion region of the transistor.

The trap identified for device #1 may be related to a divacancy-hydrogen V_2H trap ($\Delta E = 0.45$ eV and σ of 10^{-17} cm^2 reported in [16, 38–41]); it may be related to the presence of residual hydrogen after annealing. The trap identified for device #2 may be related to a single negatively charged acceptor state (0/-) of the divacancy (V_2) trap ($\Delta E = 0.42$ eV) and σ of 10^{-15} cm^2 reported in [16, 40–42]; it may be induced during the ion implantation process step, and can be explained by the recombination or the evolution to a stable state of unstable defects like Frenkel pairs.

The GR plateau versus GR relaxation time is plotted in figures 8(a) and (b) for all drain polarization considered for device #1 and device # 2, respectively. A quasi-linear behavior is observed.

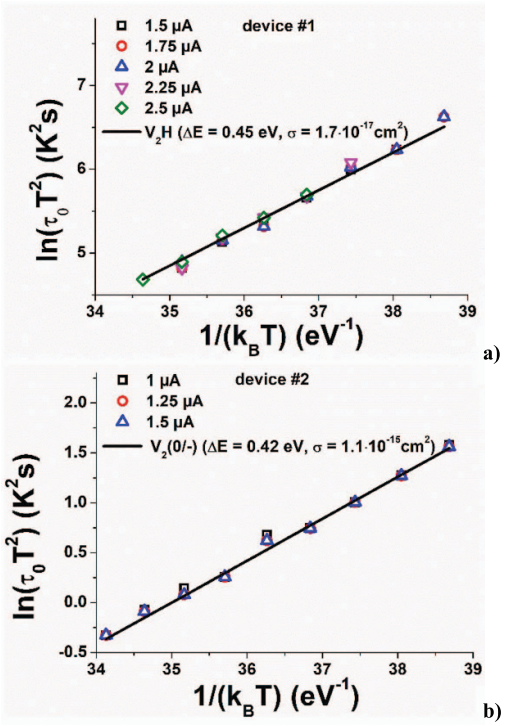

Figure 7. Arrhenius diagram constructed using (25): (a) for device #1; (b) for device #2.

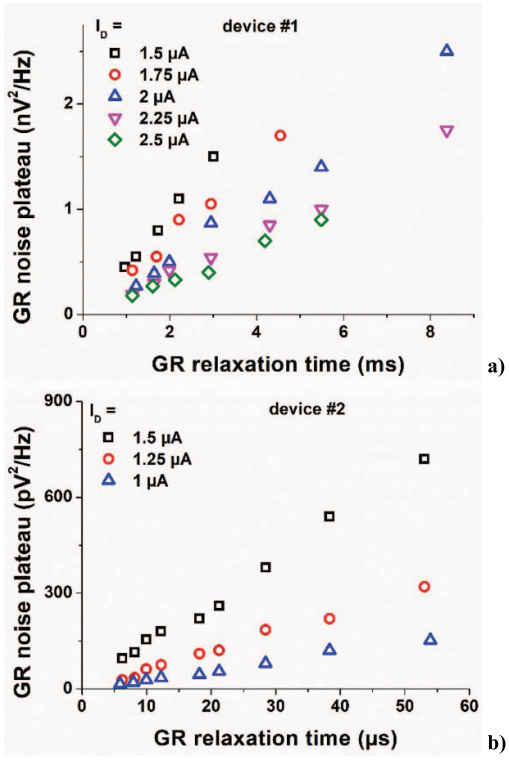

Figure 8. GR plateau versus GR relaxation time (a) device #1; (b) device #2.

This may be related to the fact that the $(R_{ch}/R_t)^2$ evolution with temperature for a given I_D polarization presents a slight variation, as may be observed from figure 9, even considering an I_D of 2.5 μA for device #1 and of 1.5 μA for device #2.

Hence, from the slope of the GR plateau versus the GR, relaxation time, according to (22), the effective surface density of the traps (N_{eff}) may still be evaluated. The estimated N_{eff} values for each drain

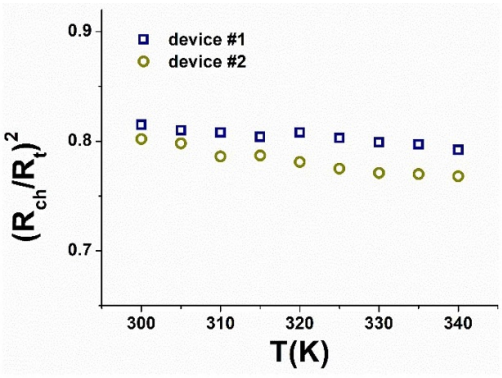

Figure 9. $(R_{ch}/R_t)^2$ ratio versus temperature. I_D is set at 2.5 μA for device #1 and at 1.5 μA for device #2.

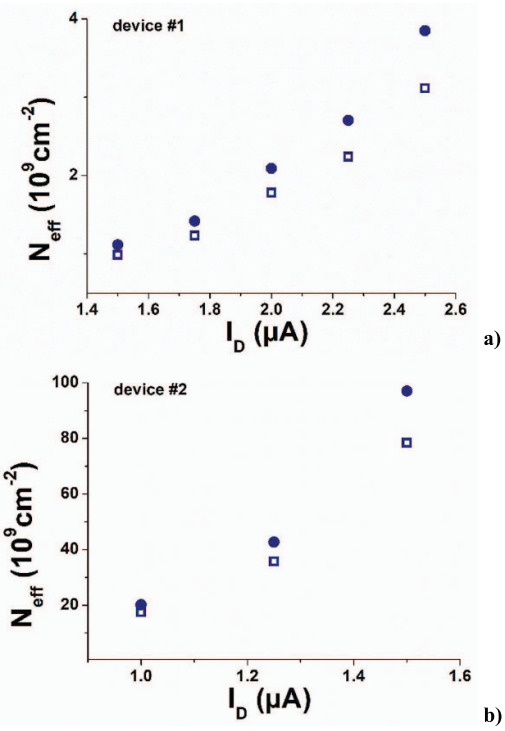

Figure 10. Estimated surface trap density N_{eff} for (a) device #1; (b) device #2. Empty symbol represents the N_{eff} values considering R_{ch}/R_t of 1 in (22); the full symbol represents the N_{eff} values considering estimated R_{ch}/R_t plotted in figure 9.

current bias are shown in figure 10. It may be noticed that not considering the access resistance impact in (22) leads to a non-negligible underestimation of the values of the surface density of traps.

In figure 11 the $S_{v,GR}(f_0,T)$ versus temperature evolution is shown for both devices for all investigated drain current polarizations. A bell-shaped behavior as expected may be observed. Using the maximum of the $S_{v,GR}(f_0,T)$ the volume trap densities multiplied by the B coefficient may be evaluated using (27), the results being illustrated in figure 12. Hence, the B coefficient may be experimentally evaluated as $N_{eff}/(N_T W_d)$, where in our case W_D is considered to be 5 nm as the nanowire width and height are of 10 nm. The B coefficient is lower than 1 and as evidenced in figure 13 its behavior exhibits a logarithmic increase with the polarization, in agreement with the 'trapping' GR noise phenomena hypothesis. However, for device #1 at I_D of 1.5 μA the estimated B value is too close to 1, suggesting a possible limitation of the method permitting the calculation of the volume trap density developed for conventional planar transistors, as already pointed out in [43]. Of course, if the access resistances impact was corrected in both N_{eff} and N_T extraction, the estimated B values are very close to the ones for which the access resistance impact was not corrected.

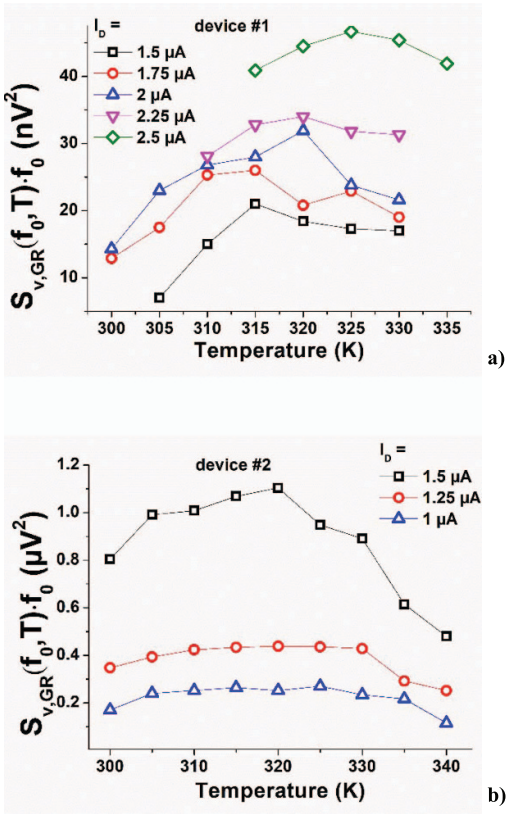

Figure 11. $S_{v,\mathrm{GR}}\ (f_0,T)\cdot f_0$ versus temperature (a) for the V_2H trap identified for device #1, $f_0 = 60$ Hz; (b) for the $V_2(0/-)$ trap identified for device #2, $f_0 = 8.9$ kHz.

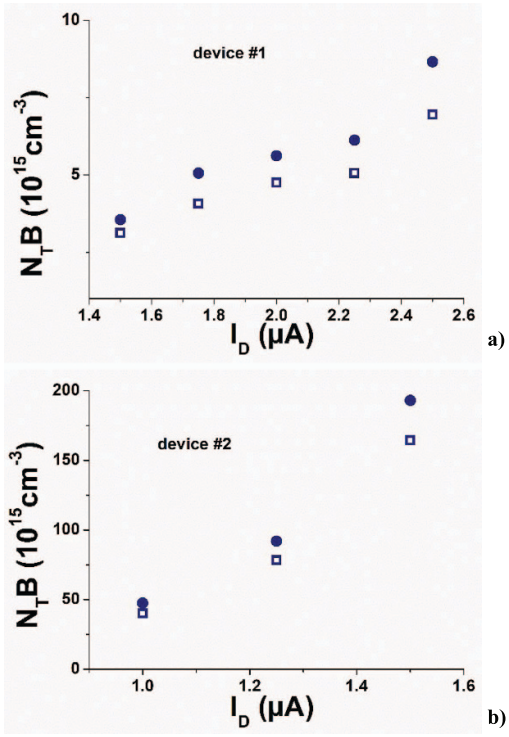

Figure 12. Volume trap densities multiplied by the B coefficient as a function of the applied polarization for (a) device # 1; (b) device #2 Empty symbol represents the N_TB values not corrected by the R_{access} impact; the full symbol represents the N_TB values corrected by the R_{access} impact.

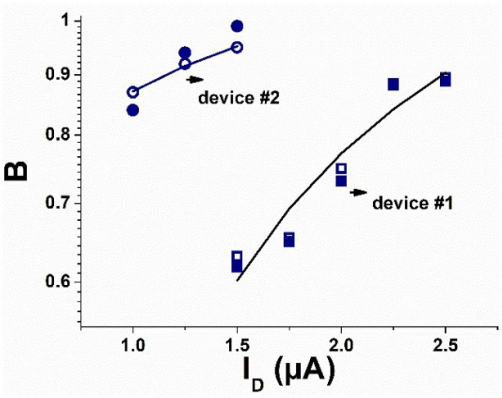

Figure 13. Extracted *B* coefficient versus the applied polarization. Empty symbol represents the *B* values not corrected by the R_{access} impact; the full symbol represents the B values corrected by the R_{access} impact.

5. Conclusion

It is shown that the generally accepted GR voltage noise plateau expression is based on $g_m = I_D/(Q_i/C_{ox})$ approximation which is unphysical even in linear operation, before or after the threshold. For instance, in strong inversion operation, this assumption can no longer be considered for actual technologies for which the access resistance and the second order mobility attenuation factor play an important role. Based on a simplified resistive model and by comparison with the small signal equivalent circuit it is demonstrated that the GR voltage noise plateau should include the ratio of the channel resistance to the total resistance.

It is confirmed that in order to keep as low as possible the quasi-Fermi level shift over the temperature it is better to impose a constant drain current polarization, in particular in strong inversion operation. It may be suggested that in order to identify the nature of traps located in the depletion region of the transistor it is mandatory to perform measurements at different polarizations at each fixed temperature. This can be used to confirm that a cross-point between the trap energy level and the Fermi level exists for all investigated temperatures. Moreover, it can be used to confirm whether it is a 'generation' or a 'trapped' GR noise phenomenon.

Two types of traps, V_2H and $V_2(0/-)$ located in the depletion region (Si film) of the devices and related to a 'trapping' GR process were identified for GAA NW FETs. Neglecting the impact of the channel-to-total resistance ratio on the GR plateau level leads to a non-negligible underestimation of the trap density.

Data availability statement

The data cannot be made publicly available upon publication because no suitable repository exists for hosting data in this field of study. The data that support the findings of this study are available upon reasonable request from the authors.

ORCID iDs

B Cretu 0000-0002-2727-4605
E Simoen 0000-0002-5218-4046

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