

Low-impedance Contact CDM – Evaluation and Modeling

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Abstract – Standard charged device model (CDM) ESD simulators used today cannot be used at wafer level and suffer from high zap-to-zap peak current variability at low voltages. The low-impedance contact CDM provides a solution to these problems. In this paper we evaluate its performance and propose a model for the setup.

I. Introduction

The low-impedance contact CDM (LI-CCDM) tester has been suggested by [1] as an alternative to the standardized field-induced CDM (FICDM) tester [2]. Even though the FICDM tester is the acknowledged method to test for CDM, its zap reproducibility for qualification levels below 250 V starts to drop. This zap reproducibility becomes intolerable for levels below 125 V [1], [3], [4]. Furthermore, the FICDM cannot be used for wafer-level testing, which could to speed up the ESD design and testing time.

A wafer-level CDM (WCDM2) tester has been demonstrated before [5]. However, the equivalent resistance of that tester is 50 Ω . The capacitively coupled TLP (CC-TLP) tester [6], which is the closest design to the LI-CCDM, is also a 50 Ω setup. Similarly, the tester presented here also uses a vfTLP as a pulse source and the DUT capacitive coupling to ground to create a CDM-like pulse. The main novelty of the LI-CCDM is the equivalent resistance lower than 50 Ω . The downside of 50 Ω CDM-like systems is their pulse width, which is wider than specified by the standard [2], unless the pulse is truncated as in CC-TLP. Lower system impedance results in narrower pulses that more closely match the standard.

In this paper, we present the 25 Ω and the 16.7 Ω CCDM testers capable of wafer-level testing with high zap-to-zap reproducibility at levels as low as 10 V. Our wafer-level LI-CCDM tester resembles the package-level version presented in [1], however, in this work, LI-CCDM will always refer to the wafer-level implementation rather than the package-level version. To understand better the LI-CCDM tester, we also test

the impact of the “field” plate dielectric thickness and the wafer chuck grounding on the pulse shape. A compact model that can reproduce measured waveforms is also presented. While differences may exist between the wafer-level and package-level testers, it is assumed that the insights gained on this wafer-level version are applicable to the package-level tester as well.

II. Low-impedance CCDM testers

Two different LI-CCDM test setups have been used for this work: one with a 25 Ω and the other with a 16.7 Ω equivalent resistance. Sub-section A describes the two setups in detail. Sub-section B explains the equation used to calculate the current through the DUT.

A. 25 Ω and 16.7 Ω CCDM

The 25 Ω CCDM discharge-head consists of two 50 Ω coaxial cables connected to the probe needle through a 50 Ω strip-line. The cable shielding is also connected to a square conductive ground plate with a 63.5 mm edge length [2]. The head is held and maneuvered using a probe station micro-manipulator (Figure 1). Figure 2 shows photograph of the prototype 16.7 Ω CCDM probe-head in more detail. The DUT is placed on a 0.381 mm thick FR4 board. The FR4 is copper-plated on the bottom side only, so it makes contact to the 200 mm wafer chuck. Holes in the FR4 allow the chuck vacuum to hold the DUT in place. The chuck itself can be grounded or left floating.

The rest of our setup consists of the Hanwa HED-T500 vfTLP, one 6 dB and two 20 dB attenuators to protect the oscilloscope input, and the Tektronix MSO72304DX oscilloscope with 100 GS/s sampling



rate and 23 GHz bandwidth. One of the 20 dB attenuators is programmable and can be bypassed in case of a small vfTLP signal.

In all cases reported in this paper, a 10 ns long pulse with rise time equal to 0.2 ns has been used. The LI-CCDM current pulses appear both during the vfTLP rising and falling edges. The 10 ns pulse has been chosen to enable the observation of a longer pulse tail, before the negative current pulse arrives. The negative pulse is not shown and should be avoided by slowing down the vfTLP falling edge. The hardware upgrade to control the falling edge speed will be available to us in the future.

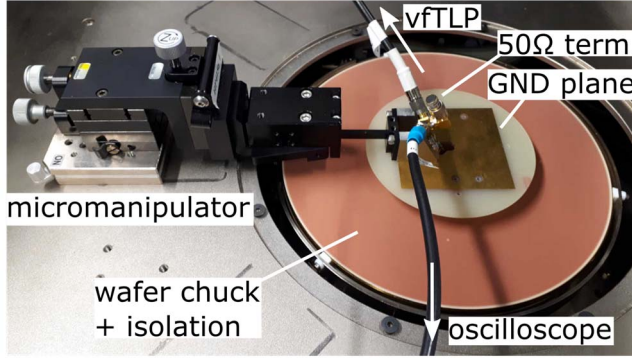


Figure 1 – Photograph of the 16.7 Ω CCDM prototype probe-head mounted onto a micromanipulator.

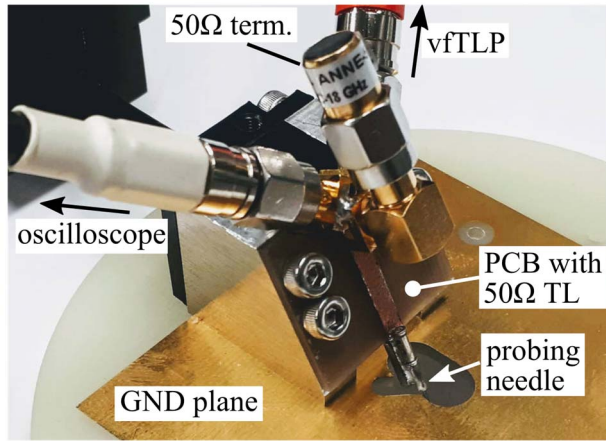


Figure 2 – Photograph of the 16.7 Ω CCDM prototype probe head. Three SMA connectors are mounted on a small PCB. All three signals are connected to one side of a 50 Ω microstrip line (TL). A short DC probe needle is mounted on the other side of the microstrip. A hole in the ground plane allows the probe needle to contact the DUT underneath and also serves as a viewing point.

The oscilloscope bandwidth has been limited to 18 GHz, which is the nominal maximum bandwidth of SMA connectors. Limiting the bandwidth also reduces the noise spectrum. The sampling rate has been set to 100 GS/s with the interpolation option disabled.

Figure 3 illustrates the 25 Ω CCDM setup. The 16.7 Ω CCDM test-head is identical to the 25 Ω one, except

for the number of coaxial cables. In this case, a third cable is connected in parallel with the previous two and terminated with a 50 Ω resistor. This reduces its equivalent impedance to 16.7 Ω. Figure 4 illustrates this 16.7 Ω CCDM setup.

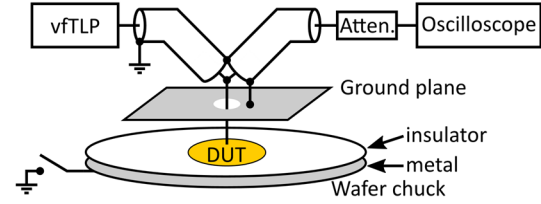


Figure 3 - Illustration of the 25 Ω CCDM measurement setup.

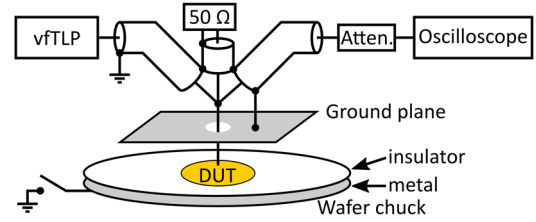
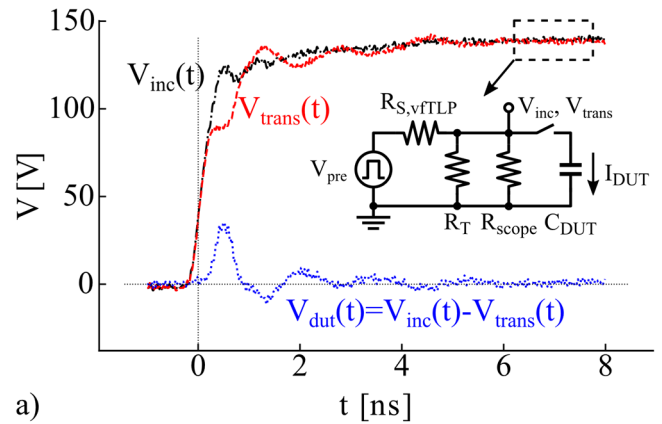
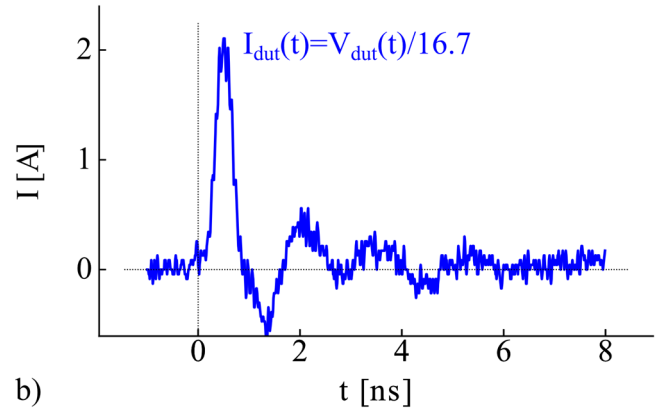


Figure 4 - Illustration of the 16.7 Ω CCDM measurement setup.



a)



b)

Figure 5 – Example of calculating the I_{dut} (b) from the measured V_{inc} and V_{trans} (a) for the 16.7 Ω CCDM using Equation 1. The plateau value of V_{inc} and V_{trans} in a) is ~133 V, which is 2/3 of $V_{vfTLP} = 200$ V or, more intuitively, 1/3 of the actual pre-charge voltage $V_{pre} = 400$ V and can be calculated by a resistive divider as in (a) formed by the vfTLP internal resistance $R_{S,vfTLP} = 50$ Ω, the oscilloscope $R_{scope} = 50$ Ω and the termination $R_T = 50$ Ω.

B. Calculating I_{DUT}

From [1] we know that the current through the device can be calculated from the transmitted voltage waveform V_{trans} , measured when in contact with the DUT, the incident voltage waveform V_{inc} , measured when separated from the DUT, and the setup equivalent resistance Z . The following equation is used:

$$I_{DUT}(t) = \frac{V_{inc}(t) - V_{trans}(t)}{Z} \quad (1)$$

In this case where two coaxial 50Ω cables are used (Figure 3), Z equals to 25Ω . For the case of three coaxial cables (Figure 4), Z equals to 16.7Ω . Figure 5 gives an example of the calculated I_{dut} .

III. Measurement waveforms

Both the 25Ω and 16.7Ω discharge heads have been used to measure the response of our LI-CCDM setup to the large and small JEDEC test module. Firstly, the LI-CCDM current waveforms are compared to FICDM data from [2] and the standardized CDM waveform characteristics. Secondly, the reproducibility of the measured LI-CCDM waveforms is discussed.

A. LI-CCDM current waveforms

To compare our LI-CCDM waveforms to data from a FICDM setup [2], waveforms for vTLP pre-charge voltages in the range from 75 to 500 V have been acquired. The LI-CCDM waveform with the closest peak DUT current I_{peak} to the reference FICDM of 250 V has been chosen.

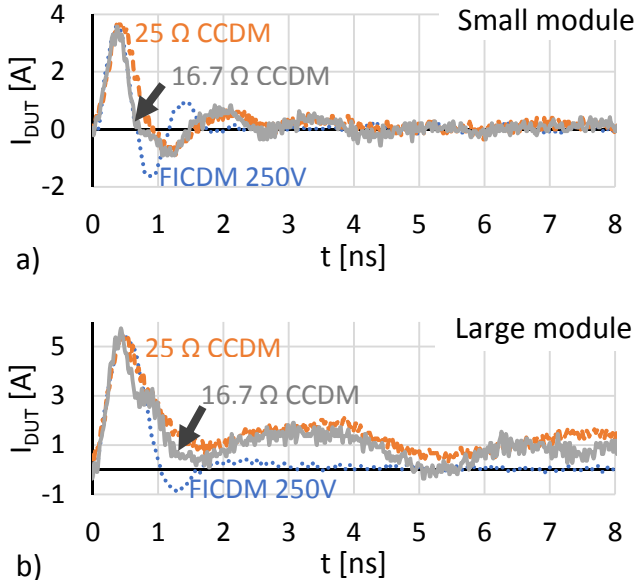


Figure 6 – Current waveforms for the a) small and b) large JEDEC test module. Measurement results from both the 16.7 and 25 Ω discharge heads are compared to the FICDM 250 V waveform.

As expected, higher pre-charge voltages are needed for the LI-CCDM to reach the same I_{peak} as FICDM [4]. The waveforms for both the small and large test modules are shown next to a 250 V FICDM waveform in Figure 6.a and Figure 6.b accordingly.

The LI-CCDM waveforms largely agree with those of FICDM and are compliant to the spec in terms of rise time, peak current, overshoot and pulse width at the 50% point. Still, the 16.7Ω setup matches the CDM pulse width better. However, it is noticeable that the pulse tail for the large module (Figure 6.b) does not return to zero as in the FICDM case. This waveform tail offset is not observed for the small module (Figure 6.a).

The waveform tail offset is suspected to arise from the wafer chuck parasitic capacitance and inductance towards ground, as further discussed in Section IV. Regardless of this offset, the analysis of I_{peak} has been carried on and reported in the following section.

B. Zap reproducibility

To check the zap-to-zap reproducibility, we have conducted the following experiment: 100 repetitions for each vTLP zap voltage V_{vTLP} ranging from 10 or 100 V, to 500 V, both for the incident V_{inc} and transmitted V_{trans} waveforms. For each zap, the peak current I_{peak} is calculated according to Eq. 1 and plotted onto a probit plot in Figure 7. The probit plot is the inverse of the cumulative distribution function of the standard normal distribution. To clarify, an similar transformation is often applied to the y-axis when plotting exponential data to generate logarithmic plots. The probit function is the inverse of the normal cumulative distribution function equivalently as the natural logarithm is the inverse of the exponential function. The values on the probit axis are equal to the number of standard deviations σ from the average measured value, while the x-axis represents the actual measured data.

The data points fit well with straight lines in the probit plot in Figure 7. This means that the I_{peak} data can be assumed to follow a normal distribution for the used sample size of 100. This allows us to analyze the I_{peak} variability in terms of normal standard deviations σ .

FICDM measurement standard deviation $\sigma(I_{peak})$ data from [1] is compared to our LI-CCDM data. As the FICDM and LI-CCDM pre-charge voltages are not equal, the deviation data has been plotted as a function of average I_{peak} value instead, as in Figure 8. No matter the pre-charge voltage, the LI-CCDM $\sigma(I_{peak})$ is constant and always below 5%. This affirms that the LI-CCDM zap reproducibility does not depend on the probe, but the accuracy and noise properties of the used instruments.

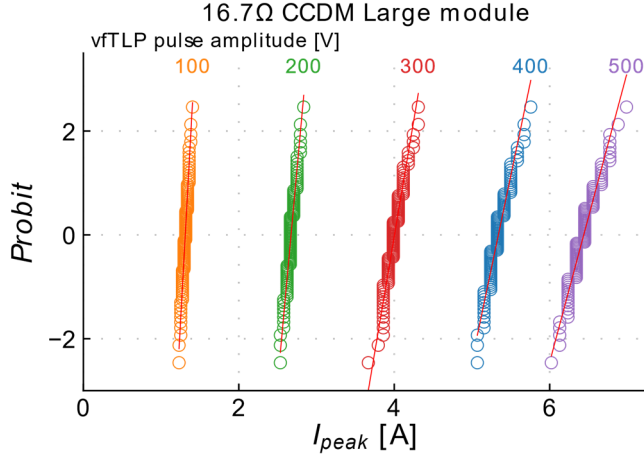


Figure 7 - Peak current (I_{peak}) distributions for pre-charge voltages from 100 V to 500 V measured using the 16.7 Ω CCDM setup and the large JEDEC module. Data points are depicted with circles while the fits are represented by the full lines.

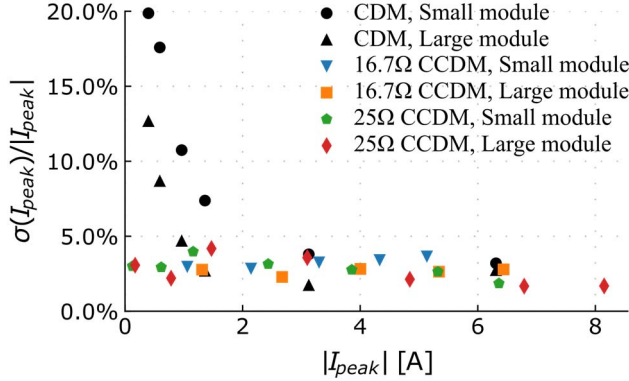


Figure 8 - LI-CCDM peak current standard deviation $\sigma(I_{peak})$ normalized for the average I_{peak} and plotted together with FICDM data from [1] as a function of $|I_{peak}|$.

The $\sigma(I_{peak})$ reported here represents the worst case since the incident waveform V_{inc} is measured in 100 iterations and each is directly compared to a corresponding transmitted wave V_{trans} . To reduce the noise, one could first average the 100 V_{inc} iterations to find the noise-free incident waveform, and then compare it to the V_{trans} .

IV. Influence of the wafer chuck on LI-CCDM measurements

The FICDM field plate is normally connected to a high-voltage source and ground through a 100 M Ω charging resistor. In our LI-CCDM setup, a floating or grounded wafer chuck is used in place of the field plate. Since the chuck is not used as a charge source and because the floating and grounded states are the two extremes in resistance towards ground, the 100 M Ω charging resistor is omitted. Three experiments are discussed in this section: the grounding method of the chuck, the thickness of the chuck dielectric and the chuck size.

A. Wafer chuck grounding

As discussed in Section III.A, the LI-CCDM waveforms measured on our setup are not entirely identical to the FICDM reference. In the attempt to improve them, the chuck grounding is investigated. Three experiments have been designed: one with a floating chuck and two with a grounded chuck. The two grounded cases differ in the cables used to connect the chuck to ground.

The chuck potential has been measured during the vTLP pulse with the same oscilloscope for all three experiments, as depicted in Figure 9. Figure 10.a and b. show that the pulse causes the chuck potential V_{chuck} to change. This can have an impact on the LI-CCDM pulse shape, namely the tail offset in the case of the large JEDEC module as in Figure 10.c.

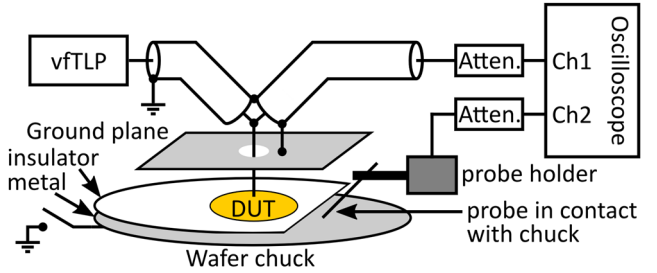


Figure 9 – Measurement setup used to capture the wafer chuck potential during the vTLP pulse.

In the first experiment, the chuck is floating. Even though there is no DC path from the chuck to ground, there is a capacitive coupling.

In the second experiment, the chuck ground is connected to the vTLP and oscilloscope ground through at least two meters long triaxial and coaxial cables, as provided by the Cascade 11000 probing station. This is a low-quality ground from the high-frequency point of view. However, a DC path from the chuck to the ground exists in this case. Regardless, the measurements show no significant difference between the two experiments, as reported in Figure 10.

In the third experiment, an approximately 15 cm long wire has been used to connect the chuck to the LI-CCDM ground plane. This wire significantly reduces the electrical distance of the chuck-to-ground connection, but also changes the parasitic impedances of the chuck and ground plane significantly. The chuck potential V_{chuck} amplitude measured during the vTLP pulse is reduced by about a factor of two (see Figure 10.a). Also, the V_{chuck} average value is much closer to zero (see Figure 10.b). However, the I_{DUT} pulse tail is drastically changed. Figure 10.c depicts the effect of this short GND wire: the first ripple in the I_{DUT} tail has a doubled amplitude. Even though the V_{chuck} is on

average closer to zero, this I_{DUT} pulse shape does not satisfy the requirements.

We assume that this short GND wire is seen by the LI-CCDM pulse as an inductor between the chuck and ground plane. Even though it does reduce the chuck potential V_{chuck} , it probably distorts the potential of the ground plane and creates an unwanted inductance. Effectively, the LI-CCDM setup is changed and should not be directly compared to setups with the floating chuck or the chuck grounded with a long coaxial cable. Therefore, this simple connection from the chuck to the ground plane is discouraged and will not be taken into consideration by other experiments presented in this paper.

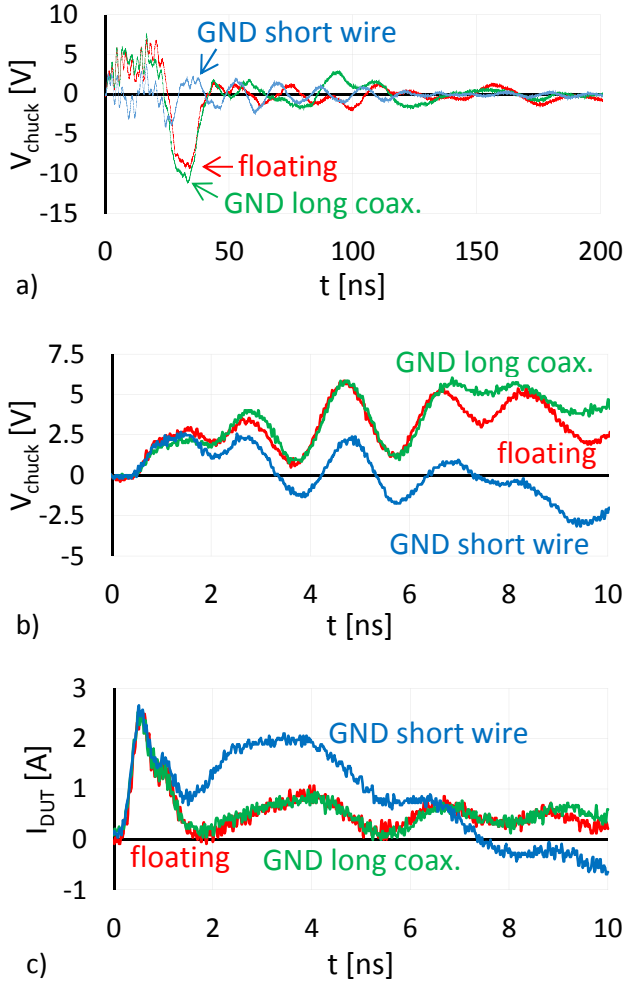


Figure 10 - Three measured LI-CCDM pulses, one for a floating and two for a grounded chuck. V_{chuck} is plotted in a) and on a shorter scale in b). I_{DUT} is shown in c). A pre-charge voltage V_{vTLP} of 200 V and the large JEDEC module have been used for this measurement.

These experiments conclude that a good option for the LI-CCDM tester is to use a floating wafer chuck, as previously suggested by [5]. Alternatively, a 100 M Ω resistor as in the FICDM tester can be used, to avoid any triboelectric charging of the chuck, as suggested by

the Standard Practice for package-level testing [7]. Even if the chuck is grounded through a long cable, the effect will not be visible in the time window of the LI-CCDM pulse. However, Figure 10.c shows that improper chuck grounding could lead to delivering unwanted stress to the DUT after the main LI-CCDM current pulse. Thus, the chuck grounding should be carefully analyzed when using a new wafer probing station for LI-CCDM measurements.

B. “Field plate” dielectric thickness

Even though the dielectric used to isolate the DUT from the field plate is clearly specified by the standard [2], we vary it in this experiment to decrease the DUT-to-chuck capacitive coupling C_{DUT} . The goal of this experiment is to observe the influence of C_{DUT} on the chuck potential V_{chuck} and on the I_{DUT} .

Three different field plate dielectric (FR4) thicknesses h are used for this experiment: the reference one with $h \approx 0.4$ mm, and two thicker dielectrics with $h = 0.8$ mm and $h = 1.6$ mm. Both the small and large modules have been used with the 16.7 discharge head and a 100 V vTLP pre-charge voltage. Figure 11 depicts the recorded V_{chuck} waveforms, while Figure 12.a and b depict the I_{DUT} .

Increasing the dielectric thickness and thus decreasing C_{DUT} results in a slightly reduced I_{peak} (Figure 12.c) and slightly shorter pulse width PW . However, the pulse tail offset is also reduced (Figure 12.d), thus more closely matching the FICDM waveform. Interestingly, the effect of the increased dielectric thickness is much stronger on the pulse tail than on the I_{peak} , as can be seen when comparing Figure 12.c and Figure 12.d.

The thinner dielectric results in more coupling to the chuck and hence can deliver more energy to the chuck parasitic impedances, further confirming the assumption that they are the cause of the I_{DUT} tail offset.

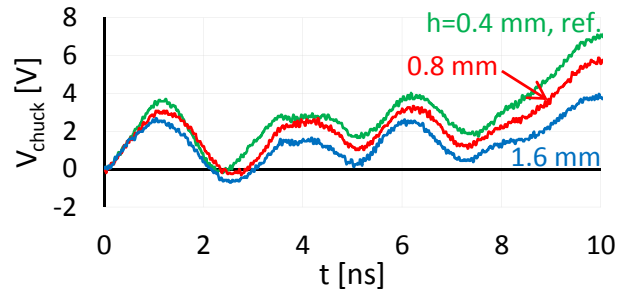


Figure 11 - The chuck potential measured during a 100 V vTLP pulse through the large JEDEC module using the 16.7 Ω CCDM discharge head. h represents the field plate dielectric thickness.

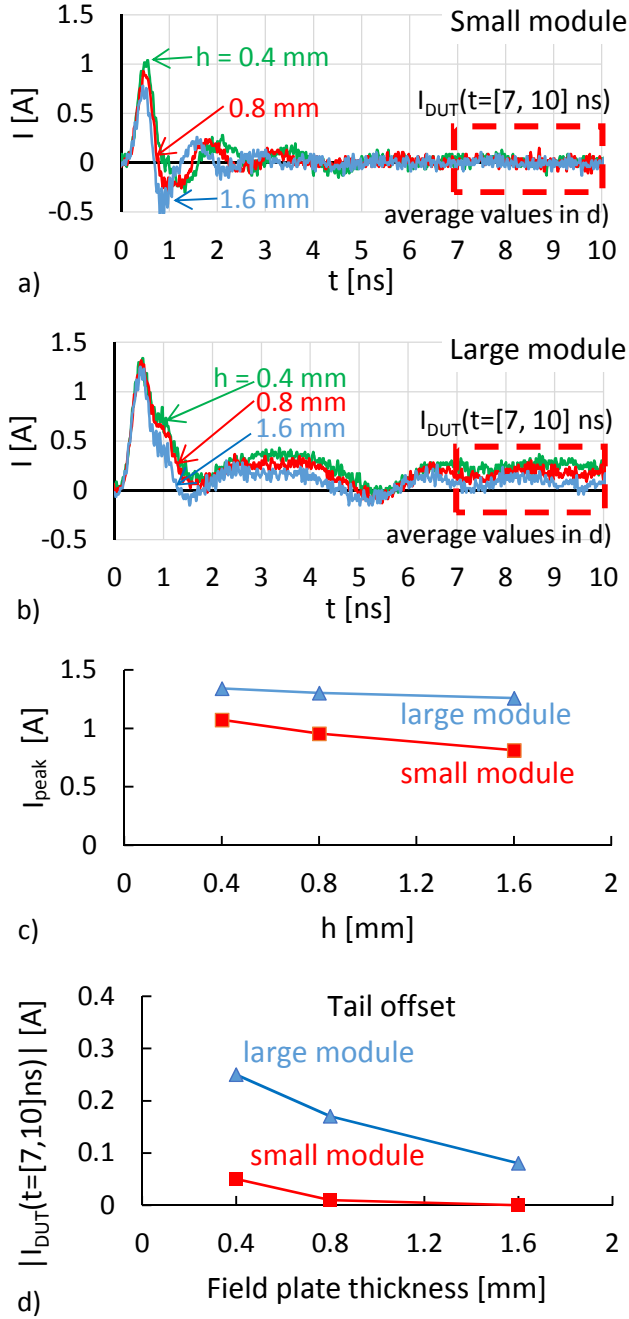


Figure 12 - LI-CCDM I_{DUT} waveforms for three FR4 thicknesses h measured using the 16.7Ω discharge head, a pre-charge V_{vTLP} of 100 V and the a) small and b) large JEDEC modules. Both c) I_{peak} and d) the tail offset are extracted and plotted as a function of h .

C. Chuck size

Another attempt to explore the impact of the wafer chuck onto the LI-CCDM waveform has been made using a smaller chuck. All measurement data shown so far have been acquired using a 200 mm wafer probing station. For this experiment, a 110 mm wafer probing station has been used and the results are compared in Figure 13.a and b. The chucks have been disconnected from ground during both measurements. The value of

the measured peak current I_{peak} is equal for both chucks. In case of the large JEDEC module, the pulse tail offset is slightly smaller for the 110 mm chuck. Also, a slight undershoot and a different impulse response is observed. This result suggests that the electrical chuck size can have an impact on the LI-CCDM measurement setup and should be taken into consideration, especially during the testing of large devices. However, the chuck size seems not to have a significant impact when the small module is used, as can be seen in Figure 13.b. Like for the thick dielectric in Section IV.A, the influence of the chuck parasitic impedances is smaller or negligible for small C_{DUT} values.

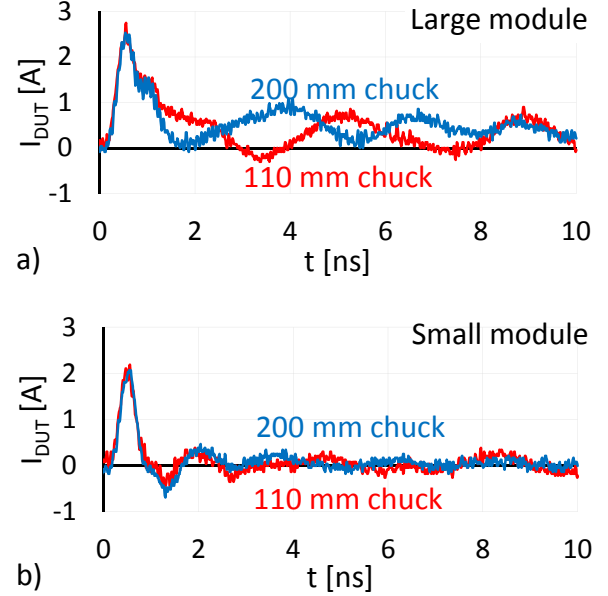


Figure 13 - 16.7Ω CCDM waveforms measured on a 200 mm and 110 mm floating wafer chucks for a pre-charge voltage V_{vTLP} of 200 V. Both a) the large and b) the small JEDEC modules have been measured.

V. LI-CCDM modeling

The LI-CCDM equivalent circuit model proposed in this section was inspired by the 5-capacitor equivalent FICDM model from [8]. However, two critical differences between the two setups exist. Firstly, for the LI-CCDM case, the ground and field plates are at the same potential and secondly, the probe-needle is connected directly to the vTLP and the oscilloscope. Figure 14 depicts the proposed LI-CCDM model.

The DUT capacitance towards the chuck C_{DUT} is the largest one and has the highest impact on the I_{DUT} . The DUT capacitance towards the ground plane C_g , is considerably smaller but crucial in shaping the LI-CCDM pulse. The probe impedances, L_p , C_p and R_p are also necessary to reproduce the CDM-like waveform. Furthermore, it is also necessary to understand the other parasitic impedances in order to build a reliable LI-CCDM tester.

effects like the tail offset and ripples are less evident. Figure 16.a shows a good match for the measured and simulated 16.7 Ω CCDM waveforms. However, the match is better for the 25 Ω CCDM setup (Figure 16.b). Two facts explain the better match for the 25 Ω case: firstly, the 25 Ω CCDM is a simpler setup and secondly, our model does not include the effect of SMA connectors which are present at all connection points. Without modeling the connectors, the additional 50 Ω termination in the 16.7 Ω CCDM setup (see Figure 12 and Figure 4) in our model appears without a transmission line.

Figure 17.a and b depict simulation results for different DUT capacitance C_{DUT} values. The tail offset for the large module and the peak current I_{peak} for the small module can be well reproduced comparing to measured data in Figure 12. This confirms that the chuck parasitic impedances do not affect small DUTs but should be further studied for the large ones.

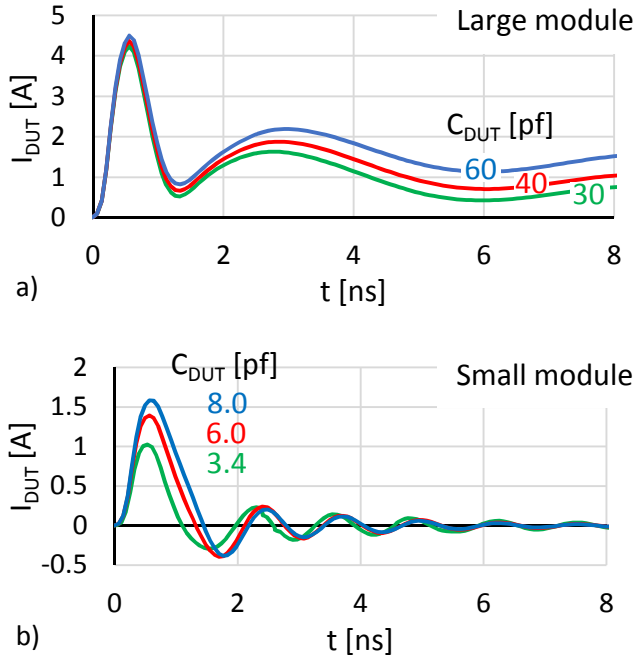


Figure 17 – Simulations for different C_{DUT} values for a) the large and b) the small module using the 25 Ω CCDM compact model.

VI. Wafer-level measurement

This last section reports on a wafer level measurement. The DUT for this experiment is a single p+/n-well diode on a full wafer. This diode itself is smaller than the small JEDEC module, so the observed current is also low. Interestingly, the fact that this diode is on a wafer, does not automatically make it a DUT with a large capacitance. Each one of the five waveform in Figure 18.a represents the average of five repeated measurements, to reduce the noise amplitude. The chuck grounding (grounded or floating) or the chuck

dielectric thickness (1.6, 0.4 or 0 mm) do not seem to have a strong impact on the diode current I_{DUT} . Like for the small JEDEC module, the tail offset is not present. Figure 18.b depicts the pulse tail mean value extracted by averaging the measurement points from 4 to 6 ns. In all five experiments, the offset absolute value is equal or smaller than 10 % compared to the I_{peak} .

The pulse tail offset is not observed even when the FR4 insulator is not used to isolate the wafer from the chuck. Clearly, the relatively high resistance of the wafer silicon substrate acts as an insulator in this experiment. This might change in case of a chip with a proper I/O ring and ESD protection circuits, where a larger amount of substrate contacts will reduce this resistance. Also, if measured on wafer-level, the capacitive coupling to neighboring chips might have an impact.

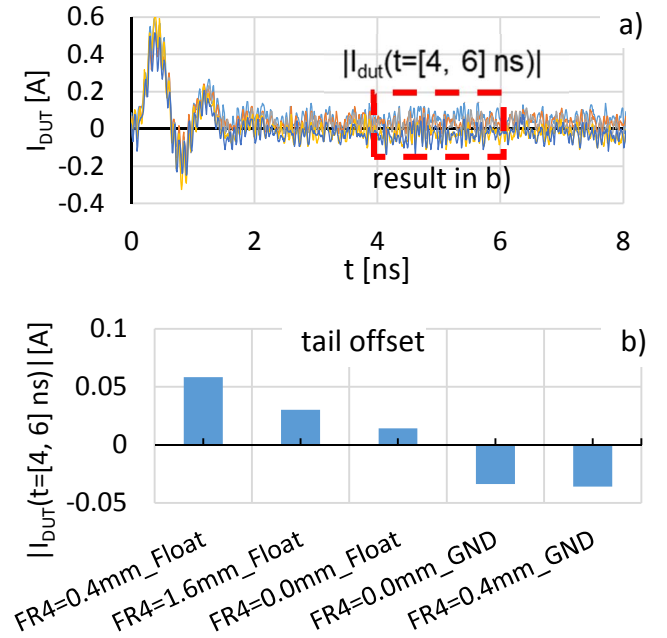


Figure 18 - Wafer level measurement of a p+ to n-well diode are taken for five different cases of chuck dielectric thickness (1.6, 0.4 or 0 mm) and chuck grounding (grounded or floating). The 16.7 Ω CCDM head and $V_{TLP} = 200$ V have been used for this measurement. a) The five depicted waveform each represent the average of five measurements, to reduce the measurement noise. The I_{peak} and tail offset difference in all five cases is minimal. b) The pulse tail offsets are extracted by averaging the measurement points from a), from 4 to 6 ns.

VII. Conclusions

We have presented a study of the 16.7 Ω and 25 Ω wafer-level LI-CCDM. We have shown that parameters like the wafer chuck dielectric and its ground connection can have a significant impact onto the LI-CCDM waveform. Decoupling the DUT from the chuck and its parasitic impedances can reduce the current tail offset. Also, we have proposed a model that can reproduce the measured waveforms to a certain

extent, including the current tail offset and ripples. Finally, a wafer-level LI-CCDM measurement has been shown as a proof of concept. This paper assumes that the wafer-level LICCDM and the packaged-device-level LICCDM are identical from the tester point of view. However, more measurements are needed to definitely confirm or reject this assumption.

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