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A High-Gain, Low-Voltage Operational Amplifier With Bias-Stress and PVT Robustness for Large-Area Temperature Sensing on LTPS Substrates

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ABSTRACT This paper analyzes the temperature coefficients of low temperature polysilicon (LTPS) devices and investigates critical blocks of a system architecture for large-area temperature sensing, which integrates sensors and readout circuits monolithically. As part of this system, a low-voltage folded-cascode (LV-FC) operational amplifier (OpAmp) with a class-AB output stage was designed and implemented using an LTPS thin film transistor (TFT) process on a 15 μm-thick polyimide flexible substrate. The performance of 20 amplifier samples was thoroughly characterized under DC, AC, long-term bias-stress (up to 40,000 seconds), and temperature conditions (0 °C to 80 °C). The amplifier achieves a maximum DC gain of 64.2 dB and a gain-bandwidth product of 400 kHz, while operating reliably under a 6 V supply with a peak power consumption of 0.6 mW in a compact area of 1.38 mm^2. Under bias stress, the gain degraded by only 2.5 dB and the offset shifted by 1.5 mV. Over the full temperature range, the average gain varied by less than 2 dB and the offset by under 6 mV. These results demonstrate strong robustness against PVT variations and prolonged stress, confirming the suitability of the proposed LV-FC amplifier for flexible, long-term, and large-area temperature sensing applications.

INDEX TERMS Flexible electronics, temperature sensing, large-area sensing systems, low temperature polysilicon (LTPS), thin film transistor (TFT), operational amplifier, folded-cascode amplifier.

I. INTRODUCTION

TEMPERATURE sensing has been widely adopted in various applications, as temperature is coupled to many physical, chemical, and biological processes [1]. Owing to the mature fabrication and continuous scaling, silicon-based temperature sensing systems dominate on-chip thermal monitoring [2] and biomedical diagnostics [3]. Nevertheless, emerging applications [4] that require large-area sensor arrays capable of conforming to complex, non-planar surfaces expose the limitations of rigid, high-cost silicon technologies. Such applications include bio-inspired robotics [5], photovoltaic solar cells, smart batteries [6], electronic skin [7], smart textiles [8], and wearable health patches [9], as illustrated in Fig. 1 and summarized in Table 1. To meet these new requirements, flexible thin-film electronics provide a cost-effective and mechanically

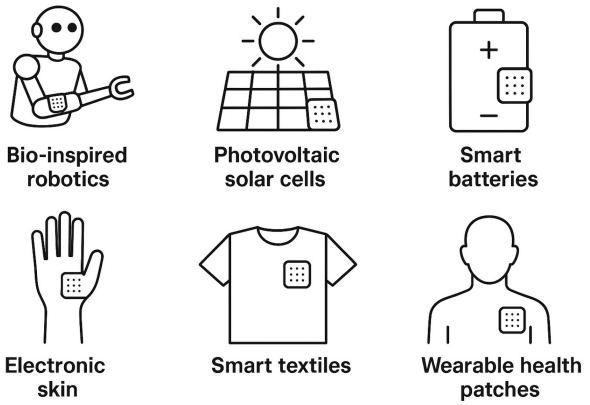

FIGURE 1. Applications of flexible large-area temperature sensing.

compliant solution, enabling conformal integration and large-area sensing beyond the limits of conventional silicon systems.

Despite the promise of flexible temperature sensing, several challenges remain in such systems. Foremost is the interconnection between the sensor array and the readout circuitry, which significantly limits array scalability [10]. At present, most flexible temperature sensors are ink-jet printed on polymer foils [11], [12], whereas high performance thin-film-transistor (TFT) readout circuits must still be deposited and photolithographically patterned on separate substrates [13], [14]. Fig. 2(a) illustrates such an architecture: the printed sensor matrix is flex-bonded to a TFT backplane that contains analog multiplexers (AMUX), an analog front-end (AFE), and an analog-to-digital converter (ADC). Although an AMUX reduces routing complexity within the readout circuits, each sensor still requires a dedicated trace to the bonding pad, consuming valuable area and constraining pitch. A scalable solution is to monolithically integrate the sensor array and the readout chain on the same flexible substrate [15] as depicted in Fig. 2(b). Realizing this integration demands a thorough understanding of TFT temperature behavior so that accurate on-chip sensing elements can be designed on chip.

Another critical challenge in flexible electronics is designing circuits that combine high performance with immunity to process, voltage, and temperature (PVT) variations. Among various thin-film technologies, low-temperature polycrystalline silicon (LTPS) offers high carrier mobility (50–100 $cm^2 \cdot V^{-1} \cdot s^{-1}$), excellent device stability, and compatibility with standard CMOS design methodologies [16]. Therefore, it is well suited for temperature-sensing systems that require high accuracy, fast response, and operating under a wide temperature range. In contrast, indium–gallium–zinc oxide (IGZO) technology provides solely n-type devices and suffers from lower mobility ($\sim$10 $cm^2/V \cdot s$) and strong photosensitivity [17], which degrades its reliability in thermally dynamic and light-exposed environments. Based on LTPS technology, several high-performance analog building blocks have been demonstrated [18], [19], [20], [21].

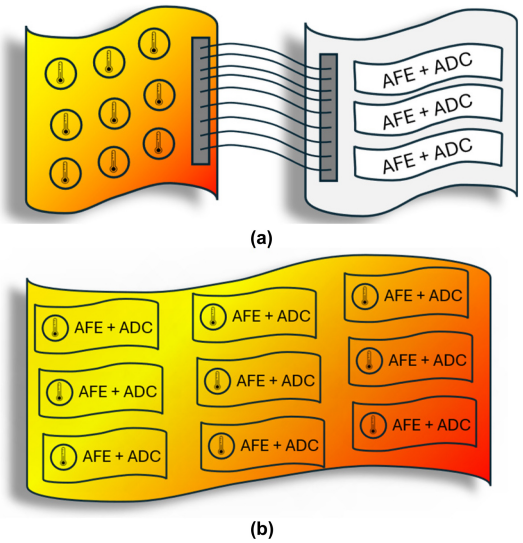

FIGURE 2. Comparison between (a) conventional temperature sensing system with flex-bonded sensors and readout circuits, and (b) monolithically integrated temperature sensor and readout circuits.

TABLE 1. Key specifications for various flexible large-area temperature sensing applications.

Application	Area	Accuracy	Response Speed
Bioinspired Robotics	Medium-Large	High	Fast
Smart Battery/ Solar Cells	Large	Low	Slow
Electronic Skin	Medium-Large	High	Fast
Smart Textiles	Large	Medium	Slow
Wearable Patch	Medium	Medium	Medium

However, most are designed for nominal conditions and lack validation under temperature variation. Since analog circuit performance can degrade significantly under PVT fluctuations, developing a PVT-robust and bias-stress-stable remains an essential and open challenge.

The authors' earlier study [22] compared several LTPS operational-amplifier (OpAmp) architectures for large-area temperature sensing. Building on that foundation, this paper first provides a detailed characterization of the temperature dependence of LTPS devices, and then analyzes the operating principles of two key building blocks in a temperature sensing system: a monolithically integrated temperature sensor and a low-voltage folded-cascode (LV-FC) OpAmp with a class-AB output stage. Comprehensive measurement results are presented, demonstrating its PVT robustness, bias-stress stability, and suitability for low-voltage high-accuracy flexible sensing applications. The remainder of this paper is organized as follows. Section II analyzes the temperature characteristics of LTPS devices. Section III explains the operating principles of the proposed sensor and the OpAmp. Section IV reports comprehensive DC, AC, bias-stress, and temperature measurements. Section V compares

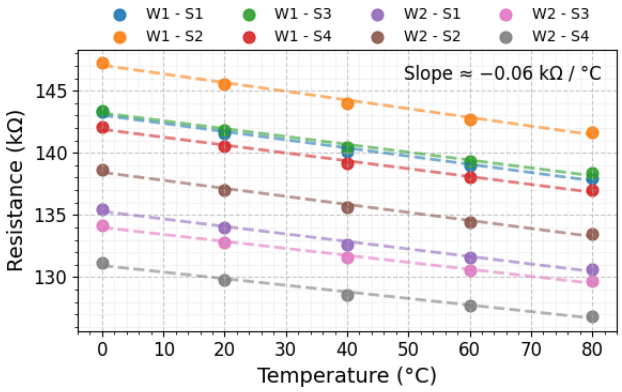

FIGURE 3. Measured resistance vs. temperature curves of eight polysilicon resistors (S1–S4 on each of two plates, W1 and W2).

the proposed design with state-of-the-art thin-film OpAmps, and Section VI concludes the paper.

II. TEMPERATURE CHARACTERISTICS OF LTPS DEVICES

Understanding the temperature dependence of LTPS devices is essential for designing accurate temperature sensors and thermally robust AFEs. Accordingly, this section analyzes the thermal behavior of the two devices most frequently employed in LTPS processes: polysilicon resistors (thermistors) and thin-film transistors.

A. THERMISTOR TEMPERATURE CHARACTERISTICS

The total resistance R of a polysilicon resistor is given by [23]:

$$R = R_{\mathrm{C}} + R_{\mathrm{silicide}} + \frac{L}{W}R_{\mathrm{bulk}} + \frac{W_0}{W}R_{\mathrm{interface}} \tag{1}$$

where R_{C} and R_{silicide} are the effective contact and silicide resistances, R_{bulk} represents the resistance from the polysilicon grain interior, and $R_{\mathrm{interface}}$ accounts for grain-boundary and surface effects. Note that R_{silicide} does not exist in LTPS processes and is therefore excluded from the analysis. L and W are the physical length and width, and $W_0 = 1\ \mu$m is a normalization factor to preserve dimensional consistency. Since R_{C} is typically negligible, it is omitted in the temperature-coefficient analysis. The temperature coefficient of resistance (TCR) is obtained as:

$$\mathrm{TCR} \approx \frac{1}{W}\frac{1}{R}\left[\left(\frac{\partial R_{\mathrm{bulk}}}{\partial T}L\right) + \left(\frac{\partial R_{\mathrm{interface}}}{\partial T}W_0\right)\right] \tag{2}$$

The TCR is dominated by the temperature coefficients of R_{bulk} and $R_{\mathrm{interface}}$ and shows a strong dependence on the resistor geometry.

Fig. 3 plots the measured resistance of eight p-type polysilicon thermistors fabricated in the LTPS process on large-area flexible substrates. Dots indicate measured data; dashed lines represent linear fits. Each device was designed for $R(20°\mathrm{C}) = 140$ kΩ with $L = 632\ \mu$m and $W = 20\ \mu$m. At 20 °C, the measured resistance averages 137.9 kΩ with a standard deviation of 5.4 kΩ (3.9% of nominal). The variation is dominated by wafer-to-wafer mismatch: resistors on wafer W1 are on average ≈ 9 kΩ higher than those at the same locations on wafer W2. Linear regression over the full 0–80 °C range yields a minimum coefficient of determination $R^2 = 0.988$ for the eight devices and a maximum linearity error of 2.03%. The fitted slope of –0.06 kΩ/°C, corresponds to a negative TCR of –449 ppm/°C with $\sigma_{\mathrm{TCR}} = 24$ ppm/°C.

Although such polysilicon resistors enable compact and low-power temperature sensors for moderate-accuracy applications, their linearity remains insufficient for high-precision use. Consequently, additional calibration is required to meet stringent accuracy requirements [1].

B. TRANSISTOR TEMPERATURE CHARACTERISTICS

Besides polysilicon thermistors, temperature sensing can also be realized by transistor structures based on the thermal dependence of TFT electrical parameters, such as threshold voltage (V_{th}) and carrier mobility (μ_0) [24].

The temperature dependence of the threshold voltage V_{th} can be derived from the MOSFET model [24], [26]. In this model:

$$V_{\mathrm{th}} = V_{\mathrm{FB}} + 2\phi_{\mathrm{f}} + \sqrt{\frac{4\varepsilon_{\mathrm{ch}} q N \phi_{\mathrm{f}}}{C_{\mathrm{ox}}}} \tag{3}$$

where V_{FB} is the flat-band voltage, ϕ_f is the potential difference between the Fermi level and intrinsic level, $\varepsilon_{\mathrm{ch}}$ is the permittivity of the LTPS channel, q is the elementary charge, C_{ox} is the oxide capacitance per unit area, and N is the doping concentration. Among these terms, φ_f is an important factor deciding the thermal shift of V_{th}, defined by:

$$\frac{d\phi_f}{dT} = \frac{k_B}{q}\left(\ln\left(\frac{N}{n_{\mathrm{i}}}\right) - \frac{T}{n_{\mathrm{i}}}\frac{\partial n_{\mathrm{i}}}{\partial T}\right) \tag{4}$$

where n_{i} is the intrinsic carrier concentration, k_B is Boltzmann's constant.

Measurements show that $|V_{\mathrm{th}}|$ in LTPS generally exhibits a negative temperature coefficient (NTC) in the range of –2.5 mV/°C to –6 mV/°C [15] [24]. Taking nominal $|V_{\mathrm{th}}|$ values of 0.8 V for N-TFTs and 2.5 V for P-TFTs, these slopes translate to temperature coefficients k_{Vth} of approximately –3100 to –7500 ppm/°C for N-TFTs, and –1000 to –2400 ppm/°C for P-TFTs.

Carrier mobility in LTPS TFTs also varies with temperature, which can be analyzed through carrier trapping and releasing at grain boundaries [27]. The effective mobility μ_{eff} can be derived as:

$$\mu_{\mathrm{eff}} = L_{\mathrm{grain}} q \sqrt{\frac{1}{2\pi m^* k_B T}} e^{\frac{-E_B}{k_B T}} \tag{5}$$

where E_B is the energy barrier height between two grains, L_{grain} is the grain size, and m^* is the effective carrier mass. Experimental data show μ_{eff} decreases with temperature at a slope of around –0.12 $\mathrm{cm^2V^{-1}s^{-1}/°C}$ for P-TFTs on glass substrate and –0.05 $\mathrm{cm^2V^{-1}s^{-1}/°C}$ for

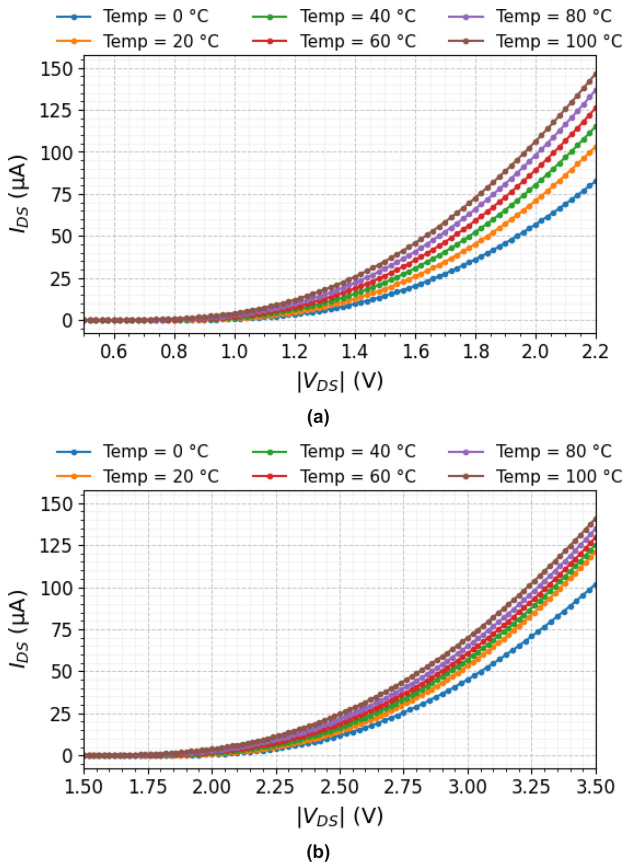

FIGURE 4. I_{DS}–V_{DS} curves of diode-connected (a) N-TFT and (b) P-TFT measured at temperatures from 0 °C to 100 °C.

TABLE 2. Temperature linearity of the drain current in diode-connected N-TFT and P-TFT at different V_{DS}.

Device	|V_{DS}| (V)	Slope (nA/°C)	Intercept at 0 °C (μA)	R^2
N-TFT	0.5	0.16	-0.002	0.818
	0.8	7.69	-0.010	0.927
	1.2	8.51	3.174	0.992
	1.5	20.33	14.425	0.999
	2.2	61.63	87.599	0.980
P-TFT	1.5	0.34	-0.006	0.772
	1.9	1.83	0.093	0.957
	2.2	6.43	2.689	0.992
	3.5	24.60	112.300	0.994

those on flexible substrates. In contrast, N-TFTs on glass exhibit a positive temperature coefficient with a slope of approximately +0.05 $cm^2V^{-1}s^{-1}/°C$ [24], [28]. Normalized to room-temperature mobility, these slopes correspond to temperature coefficients of roughly –2000 ppm/°C on glass and –1000 ppm/°C on flexible substrates for P-TFTs, and approximately +800 ppm/°C for N-TFTs on glass.

Both $V_{th}(T)$ and $\mu_0(T)$ directly modulate TFT drain currents, which can be modeled by [25]:

$$I_{DS} = \frac{\mu_0 C_{ox}}{2}\frac{W}{L}\left(V_{GSTe}^2 - V_{GDTe}^2\right)(1 + \lambda V_{DS}) \quad (6)$$

where W/L is the channel width-to-length ratio, λ models the channel length modulation. The mobility enhancement factor is excluded as trap-state filling in IGZO does not occur in LTPS, which is limited by grain-boundary. To capture subthreshold behavior, effective gate-source and gate-drain voltages V_{GSTe} and V_{GDTe} are defined using an asymptotic interpolation method:

$$V_{GXTe} = 2SS\log_{10}\left(1 + 10\text{^}\left(\frac{V_G - V_X - V_{th}}{2SS}\right)\right) \quad (7)$$

where SS is the subthreshold slope, and X represents the source or drain terminal.

Fig. 4 presents the measured I_{DS}-V_{DS} curves of a diode-connected N-TFT and P-TFT with a channel dimension of 150 μm/5 μm. In both cases, the drain current I_{DS} increases with temperature, consistent with the behavior reported in [24], [28], suggesting its potential use as a temperature sensor. The temperature linearity of the transistor is summarized in Table 2. As |V_{DS}| increases beyond threshold, the temperature sensitivity (slope) increases significantly, accompanied by good linearity ($R^2 > 0.99$). Notably, for the N-TFT, linearity begins to degrade when |V_{DS}| exceeds approximately $2V_{th}$.

III. LTPS TEMPERATURE SENSING SYSTEM

Fig. 5 depicts the conceptual architecture of a proposed LTPS temperature-sensing system. The system consists of N readout channels, each equipped M temperature sensors. Every sensor is implemented on chip by a thermally drifting current source and can be sequentially addressed by an analog multiplexer (AMUX). The selected sensor current is fed to a shared readout circuit that includes (i) a transimpedance amplifier (TIA) for current-to-voltage conversion and (ii) a Δ-Σ ADC for digitization. In this configuration, the sensor current is converted into a voltage by impedance gain of R_F. Negative feedback maintains the OTA input at the common-mode voltage V_{CM}, and the output V_{OUT} for an ideal TIA follows:

$$V_{OUT} = V_{CM} - I_{SENSOR}(T) \cdot R_f \quad (8)$$

After scanning all sensors, the system reconstructs an N × M thermal map that updates in real time. As both the sensors and readout circuitry are on the same LTPS substrate, no additional integration steps are required, thereby simplifying assembly and enabling large-area sensing.

In the case of a non-ideal TIA, a feedback capacitor C_F can be added in parallel with R_F to improve stability and transient response. Accordingly, the system response is expressed as:

$$V_{OUT} = V_{CM} - I_{SENSOR}(T) \cdot Z_{CL} \quad (9)$$

where Z_{CL} denotes the closed-loop transfer function of the TIA derived from the signal flow graph (SFG):

$$Z_{CL} = R_F \cdot \left(\frac{1}{1 + sR_FC_F}\right) \cdot \left(\frac{F \cdot A_{OL}}{1 + F \cdot A_{OL}}\right) \quad (10)$$

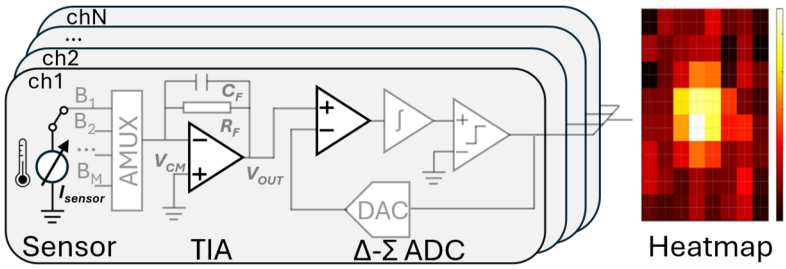

FIGURE 5. Conceptual architecture of the proposed temperature sensing system, with implemented sensor and OpAmp highlighted.

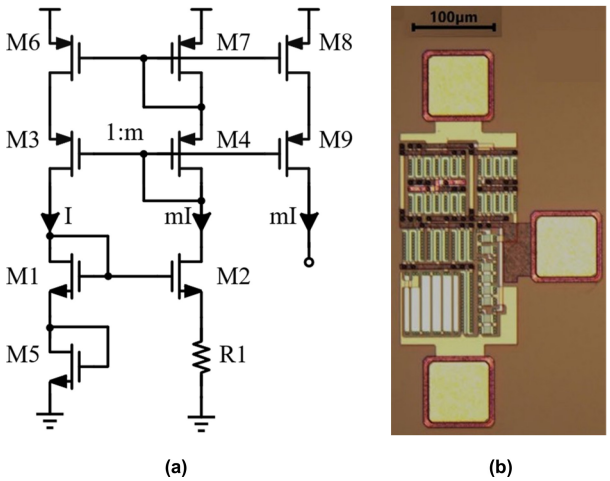

FIGURE 6. (a) Schematic of the current source with thermal drift used for temperature sensing, and (b) corresponding micrograph [15].

$$F = \frac{Z_{\text{SENSOR}}}{Z_{\text{SENSOR}} + Z_F} \tag{11}$$

where F represents the feedback factor, Z_F is the feedback impedance ($Z_F = R_\text{F} \,//\, C_\text{F}$), and Z_{SENSOR} is the inherent source impedance of the current sensor. Since the current source exhibits a significantly large impedance, F is approximated to be one. Consequently, the loop gain depends solely on the open-loop behavior A_{OL} of the OpAmp.

The remainder of this section first details the operating principle of the temperature sensor, implemented as a thermally drifting current source I_{SENSOR}. We then present a high-performance OpAmp topology for the TIA, which largely determines the system's accuracy, bandwidth, and power consumption. The amplifier employs a folded-cascode (FC) structure to achieve high gain at low supply voltage, complemented by a low-voltage class-AB output stage to improve power efficiency and further reduce the supply.

A. LTPS TEMPERATURE SENSOR

The current source circuit shown in Fig. 6 [15], [29] functions as a temperature sensor using the thermal drift of its output current. All transistors are biased in the saturation region, so the subthreshold factor (SS) can be neglected. For simplification, the channel length modulation (λ) is also not considered. The I-V formula is simplified to the classical square-law form:

$$I_{\text{DS}} = \frac{\mu_0 C_{\text{ox}}}{2} \frac{W}{L} (V_{\text{GS}} - V_{\text{th}})^2 \tag{12}$$

Applying Kirchhoff's voltage law (KVL) to the loop consisting of M1, M5, M2, and R_1 yields:

$$V_{GS1} + V_{GS5} - V_{GS2} - mR_1 I = 0 \tag{13}$$

which can be rearranged to:

$$\sqrt{\frac{I}{\beta_{\text{n0}}}} \left(\frac{1}{\sqrt{\alpha_1}} + \frac{1}{\sqrt{\alpha_5}} - \sqrt{\frac{m}{\alpha_2}} \right) + V_{\text{th,n}} - mR_1 I = 0 \tag{14}$$

where $\beta_{\text{n0}} = \mu_{\text{n0}} C_{\text{ox}}/2$ is the current factor, and $\alpha_\text{i} = W_\text{i} \,/L_\text{i}$ represents the aspect ratio of transistor M_i. The same size ratios are used for M1, M2, and M5: $\alpha = \alpha_1 = \alpha_2 = \alpha_5 =$ 160 μm/ 5 μm. The current mirror ratio m is set to one by sizing $\alpha_3 = \alpha_4 = \alpha_6 = \alpha_7 =$ 100 μm / 5 μm. Under these conditions, (14) is simplified to:

$$IR_1 = \frac{1}{\sqrt{\alpha}} \cdot \sqrt{\frac{2I}{\mu_{\text{n0}} C_{\text{ox}}}} + V_{\text{th}} \tag{15}$$

The temperature-dependent terms in (14) are μ_{n0}, V_{th}, and R_1. Defining the temperature coefficient of any quantity X as:

$$k_\text{X} = \frac{1}{X} \frac{\text{d}X}{\text{d}T} \tag{16}$$

the temperature coefficient of the reference current (k_I) can be derived as [29]:

$$k_\text{I} = \frac{(2k_{\text{Vth,n}} + k_{\mu n,0}) V_{\text{th,n}} - (2k_{R_1} + k_{\mu_{\text{n0}}}) IR_1}{V_{\text{th,n}} + IR_1} \tag{17}$$

Using the representative parameters within the range derived in Section II: $k_{\text{Vth}} = -5000$ ppm/°C, $k\mu_{n,0} = +800$ ppm/°C (for N-TFT on glass), $k_{R1} = -449$ ppm/°C, $V_{\text{th,n}} = 0.8$ V, $I = 10$ μA, and $R_1 = 140$ kΩ, the resulting temperature coefficient is $k_\text{I} = -3282$ ppm/°C.

As shown in Fig. 7, the measured current from five current-cell replicas (S1–S5) exhibits excellent linearity across temperature. Each curve was fitted with a linear regression over the 0–80 °C range. The fitted slopes range from –23.2 to –27.1 nA/°C, averaging –25.4 nA/°C, corresponding to a temperature coefficient of $k_\text{I} = -2540$

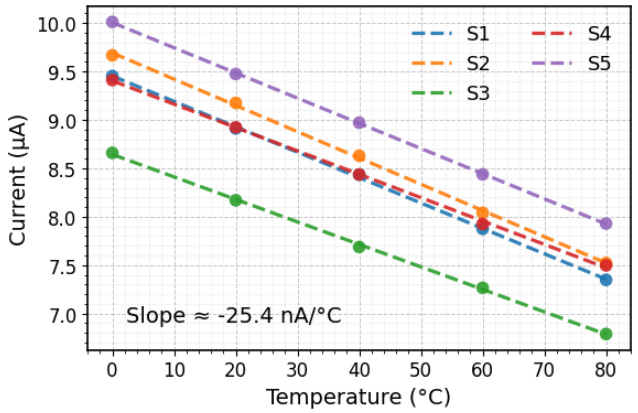

FIGURE 7. Measured temperature dependence of the thermal-drift current source used in temperature sensing.

ppm/°C. The discrepancy in k_1 between the calculation and measurement is expected, as the calculation is a back-of-the-envelope estimate that does not account for process differences. All devices achieve $R^2 \geq 0.9992$, with maximum linearity error below 1.65 % of full-scale.

The large device-to-device offset of the sensor can dominate the temperature-sensing error. Therefore, a one-point calibration at a reference temperature is required to remove the dominant offset by anchoring each sensor's transfer curve. This calibration compensates offsets from both the sensor and its interface circuitry (TIA and OpAmp), significantly improving overall accuracy. The remaining error is mainly determined by slope variations. For higher precision, a two-point calibration can be applied to extract both offset and gain from two reference points, leaving only minor residual errors due to nonlinearity.

B. LTPS LOW-VOLTAGE FOLDED-CASCODE OPAMP WITH CLASS-AB OUTPUT STAGE

The thermally drifting sensor current is converted to voltage by a single-ended TIA, whose input common-mode is set by an external reference, while output voltage change is determined by the sensed current. Fig. 8 shows the schematic of the implemented LV-FC OpAmp used for the TIA, with a class-AB output stage [22], [30].

A P-type differential pair forms the input stage. The differential currents are steered into two cascode branches biased by M26 and M27, to achieve high gain under a reduced supply voltage. The drain terminals of transistors M18 and M22 connect to the gates of the output transistors M11 and M20, respectively, generating the bias voltages required for class-AB operation. As the output current varies, the gate voltage of M22 changes accordingly, modulating its drain current. This results in an equal but opposite change appears in M18. To keep M17 at the same operation point as M18, transistor M21 mirrors the current from M22 into the M17 branch, which removes the output-dependent current variations to the folded-cascode current-mirror paths.

The output pair M11 and M20 operates in push-pull mode, with M11 sourcing and M20 sinking current. The output currents are sensed by M10 (for M11) and M19 (for M20). To ensure stable operation at minimal quiescent current, a minimum selector circuit is formed by M10, M14, M15, M19, and M23. This selector, together with the sensing transistors M10 and M19, makes a feedback loop to dynamically bias the output stage.

When the sinking current of M20 approaches zero, the sensing current in M19 decreases accordingly. This reduced current is mirrored by the cascode structure (M10, M14, M15) to the diode-connected transistor M23. As the current through M23 falls, its gate-source voltage decreases. This change is then fed back through the common-source amplifier M22 to adjust the gate voltage of M20, ensuring a minimal standby current is maintained.

Conversely, when the sourcing current from M11 decreases, M10 senses the reduction and mirrors it through the cascode structure. The differential pair M18 and M22 then adjust the gate voltages of M11 and M20, respectively, preserving the proper bias under low-current conditions.

This feedback network allows the class-AB stage to adaptively regulate its quiescent current, combining low-static power with sufficient dynamic drive capability. The minimum supply voltage is set by one gate–source voltage of M11 ($\approx$ 2.5 V) plus two saturation voltages to bias M18 and M27 ($\approx$ 1 V each), yielding a lower limit of supply voltage approximately 4.5 V. Further reduction is possible by using low-voltage architectures such as inverter-based or bulk-driven OTAs.

IV. MEASUREMENT OF LTPS LOW-VOLTAGE FOLDED-CASCODE OPAMP

Fig. 9 shows the micrograph of the fabricated LV-FC OpAmp and the photograph of its 15-μm-thick polyimide flexible substrate. The IBIAS is used to generate all bias voltages, as shown in Fig. 8. A total of 20 instances of the proposed OpAmp were characterized on a probe station, with four instances placed on each of the five plates. DC measurements were conducted using a Keysight B1500 parameter analyzer, which provided the supply voltages (VDD = 5, 6, and 7 V), generated the DC input signals, sourced the 5 μA bias current, and measured the output voltage, current, and power consumption. For AC characterization, a Rigol DG5252 arbitrary waveform generator (AWG) was employed to supply the AC input signals, and a Tektronix MDO3000 mixed domain oscilloscope was used to capture the AC output waveforms for frequency-response calculation. To assess the thermal stability of the chip, the samples were characterized in an ATT thermal chuck system for precise temperature control. The circuit was extensively evaluated in terms of DC behavior, AC frequency response, long-term bias stress stability, and performance under temperature variation. Fig. 10 illustrates the measurement setup used for the evaluation.

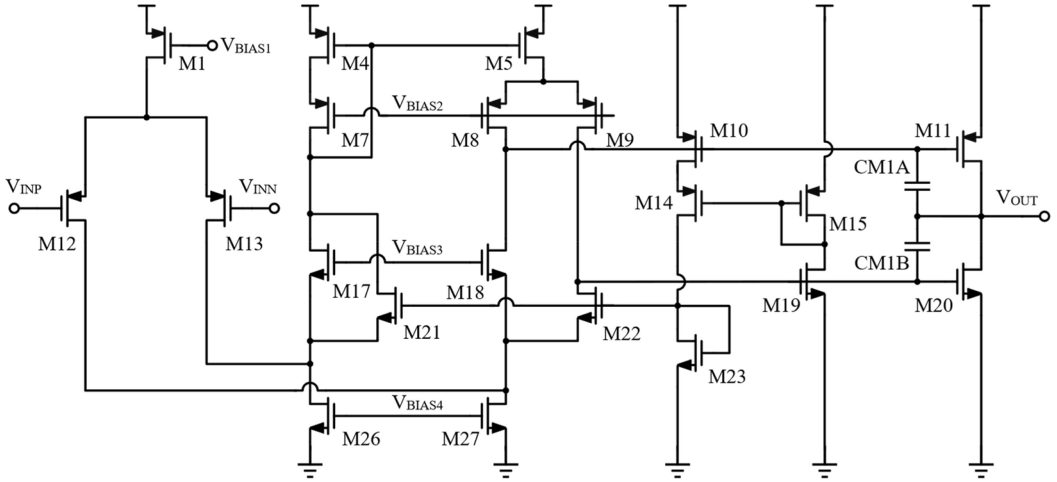

FIGURE 8. Schematic of the LV-FC OpAmp with a class-AB output stage [22].

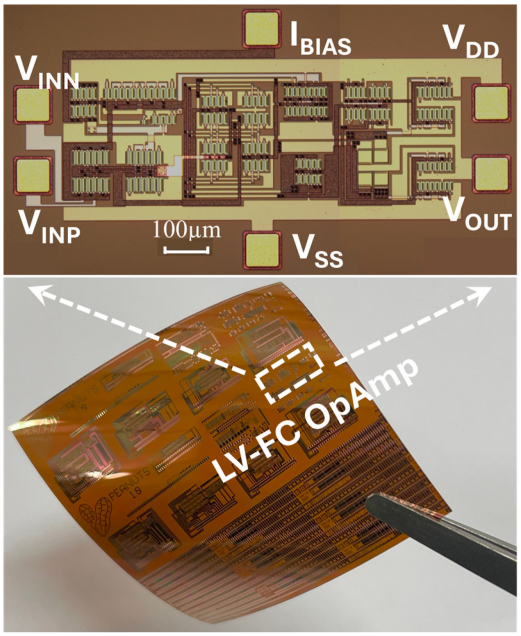

FIGURE 9. Micrograph of the low-voltage folded-cascode OpAmp, and photograph of the flexible plate [22].

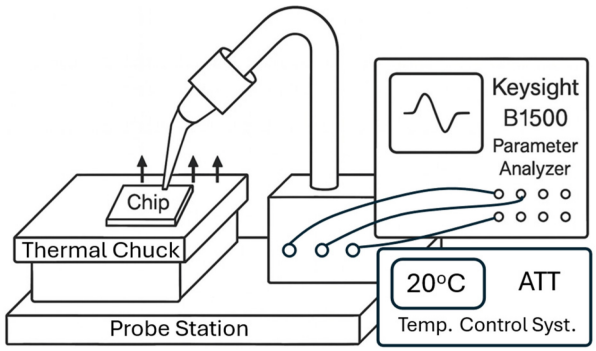

FIGURE 10. Test setup for the LV-FC OpAmp.

A. DC MEASUREMENTS

The DC performance of the LV-FC OpAmp was characterized at room temperature (20 °C). During the test, a differential input signal (V_{IN}) was applied between the V_{INP} and V_{INN} terminals, swept from –20 mV to +20 mV in a 1 mV step, with the input common-mode voltage V_{CM} of half of the supply voltage $V_{DD}/2$. The DC gain was extracted from the slope of the V_{OUT} vs. V_{IN} curves at the operating point $V_{OUT} = V_{DD}/2$, while the input offset voltage was determined as the V_{IN} differential value under the same condition.

Fig. 11 presents the measured gain and offset variations across 20 samples. A significantly larger spread is observed at a 5 V supply, which is because the supply voltage is approaching the circuit's minimum operating voltage (~4.5 V). Under such marginal conditions, inherent variations in LTPS TFTs can push transistors out of their intended operating region, resulting in degraded and inconsistent performance. In contrast, higher supply voltages (6 V and 7 V) provide greater design margin and yield more stable behavior. At 6 V supply, the measured average DC gain is 60.03 dB with $\sigma_{Gain} = 2.24$ dB, and the input offset is –25.4 mV with $\sigma_{offset} = 19$ mV (after removing one outlier marked by red ×). The maximum and minimum gains observed were 64.2 dB and 55.65 dB, respectively. When used in a TIA with $F \approx 1$, finite OpAmp gain introduces a closed-loop transimpedance error of $1 / (1 + A_{OL})$. Using the minimum measured gain, the worst-case error is around 0.16%. With a 7 V supply, the average gain is 59.98 dB with $\sigma_{Gain} = 2.28$ dB, and the intrinsic offset is –7.79 mV with $\sigma_{offset} = 20.45$ mV (after removing the same outlier). While the gain of LTPS TFT-based circuits is fundamentally limited by the low mobility of the devices, transconductance enhancement techniques can be applied to further improve performance, such as using conjugated current mirrors, positive feedback, and nonlinear tail current [31], [32].

The statistical performance of circuits is limited by large variations in LTPS TFTs, resulted from the random grain

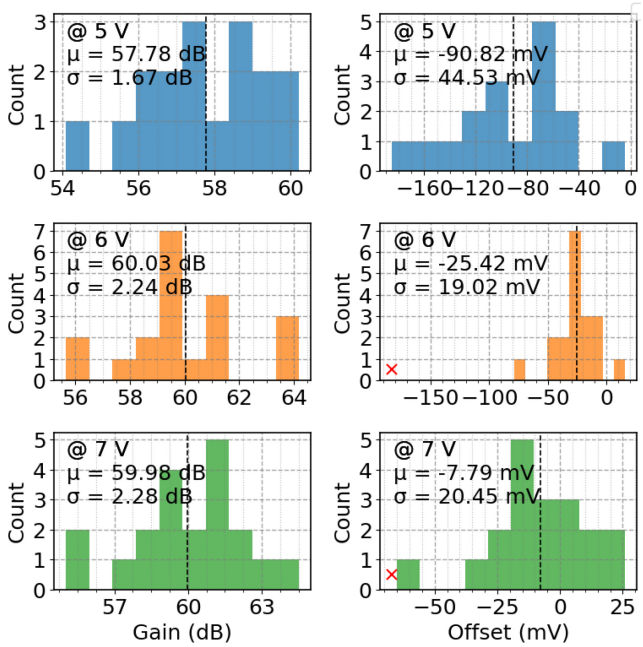

FIGURE 11. Gain and offset histograms of 20 OpAmp devices at supply voltages of 5 V, 6 V, and 7 V.

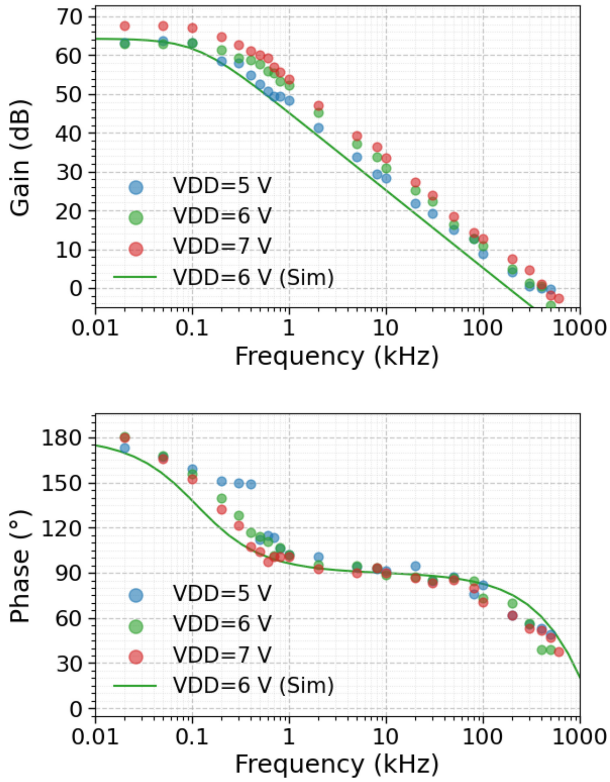

FIGURE 12. AC response of the low-voltage OpAmp measured under different supply voltages with a fixed bias current of 5 μA.

distribution in the polysilicon film. Such offset variations can significantly impair temperature sensing resolution. While static trimming techniques such as adjusting current mirror symmetry or tuning back-gate bias can mitigate systematic offsets, they generally lack the precision due to their discrete adjustment steps and are not adaptable enough to compensate for long-term drift. In contrast, dynamic offset cancellation methods, such as auto-zeroing and chopping, are more effective in suppressing both offset and drift. In auto-zeroing, the amplifier periodically samples its offset on capacitors and subtracts it in the next phase. In chopping, the input signal is modulated to a higher frequency, amplified, and demodulated back, while the offset and $1/f$ noise are shifted to the chopping frequency and removed by the low-pass filtering. These techniques can be implemented separately at system level to greatly reduce offset and drift.

B. AC MEASUREMENTS

Once the input offset has been determined and after proper biasing and offset calibrations, a differential small-amplitude sine wave was applied to the V_{INP} and V_{INN} terminals. The output signal's amplitude and phase were recorded using an oscilloscope, from which the gain and phase response over frequency were derived.

Fig. 12 presents the measured frequency response of the OpAmp under different supply voltages. At a supply voltage of 6 V, the circuit exhibits a bandwidth of 300 Hz, a gain bandwidth product of 400 kHz, and a phase margin of 40°. A small increase in both gain and bandwidth is observed as the supply voltage increases.

In the temperature-sensing system, the OTA operates within a closed-loop TIA rather than in open-loop mode. In this configuration, the feedback resistor sets the transimpedance gain, while the resistor–capacitor pair defines the dominant pole and thus the closed-loop bandwidth. When the OTA's unit-gain bandwidth (UGB) is well above this pole, the TIA performance is primarily determined by the feedback network. Therefore, with a sufficiently large UGB, the TIA behaves as a single-pole system, providing stable and robust amplification determined by the passive components.

C. BIASING STRESS MEASUREMENTS

Reliable long-term operation is essential for temperature sensing applications. However, the I–V characteristics of TFTs can drift under continuous bias stress [33], causing transistors to deviate from their intended operating regions and thus impair circuit performance. To evaluate long-term stability, the LV-FC OpAmp was biased at a 6 V supply for 40,000 seconds (667 minutes) at 20 °C, with a DC measurement per 84 seconds.

Fig. 13 measured the output voltage V_{OUT} versus differential input ΔV_{IN} during 667 minutes of bias-stress testing. Initially, the curves show a steep transition region, indicating high amplifier gain. Over time, this slope becomes more gradual, reflecting a modest decrease in gain before stabilizing toward the end of the test.

In Fig. 14, each horizontal line represents a complete $V_{\mathrm{OUT}} - \Delta V_{\mathrm{IN}}$ sweep at a given time point, with pixel color indicating the output voltage corresponding to each ΔV_{IN}. Initially, the offset increases continuously during the first

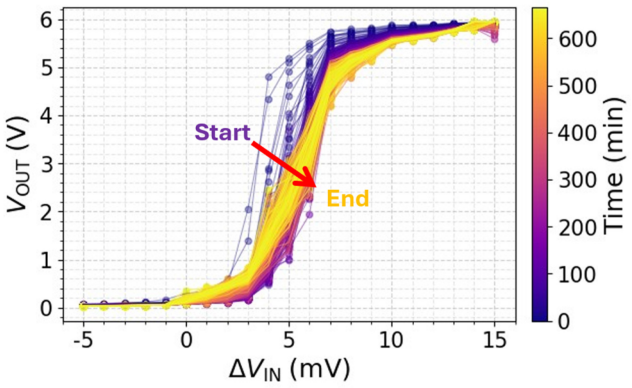

FIGURE 13. Measured V_{OUT} vs. ΔV_{IN} curves over 40,000 seconds under 6V power supply bias-stress stability testing.

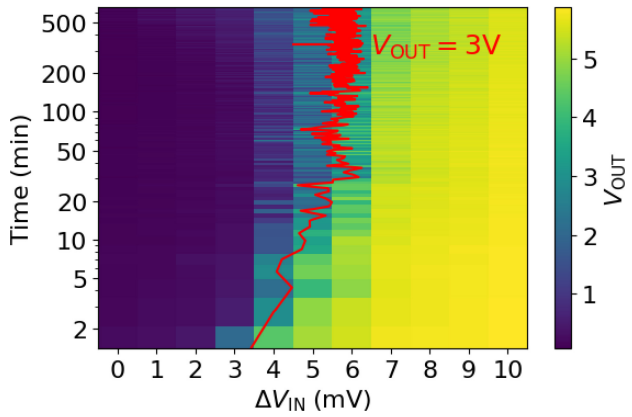

FIGURE 14. Time evolution of V_{OUT} vs. ΔV_{IN} characteristics under 40,000-second bias-stress testing, visualized as a heatmap.

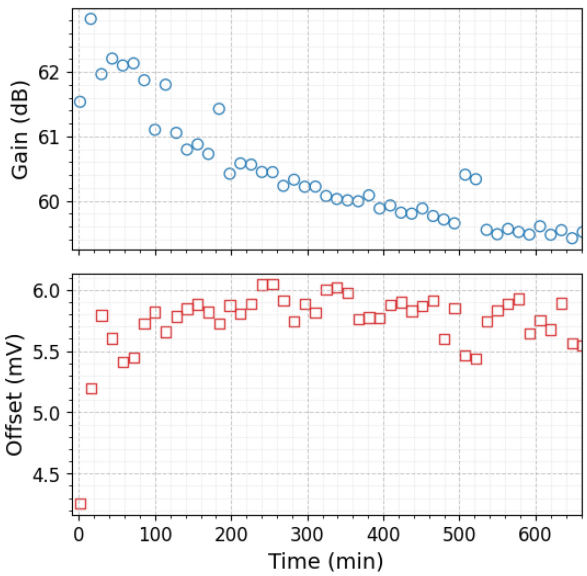

FIGURE 15. Time evolution of gain and offset during continuous 40,000-second bias-stress testing under a 6 V supply.

30 minutes, reaching approximately 5.5 mV at the 30-minute mark. After that, the offset tends to stabilize. The long-term fluctuations in offset could be attributed to the relatively large

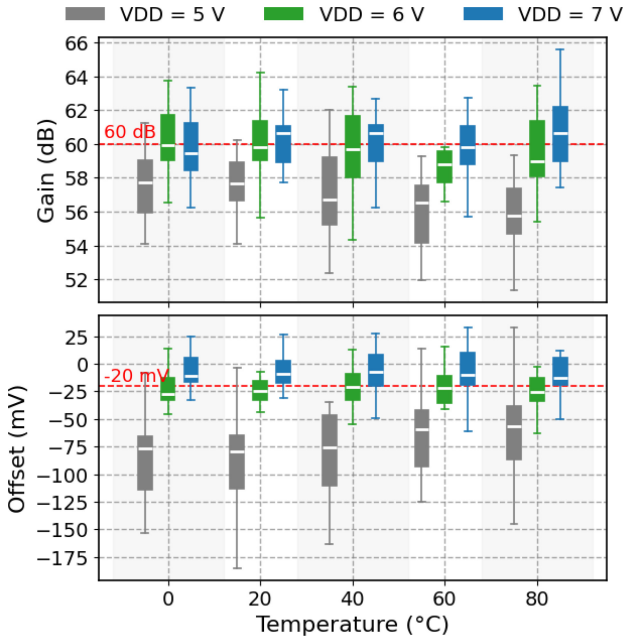

FIGURE 16. Gain and offset variation of 20 OpAmp devices over a 0–80 °C temperature range and supply voltages of 5 V, 6 V, and 7 V.

step size (1 mV) of the V_{IN} during measurement, which may introduce interpolation error when determining the offset.

To further validate the bias stress stability of the circuit, the time evolution of gain and offset is summarized in Fig. 15. For better illustration, the results were averaged over every 10 measurements, so each data point represents the average behavior over an 840-second interval. The observed trends are consistent with the direct observations from Fig. 13 and Fig. 14. Specifically, the gain decreases by approximately 2 dB over the 40,000-second test period but shows a tendency toward stabilization. In contrast, the offset changes more rapidly during the initial 100 minutes, increasing from 4.3 mV to around 5.8 mV, after which it remains relatively stable. The observed gain and offset drift can be attributed to bias-stress effects in LTPS TFTs, including electron trapping, interface trap states, and grain boundary trap states, which lead to threshold voltage shift and mobility degradation [33].

D. TEMPERATURE MEASUREMENTS

As readout circuits are integrated with temperature sensors operating across wide thermal ranges, maintaining circuit stability becomes a critical design requirement. In particular, the gain and offset of the OpAmp should remain consistent under temperature variations to ensure accurate amplification.

The measured variations of gain and offset over temperature are illustrated in Fig. 16. For supply voltages of 6 V and 7 V, the average DC gain was approximately 60 dB with an average offset of around –20 mV. In contrast, when biased at 5 V, the circuit shows significantly larger gain variation and increased input offset.

TABLE 3. Comparison of state-of-the-art thin-film OpAmp designs.

	2019 [36]	2021 [37]	2023 [38]	2024 [39]*	2022 [40]	2020 [41]	2024 [42]*	2023 [34]	This work [22]
TFT Tech.	IGZO				IZO	LTPO	LTPS		
Topology	Positive-feedback	Pseudo-PMOS	Positive-feedback	Three-stage	Positive-feedback	Two-stage	Three-stage	Two-stage	**Two-stage**
Min Length (µm)	5	3	2	0.6	7	6	8	5	**5**
Supply (V)	15	10	6	3	20	± 20	10	12	**6**
Max Gain (dB)	43	57	42.2	52	50	50.7	58.8	64.1	**64.2**
GBP (kHz)	205	311	7,200	1,190	4,806	68,500	207	320	**400**
Phase Margin (°)	52	75	52	64	-24	92	83	80	**40**
Power(mW)	0.09	2.43	0.77	0.19	8.07	0.6	1.9	1	**0.6 (Max)**
Area(mm^2)	0.28	3.7	0.2	0.019	1	0.07	8.8	0.72	**1.38**
Gain Variation (dB)	-	-	± 2.7	-	-	-	-	± 3	**± 2.2**
Offset Variation (mV)	-	-	± 90	-	-	-	-	± 30	**± 19**
Temp. Range (°C)	-	-	-	-	-	-	-	0–80	**0–80**[a]
Stress Stability(s)	-	-	-	-	-	-	-	-	**40,000**[b]

* Simulated data

[a] Gain varies within 2 dB, offset within 6 mV across all temperatures (average across 20 samples).

[b] Gain stabilizes after 2.5 dB drop, offset after 1.5 mV rise during bias stress.

Although the average gain and offset at 6 V and 7 V remain thermally stable, which is consistent with prior folded-cascode LTPS designs [34], a significant spread is still observed across devices. This variation primarily stems from intrinsic LTPS non-uniformities and design limitations under low-voltage constraints, such as simplified current mirrors and cascoded stages. To meet the accuracy requirements, offset compensation techniques like auto-zeroing and chopping are recommended to mitigate input offset and 1/*f* noise in TFT-based OpAmps [35].

V. PERFORMANCE COMPARISON

Table 3 summarizes the state-of-the-art TFT operational amplifiers. Metal-oxide-based technology (IGZO and IZO) achieves the best technology scaling (0.6 μm), the lowest supply (3 V), and the smallest footprints (0.019 mm^2), yet their maximum open-loop gain are lower than 57 dB. LTPO OpAmp presents the highest gain-bandwidth-product (GBP) of 68 MHz and reaches 50.7 dB gain with 0.07 mm^2 area, but requires ± 20 V supply voltage for operation.

The proposed LV-FC OpAmp, fabricated in LTPS technology, achieves the highest reported DC gain of 64.2 dB at a 6-V supply, the lowest operating supply among reported LTPS designs, while occupying a chip area of 1.38 mm^2. Compared with a class-A output stage [34], the dynamically biased class-AB output stage reduces peak power consumption to 0.6 mW and improves output linearity and output swing by providing both sourcing and sinking currents. PVT robustness was confirmed across 20 measured samples. Under supply fluctuations, the design maintains operation down to 5 V, with an average gain of 57.6 dB, albeit with increased variation. At 6 V supply, it achieves an average gain of 60.03dB with $\sigma = 2.24$ dB, and an average input offset of -25.4 mV with $\sigma = 19$ mV. Over the 0–80 °C temperature range, the average gain changes by less than 2 dB, and the average offset shifts by under 6 mV. During a 40,000 s bias-stress test, the gain drifted by 2.5 dB, and the offset varied by 1.5 mV before stabilizing. These results demonstrate the LV-FC design's high performance, strong PVT tolerance, and excellent long-term reliability.

VI. CONCLUSION

In this work, we analyzed the temperature behavior of LTPS devices and proposed a monolithically integrated architecture for large-area temperature sensing. As part of this system, we designed and fabricated a low-voltage folded-cascode operational amplifier with a class-AB output stage using a flexible LTPS TFT process. Beyond conventional functional metrics, the amplifier was extensively characterized across 20 samples under DC, AC, temperature (0 °C to 80 °C), and long-term bias stress (up to 40,000 s). The results demonstrate that the amplifier maintains stable gain and offset over wide PVT and stress conditions. These results highlight the amplifier's strong robustness to PVT and aging effects, confirming its suitability for reliable, long-term operation in large-area, flexible sensing systems.

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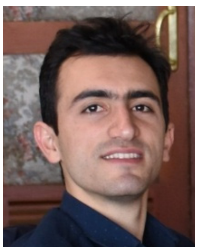
His current research interests include thin-film technology, analog and mixed-signal circuit design, and system-level development for biomedical applications, especially for neural interfaces.



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His research topic is to work towards smart energy devices, mainly focused on integration of sensors and read-out circuitry inside solar cells and batteries. His research activities are design and fabrication of thin film sensors, design of analog and digital circuits and test and measurement of devices made in thin-film technology.

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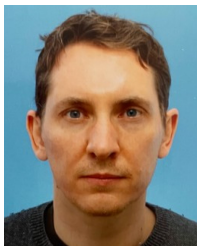
Then, he continued as an Analog, Mixed-Signal Researcher with imec, Leuven, in 2021. He is currently a Senior Researcher of Circuits and Systems for Health. He designed application specific integrated circuits for wearable/ingestible applications, such as electrocardiogram, bioimpedance, and photoplethysmography readouts. More recently, his research focused on the next-generation electrochemical, DNA sequencing, neural recording, and stimulation chips.



YANNICK BAINES was born in U.K., in 1982. He received the Ph.D. degree in condensed matter physics from Grenoble Alpes University in 2010. He spent the first half of his career working on III–V materials and devices, in particular quantum transport at cryogenic temperatures in AlGaAs/GaAs lateral quantum dots (2006–2010, Neel Institute, France), III–V epitaxial wafer growth and characterization for RF and power applications (2011-2013, Soitec, France), and GaN power diodes and transistors design for energy conversion (2013-2018, CEA-Leti, France). He later entered the field of Silicon sensing and imaging as a lead device engineer working on SPAD design for mobile and automotive Lidar (2019-2023, Sony, Japan), and is currently involved in imec Belgium in the design of pixels and specialty devices in a wide variety of fields, such as sensing, imaging or photonics.

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KRIS MYNY (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from KU Leuven, Leuven, Belgium, in 2013.

He is currently an Associate Professor with KU Leuven and a Guest Professor with imec. He specializes in circuit design for flexible thin-film transistor applications. His work has been published in numerous international journals and conferences, including *Nature*, *Nature Electronics*, and several ISSCC contributions. He was listed as one of the Belgium's top tech pioneers by the business newspaper De Tijd and received in 2018 the European Young Researcher Award for design on thin-film electronics. He was a recipient of two prestigious ERC Grants from the European Commission: An ERC Starting Grant from 2017 to 2021 enabling breakthrough research in thin-film transistor circuits and an ERC Consolidator Grant from 2023 to 2028 on the development of a universal interposer layer on top of Si CMOS (ORISON). He served as a member of the Young Academy of Belgium from 2019 to 2024. He also served as the Track Chair for the IEEE FLEPs Conference and acts in the editorial board of the IEEE JOURNAL ON FLEXIBLE ELECTRONICS and is a Guest Editor of *npj Flexible Electronics* (Nature Portfolio).