The design of non-stacked and symmetric XOR for high-speed applications

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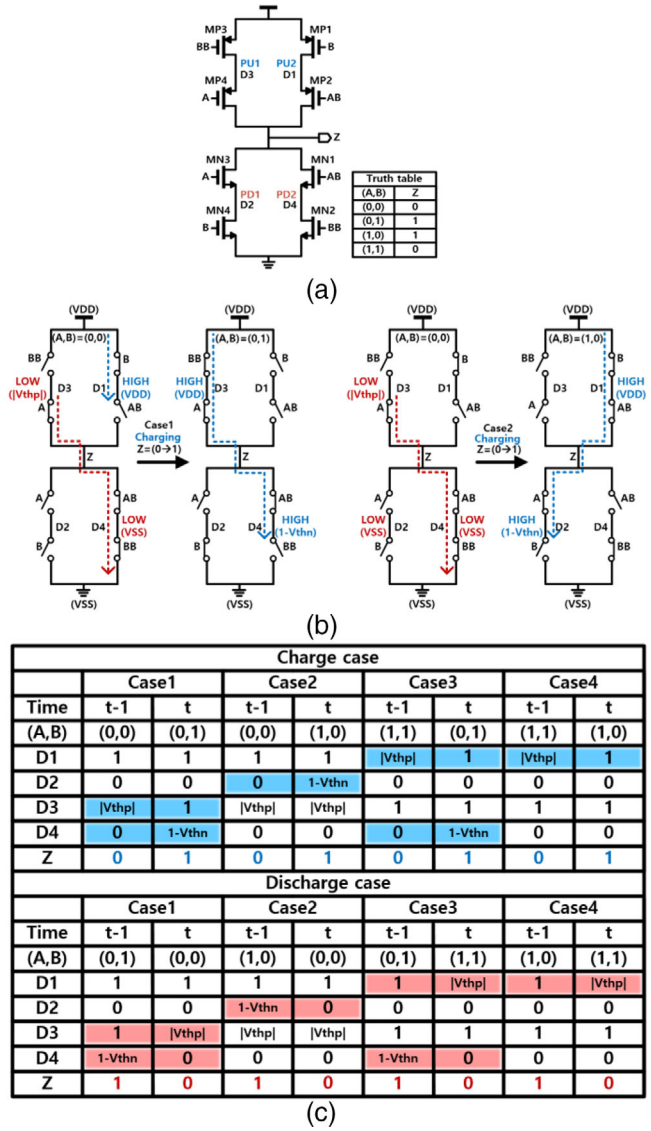
The paper proposes an advanced exclusive-OR (XOR) design using a non-stacked symmetric structure based on complementary pass transistor logic (CPL) for high-speed applications. The proposed XOR adopts a non-stacked structure where a cascade structure is used for pull-up/down paths instead of a cascoded structure, allowing the increase of pull-up/down strength and thus faster output transitions. The CPL provides a symmetric scheme that further improves the bandwidth by eliminating the deterministic jitter generated from various input patterns. Verified in a 28-nm CMOS process, the proposed XOR shows 17.2 times smaller data-dependent jitter compared to the conventional XOR at the data rate near the limit bandwidth of the process.

Introduction: As an element circuit, the XOR unit is used in various applications such as arithmetic operations, comparators, compressors, and parity checkers [1]. In high-speed applications, it is commonly used in clocking circuits such as phase detectors (PD) [2]. Some research groups have reported various XOR circuits based on pass transistor logic (PTL) [3–6]. In general, the single PTL-based logic gate operates with a non-full voltage swing at the output node [6], achieving significantly low power consumption but at the cost of driving capability. This leads to a limit on the bandwidth. To achieve high-frequency operation, other PTL-based XOR circuits have been reported. XOR structures in [3, 4] employ a feedback transistor to improve driving capability, and an XOR circuit in [5] adopts a power-less structure with a keeper transistor to improve power efficiency. However, the reported XOR circuits generate deterministic jitter depending on various input patterns, limiting bandwidth.

This paper proposes a high-speed XOR unit with fast transition and minimized data-dependent jitter. A non-stacked or cascaded structure [7] is used to improve the driving capability because this structure basically operates based on the static CMOS inverter. To eliminate the dependency on input data patterns, the proposed XOR adopts symmetric complementary pass transistor logic (CPL).

Architecture of conventional XOR unit: As shown in Figure 1a, the conventional XOR, XOR1, is composed of four stacked pull-up/down paths, PU1, PU2, PD1, and PD2, and receives A, B, and their complementary values. The four paths match four input patterns one-on-one, and only one of the four paths is turned on, charging or discharging the output Z. For example, when A and BB are Low, PU1 is turned-on and charges Z. Though the XOR1 is widely used in a variety of applications, it exhibits two disadvantages in terms of high-frequency operation. First, the stacked or cascoded pull-up/down path slows down transition time. As a solution, a cascaded structure can be used. Second, data-dependent jitter (DDJ) limits the high-frequency operation. The DDJ is generated due to an unexpected node that can be seen from the output when another output-neighbouring transistor is turned on during the transition. For better understanding, Figure 1b introduces two of four possible cases of LOW-to-HIGH output transition. The two cases can be expressed in the form of (A, B): Case1) (0,0) → (0,1), Case2) (0,0) → (1,0) where (A, B) means the logic values of A and B. Assume that D2 is initially discharged in both cases. Besides, D3 is not fully pre-discharged and



Charge case

	Case1		Case2		Case3		Case4	
Time	t-1	t	t-1	t	t-1	t	t-1	t
(A,B)	(0,0)	(0,1)	(0,0)	(1,0)	(1,1)	(0,1)	(1,1)	(1,0)
D1	1	1	1	1	|Vthp|	1	|Vthp|	1
D2	0	0	0	1-Vthn	0	0	0	0
D3	|Vthp|	1	|Vthp|	|Vthp|	1	1	1	1
D4	0	1-Vthn	0	0	0	1-Vthn	0	0
Z	0	1	0	1	0	1	0	1

Discharge case

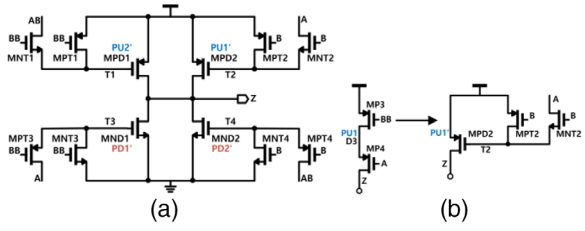
	Case1		Case2		Case3		Case4	
Time	t-1	t	t-1	t	t-1	t	t-1	t
(A,B)	(0,1)	(0,0)	(1,0)	(0,0)	(0,1)	(1,1)	(1,0)	(1,1)
D1	1	1	1	1	1	|Vthp|	1	|Vthp|
D2	0	0	1-Vthn	0	0	0	0	0
D3	1	|Vthp|	|Vthp|	|Vthp|	1	1	1	1
D4	1-Vthn	0	0	0	1-Vthn	0	0	0
Z	1	0	1	0	1	0	1	0

(c)

Fig. 1 *Conventional XOR unit. (a) Architecture of conventional XOR unit. (b) Pre-charged or pre-discharged status of internal nodes. (c) State table according to all transition patterns.*

has the value of $|V_{thp}|$ due to the PFET's characteristic, but this paper considers this pre-discharged value as LOW for convenience. In Case1, when (A, B) becomes (0,1), PU1 is activated, charging D3, Z, and D4. On the other hand, in Case2, when (A, B) becomes (1,0), PU2 is activated and charging only D2 and Z. These two different charging cases show different amounts of capacitance to be charged, resulting in different rising edges. Including the other two possible charging cases, the details of four charging cases are summarized in the table in Figure 1c. For each case, the internal nodes that are charged/discharged are indicated by blue and red backgrounds, respectively. Likewise, four possible discharging cases exist, generating different falling edges. The details of the discharging cases are also summarized in Figure 1c.

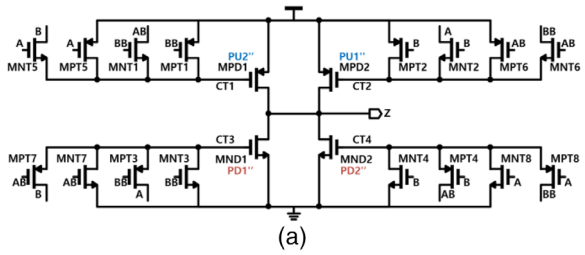
Architecture of proposed XOR unit: As shown in Figure 2a, the proposed XOR, XOR2, adopts a non-stacked structure [7] for bandwidth extension. Unlike XOR1 which is composed of a cascoded pull-up/down path, the configuration of cascaded structure is applied to XOR2 improving output transition speed. Figure 2b shows how the stacked pull-up path PU1 is converted to the cascaded structure of PU1' with pass transistors (TRs). When (A, B) = (0,1), a pass TR, MNT2, is turned on and discharges T2, thereby enabling MPD2 to charge the output. Another pull-up/down paths, PU2', PD1', and PD2', are generated in the same manner. Like XOR1, only one of four pull-up/down paths is turned on by the input patterns, determining the output value. In this structure, the initial state of T1 and T2 can be different according to input patterns.



	Charge case				Discharge case			
	Case1		Case2		Case1		Case2	
Time	t-1	t	t-1	t	t-1	t	t-1	t
(A,B)	(0,0)	(0,1)	(0,0)	(1,0)	(0,1)	(0,0)	(1,0)	(0,0)
T1	1-Vthn	1	1-Vthn	0	1	1-Vthn	0	1-Vthn
T2	1	0	1	1	0	1	1	1
T3	0	|Vthp|	0	0	|Vthp|	0	0	0
T4	1	0	1	|Vthp|	0	1	|Vthp|	1
Z	0	1	0	1	1	0	1	0

(c)

Fig. 2 *Improved XOR unit. (a) Architecture of non-stacked XOR unit. (b) Concept of non-stacked structure. (c) State table according to all transition patterns.*



	Charge case				Discharge case			
	Case1		Case2		Case1		Case2	
Time	t-1	t	t-1	t	t-1	t	t-1	t
(A,B)	(0,0)	(0,1)	(0,0)	(1,0)	(0,1)	(0,0)	(1,0)	(0,0)
CT1	1	1	1	0	1	1	0	1
CT2	1	0	1	1	0	1	1	1
CT3	0	0	0	0	0	0	0	0
CT4	1	0	1	0	0	1	0	1
Z	0	1	0	1	1	0	1	0

(b)

Fig. 3 *Proposed XOR unit. (a) Architecture of non-stacked symmetric XOR unit. (b) State table according to all transition patterns.*

Since T1 and T2 directly control the pull-up devices, MPD1, and MPD2, the different initial value leads to different charging timing. For example, two charging cases, Case1 and Case3, represent different initial values of T2. Likewise, the other two possible charging cases also generate different rising edges, and four possible discharging cases generate different falling edges. To minimize the input pattern dependency, the symmetric configuration is applied to XOR2, generating a new topology of XOR3, as shown in Figure 3a. The PTLs of each pull-up/down unit are duplicated for symmetrical usage and strongly hold the gate voltage of pull-up/down TRs for every case. Note that the size of each CPL is halved to maintain the same size as others. Figure 3b summarizes the charging/discharging cases and shows that initial values of internal nodes are completely symmetric. As a result, the input dependency is removed.

Simulation results and comparison: To validate the proposed XOR design, we compared the performance of four different XOR units in terms of transition time and jitter. These four XOR units were simulated under identical input/output conditions such as a load and an input buffer. Figure 4 shows eye diagrams of XOR outputs obtained from post-layout simulations. PRBS-7 and PRBS-13 are used as inputs. Note that 28-nm CMOS technology is used, and the sum of every transistor's finger number is the same for every XOR. Unlike the previous structure, where the output transition is highly dependent on the input data pattern, which limits logic bandwidth even with process scale down, the proposed structure exhibits minimal data-dependent jitter (DDJ) allowing the logic bandwidth to increase proportionally as the process scales down. In addition, the average transition time is more than twice that of the proposed structure. More performance metrics are compared with additional XOR circuits and summarized in Table 1 including power, delay, and a proposed FOM including jitter. Compared with the previous XOR [3–5], the proposed XOR shows better FOM of at least 17.2 times to up to 88.9 times.

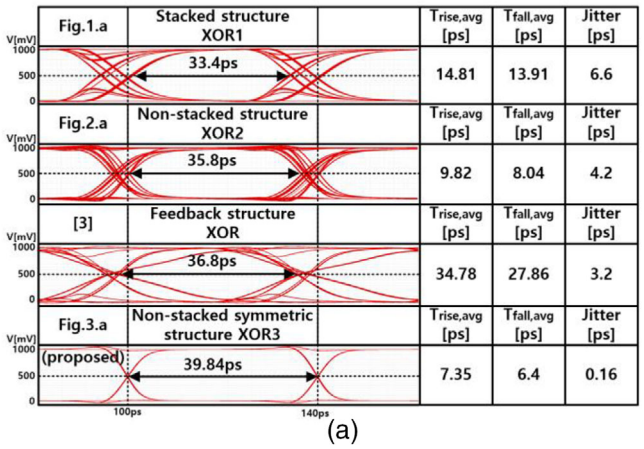


Fig. 4 *Eye diagram. (a) Simulation result of XOR unit (@ 25Gbps).*

Table 1. Performance summary of XOR units (@ 25Gbps).

XORs	Jitter (ps)	Power[a] (μW)	Delay (ps)	FOM[b] (10^{15} / J·s)
[3]	3.2	353.0	10.2	8.679
[4]	19.1	269.5	11.57	1.679
[5]	11.6	294.6	7.4	3.954
Non-stacked	4.2	265.3	12.3	7.296
Proposed (non-stacked symmetric)	0.16	367.4	11.4	149.221

Note:[a]Power = buffer + XOR unit
[b]FOM = 1 / (jitter × power × delay)

Conclusion: A symmetric and non-stacked XOR design is proposed for high-speed applications. The usage of CPLs allows the non-stacked structure, enabling fast transitions at the output. The symmetric configuration of CPLs eliminates the input dependency, increasing the bandwidth further. As a result, the proposed design shows better performance than the previous design in terms of jitter, power, and delay.

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Data availability statement: Data is openly available in a public repository that issues datasets with DOIs.

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