60-dB 70-V/μs Three-Stage Op-Amp With Dual Single-Miller Frequency Compensation in GaN-IC Technology

Katia Samperi, *Graduate Student Member, IEEE*, Urmimala Chatterjee, and Salvatore Pennisi, *Fellow, IEEE*

***Abstract*— Modern high-performance electronics is pushing Si technology to its limits. Gallium Nitride (GaN) emerges as a promising alternative due to its superior properties in high-frequency and high-power applications. To fully utilize the fast-switching ability of the GaN technology, monolithic integration is a key. A monolithically integrated GaN power IC (Integrated Circuit) reduces the inductive parasitic enabling a fast efficient switching operation. However, GaN basic building blocks, particularly operational amplifiers (Op-Amps), face severe challenges due to the limitations of the GaN technology. This paper presents the first three-stage Op-Amp for high-performance feedback circuits realized in the IMEC's 200-V GaN-IC technology on a GaN-on-SOI (Silicon on Insulator) substrate. The design utilizes a cascade of three differential stages resistively loaded to achieve a nearly 60-dB DC gain and 25-MHz gain-bandwidth and implements a novel dual single-Miller frequency compensation technique to provide closed-loop stability. The Op-Amp offers a Slew Rate exceeding 70 V/μs with 1% settling time of about 120 ns at room temperature. The correct circuit functionality from −40 °C to 150 °C was demonstrated through simulations and experimental test.**

***Index Terms*— Gallium Nitride, amplifiers, analog IC design, frequency compensation.**

I. Introduction

MODERN electronic systems demand ever-increasing performance in terms of bandwidth, efficiency, and power density. This trend puts significant pressure on traditional silicon (Si) technology, particularly for applications requiring high-frequency and high-power operation with high efficiency. Gallium Nitride (GaN) has emerged as a promising alternative technology for these demanding applications due to its superior properties [1], [2]. Indeed, compared to Si, GaN boasts several advantages that make it ideal for high-performance power electronics and radio frequency (RF) applications such as: a) wider bandgap that enables higher breakdown voltage and operation at high temperatures, b) higher electron mobility that leads to improved transconductance and faster switching speeds, and c) higher saturation velocity that enables efficient operation at high frequencies [3], [4], [5], [6].

However, the development of GaN integrated circuits (ICs) presents several challenges, especially when it comes to designing mixed-signal and pure analog blocks such as operational amplifiers (Op-Amps), the workhorses of analog design. One of the significant drawbacks is the absence of p-channel devices in GaN technology. Unlike Si IC technology, where complementary metal-oxide-semiconductor (CMOS) transistors allow for both n-channel and p-channel devices, GaN IC technology currently only supports n-channel transistors and passives like resistors and capacitors. This limitation complicates the design of Op-Amps [7], [8], [9], [10], [11], which CMOS implementations typically rely on complementary pairs of transistors to achieve high gain, linearity, and power efficiency [12], [13], [14].

IMEC has developed GaN-based integrated circuits on a SOI (Silicon-on-Insulator) substrate with deep trench isolation and buried oxide to fully isolate the HEMT and its logic circuitry that are cut-off by a trench. By using this trench isolation, it is possible to have a local contact with the source of a device to the top thin silicon layer of the SOI substrate, wherever a galvanic isolation is required [15]. The process employed in this work, namely a 200-V GaN-on-SOI GaN-IC technology by IMEC, features also 20-V E-mode n-channel devices with intrinsic gain and transition frequency of 40 dB and 1 GHz, respectively, MIM capacitors and 2DEG resistors as low voltage components, [16]. Therefore, the main building block for the digital/analog designer in this technology becomes an RTL (Resistor-Transistor-Logic) based inverter [17]. The absence of D-mode (depletion) devices, which can serve as both bias elements and active loads, significantly constrains design flexibility and necessitates trade-offs in DC gain, *CMRR*, *PSRR*, power consumption, and circuit complexity. Despite these challenges, advancements in GaN technology and integrated-circuit design continue to push the boundaries of what is possible [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28]. As research and development progress, it is expected that new device structures and fabrication techniques will further mitigate the limitations of

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Katia Samperi and Salvatore Pennisi are with the Dipartimento di Ingegneria Elettrica Elettronica ed Informatica (DIEEI), Università di Catania, 95125 Catania, Italy (e-mail: katia.samperi@phd.unict.it; salvatore.pennisi@unict.it).

Urmimala Chatterjee is with IMEC, 3001 Leuven, Belgium (e-mail: urmimala.chatterjee@imec.be).

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RTL based designs, paving the way for more robust and versatile GaN-based ICs.

Starting from the IMEC GaN-on-SOI process, this paper proposes the design and experimental characterization of a three-stage Op-Amp suitable for low-power, high-bandwidth, high-speed feedback circuits targeting low-capacitive loads in on-chip applications. For example, it can be used as an error amplifier in a half-bridge integrated driver paired with a GaN power transistor. The proposed solution utilizes a straightforward cascade of three differential stages to achieve the targeted DC gain of 60 dB and gain-bandwidth product (*GBW*) greater than 10 MHz. This modular topology provides inherently robustness against process variations. The choice of three stages stems from the fact that single-stage differential amplifiers with resistive loads and currents respectively in the range of some tens kiloohms and some hundred microamperes typically offer a maximum DC gain of around 20 dB.

However, three-stage amplifiers pose significant challenges for frequency compensation due to the difficulty of maintaining high gain-bandwidth product while ensuring stability. Miller compensation in this case is essential to attain stability with limited capacitance, but traditional techniques for multistage Op-Amps, like nested and reversed nested Miller compensation [29], [30], [31], [32], [33], [34], [35], [36], are not suitable for low-capacitive loads when bandwidth must be optimized. Indeed, in multistage amplifiers with substantial capacitive loads, the output pole is often located at low frequencies, close to the dominant pole at the first stage's output. Traditional nested and reversed-nested Miller compensation techniques for such amplifiers require two (large) capacitors. In contrast, the single Miller capacitor approach was introduced in [37] to reduce area and enhance both small-signal and large-signal performance. Following works extended the approach also to large load capacitances [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50]. As a result, a custom compensation approach is here required to preserve speed performance. At this purpose, our solution employs a single Miller capacitor for each of the two differential paths. This configuration offers excellent performance metrics, including a slew rate exceeding 70 V/μs with a 1% settling time around 120 ns.

The subsequent part of this paper is organized as follows. Section II details the Op-Amp's topology and outlines the key design equations. Section III elaborates on the specific frequency compensation approach and presents the associated design equations in detail. Section IV validates the design through extensive simulation results and experimental characterization. Finally, the paper ends with the authors' key findings and a discussion of future work directions.

II. The Proposed Three-Stage GaN Amplifier

One of the first Op-Amps in GaN technology was presented by two of the authors in [9]. However, the solution utilized E-mode and D-mode transistors, and it was tailored for off-chip loads (i.e. up to 1 nF load capacitors), whereas the solution proposed here exploits a technology providing only E-mode devices and is intended for on-chip loads. Moreover, given the significant parameter variations inherent to this technology, matching is a critical concern. We therefore opted for the simplest design approach to mitigate the impact of mismatches, as more complex structures like folded-cascode topologies may be even more susceptible to these variations.

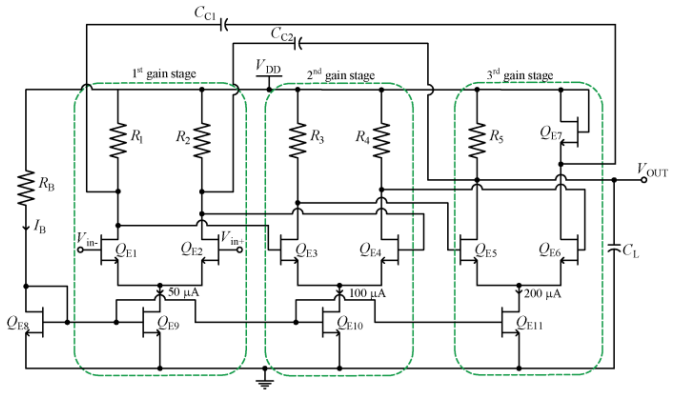

Fig. 1. Schematic of the three-stage GaN Op-Amp with the frequency compensation network and the bias branch.

The target DC gain and gain-bandwidth are 60 dB and >10 MHz, respectively.

A. Topology

The simplified schematic of the proposed operational amplifier in GaN-IC technology is depicted in Fig. 1. It is made up of the simple cascade of three differential stages (source-coupled stages) with resistive loads. The first stage is made up of transistors Q_{E1}-Q_{E2}, resistors R_1-R_2 and tail current generator Q_{E9}. The two outputs of this first stage drive the gates of the second stage, made up of transistors Q_{E3}-Q_{E4}, resistors R_3-R_4 and tail current generator Q_{E10}. The two outputs of this second stage drive in turn the gates of the third stage, made up of transistors Q_{E5}-Q_{E6}, resistor R_5, at the Op-Amp output, diode-connected transistor Q_{E7}, as an active load at the auxiliary output, and tail current generator Q_{E11}. The reason of different loads in the output stage will be clearer in the next section. Diode-connected transistor Q_{E8} through resistor R_B sets the current in this reference branch to be mirrored in the tail generators. Capacitor C_L is the equivalent load, while frequency compensation is accomplished through Miller capacitors C_{C1} and C_{C2}. As said, this technique utilizes only one single Miller capacitor in each differential path.

B. Design

Given the supply voltage of 6 V, to ensure a good enough over-drive voltage for the pairs against process mismatches, we set the nominal common-mode input voltages of all the pairs to 3 V. This requires that the voltage drop across the load resistors R_1-R_5 must be equal to 3 V. Moreover, the tail currents of the pairs were designed to progressively double moving from the left to the right (50 μA, 100 μA and 200 μA), to provide increased driving capability, slew rate, and low output resistance at the Op-Amp output terminal.

This means that the resistors of the first, second and third pair must be equal to $R_{1,2} = 120$ kΩ, $R_{3,4} = 60$ kΩ, and $R_5 = 30$ kΩ, respectively. The equivalent small-signal resistance value of $1/g_{m7}$ at the drain of Q_{E6} is selected in the next section as required by the frequency compensation approach.

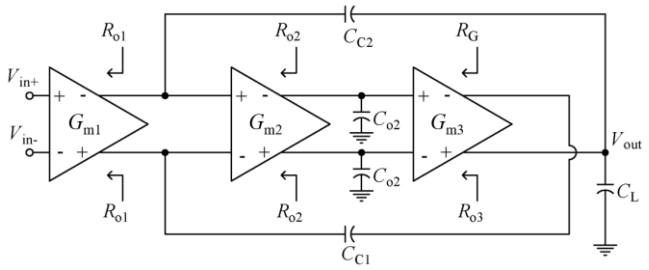

Fig. 2. Equivalent small-signal model of the proposed Op-Amp.

Finally, the stages' transconductances, g_{mi}, were chosen to provide an overall single-ended voltage gain of 60 dB equally distributed for each stage. To compensate for the 6-dB loss due to the single ended output, $g_{mi}R_i$ for $i = 1$ to 3 was set equal to 12.6. Therefore, the transconductances must be equal to $g_{m1,2} = 105\ \mu$A/V, $g_{m3,4} = 210\ \mu$A/V, and $g_{m5,6} = 420\ \mu$A/V.

III. Small Signal Model and Frequency Compensation

The Op-Amp small-signal model utilized to derive the loop gain transfer function is given in Fig. 2. The transconductance and the resistances at the inverting and noninverting output terminals of the first two stages are respectively G_{m1}, G_{m2} and R_{o1}, R_{o2}. For the third stage the transconductance is G_{m3} and the output resistances are R_{o3} (noninverting output) and R_G (inverting output). Of course, with reference to Fig. 1, we have: $G_{m1} = g_{m1,2}$, $G_{m2} = g_{m3,4}$, and $G_{m3} = g_{m5,6}$, where g_{mi} is the transconductance of transistor Q_{Ei}. Moreover, $R_{o1} = R_{1,2}$, $R_{o2} = R_{3,4}$, $R_{o3} = R_5$, and $R_G = 1/g_{m7}$. Furthermore, to account for the non-ideal behavior of the circuit, we incorporated parasitic capacitances (C_{o2}) at the outputs of the second stage. These capacitances, not explicitly shown in Fig. 1 like instead the compensation capacitors (C_{C1}, C_{C2}), and the load capacitance (C_L), are crucial to represent the realistic impact of stray capacitances on the circuit's performance.

To evaluate the transfer function of the Op-Amp we adopted the symbolic calculation tool and transfer function simplification method described in [51]. Symbolic analysis shows that the simplified loop gain transfer function includes four negative poles and two negative zeros. Hence, the loop gain is expressed with good approximation as

$$A(s) \approx A_0 \frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)\left(1+\frac{s}{p_4}\right)} \tag{1}$$

where

$$A_0 = \frac{1}{2} G_{m1} R_{o1} G_{m2} R_{o2} G_{m3} R_{o3} \tag{2}$$

$$p_1 \approx \frac{2}{R_{o1} G_{m2} R_{o2} G_{m3} \left(R_{o3} C_{C2} + \frac{1}{2} R_G C_{C1}\right)} \tag{3}$$

$$p_2 \approx \frac{2R_{o3}C_{C2} + R_G C_{C1}}{C_{C2}[2R_{o1}(R_{o3}+R_G)C_{C1} + R_{o2}R_{o3}C_{o2}]} \approx \frac{1}{R_{o1}C_{C1}} \tag{4}$$

$$p_3 \approx \frac{1}{(R_{o3} \,\|\, R_G)\, C_L + R_{o2}C_{o2}} \tag{5}$$

$$p_4 \approx \frac{R_{o2}(R_{o3}+R_G)C_{o2} + R_{o3}R_G C_L}{R_{o2}R_{o3}R_G C_{o2} C_L} = \frac{1}{(R_{o3} \,\|\, R_G)\, C_L} + \frac{1}{R_{o2}C_{o2}} \tag{6}$$

$$z_1 \approx \frac{1}{R_{o1}(C_{C1}+C_{C2})} \tag{7}$$

$$z_2 \approx \frac{1}{R_{o2}C_{o2}} \tag{8}$$

Moreover, the model predicts two high frequency real zeros (one positive and one negative) very close each other. The expression of the positive zero is

$$z_3 \approx -\frac{1}{4} \frac{G_{m2}R_{o2}G_{m3}}{\frac{C_{C1}C_{C2}}{C_{C1}+C_{C2}}} \tag{9}$$

which is at a frequency much greater than p_4. For this reason, these two zeros are neglected. There is another higher frequency pole that is also neglected.

The *GBW* (expressed in rad/s, as also the poles and zeros in (3)-(9)) is hence given by

$$GBW = A_0 p_1 \approx \frac{G_{m1}}{C_{C2} + \frac{1}{2}\frac{R_G}{R_{o3}} C_{C1}} \tag{10}$$

As can be seen, the dominant pole (3) is the result of the joint Miller effect on C_{C2} and C_{C1}. However, the contribution of C_{C1} is reduced by factor $0.5R_G/R_{o3}$. Besides, the compensation approach performs two pole-zero cancellations. The first occurs between p_2 and z_1. By comparing (4) and (7), it becomes evident that a pole-zero cancellation ($z_1 \approx p_2$) is achievable when C_{C1} significantly exceeds C_{C2}. However, to maintain circuit symmetry and matching, we opted for $C_{C1} = C_{C2}$. In this configuration, we obtain $p_2 \approx 2\ z_1$, which still adequately cancels the second pole.

A second pole-zero cancellation arises between p_3 and z_2. This cancellation can be made highly precise and robust against process variations by ensuring

$$(R_{o3} || R_G) C_L \ll R_{o2} C_{C2} \tag{11}$$

By setting C_L equal to C_{C2} and noting that R_{o2} is twice R_{o3}, condition (11) is satisfied when $R_G < R_{o3}$.

In our design, we hence set $R_G = 1/g_{m7} = 10$ kΩ (*i.e.*, 1/3 of R_{o3}) and $C_L = C_{C1} = C_{C2} = 400$ fF. C_{o2} was also esteemed as around 100 fF. With this settings $z_2 \approx 1.5\ p_3$ is achieved, again offering a good pole-zero cancellation.

In summary, as a result of the double pole-zero cancellation, the Op-Amp is reduced to a two-pole system with the dominant pole given by (3) and the equivalent second pole given by (6). This allows for precise control of the *GBW* (via C_{C1} and C_{C2}) to meet an adequate phase margin, *PM*, given by

$$PM \approx 90^\circ - \tan^{-1}\frac{GBW}{p_4} = 90^\circ - \tan^{-1}\frac{G_{m1}/C_{C2}}{\frac{1}{(R_{o3}\|R_G)C_L} + \frac{1}{R_{o2}C_{o2}}} \tag{12}$$

TABLE I
COMPONENTS' PARAMETERS

	W/L [µm/µm]		Value
Q_{E1-2}	12/1.3	R_B	36 kΩ
Q_{E3-4}	24/1.3	R_{1-2}	120 kΩ
Q_{E5-6}	48/1.3	R_{3-4}	60 kΩ
Q_{E7-9}	12/1.3	R_5	30 kΩ
Q_{E8}	6/1.3	C_{C1-2}	400 fF
Q_{E10}	24/1.3	C_L	400 fF

Finally, by substituting the component values in (2)-(10) and (12) we get the following numerical values: $A_0 = 1000$, $p_1 = 35.8$ kHz, $p_2 = 2.7$ MHz, $p_3 = 17.7$ MHz, $p_4 = 79.6$ MHz, $z_1 = 2.2$ MHz, and $z_2 = 26.5$ MHz, (with the positive zero $z_3 = 228$ MHz). The *GBW* is 35.8 MHz and *PM* is 65.8°.

IV. VALIDATION RESULTS

The proposed Op-Amp was designed using the IMEC's 200-V GaN-IC technology [19], accessed through Europractice. This processing is done in IMEC's 200-mm pilot line by using an Au free process flow. The power device fabrication starts with the patterning of the TiN/p-GaN stack to form the gate [17]. To form the drain and source of the device, an ohmic contact with the different metal field plates are processed. The fields plates are designed such a way that the electric field peaks can be redistributed. The process concludes with a Si3N4 passivation. To eliminate the backgating effect and crosstalk between the different parts of the circuitry, an oxide filled deep trench isolation (DTI) in combination with the buried oxide is implemented.

Table I summarizes transistors dimension and passive components value. Supply voltage is 6 V and nominal current consumption is 350 μA. To minimize the impact of process variations, a highly symmetrical layout style with guard rings and suitable dummy elements was adopted. The layout is shown in Fig. 3, which also depicts the die micrograph. The total chip area is approximately 170 μm × 210 μm.

A. Simulations

The simulated frequency response of the OTA's loop gain (magnitude and phase) is shown in Fig. 4. The DC gain is 58.6 dB, the dominant pole is at around 37.6 kHz and the gain-bandwidth product is 32 MHz with a phase margin of approximately 60°. The very good pole-zero compensation is apparent as both the magnitude and phase plots behave like a single-pole function until the transition frequency.

Figure 5 presents the simulated magnitude of the common-mode rejection ratio (*CMRR*) and power supply rejection ratio (*PSRR*) versus frequency. The DC values are 85 dB and 62 dB, respectively. The large value of *CMRR* simulated in ideal matching conditions is of course expected to be reduced by fabrication tolerances. Unfortunately, no Montecarlo models are available in the design kit and therefore no statistical simulations can be conducted. As a worst-case scenario, considering a 5% mismatch in the resistors yields the dashed curve in the same Fig. 5. *CMRR* at DC is 71 dB.

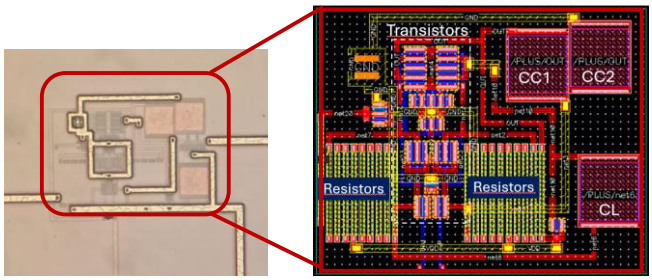

Fig. 3. Die photo and layout of the proposed OTA. Area is 170 μm × 210 μm.

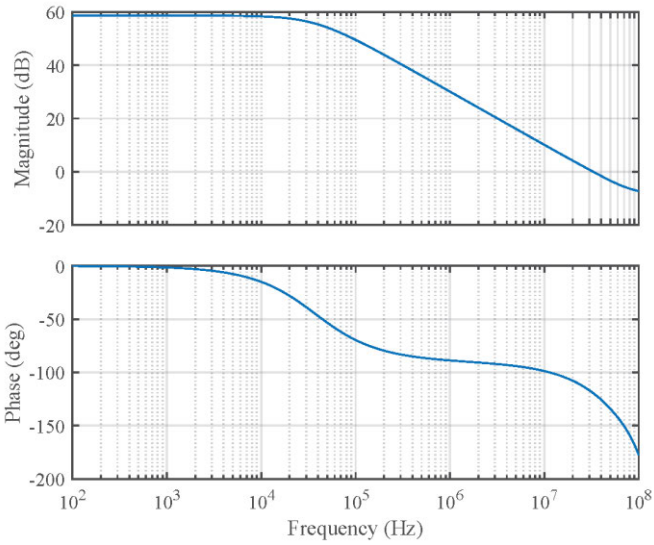

Fig. 4. Simulated Bode plots of the loop gain ($C_L = 400$ fF).

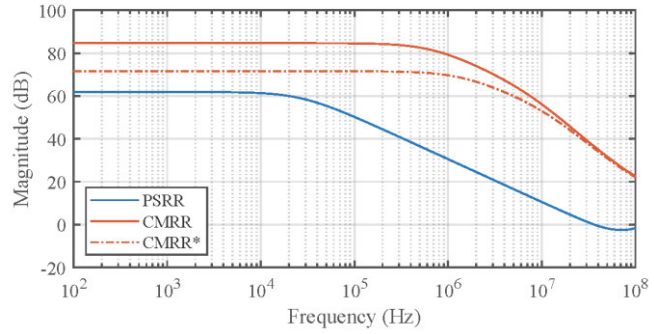

Fig. 5. Simulated magnitude of *CMRR, CMRR*∗(evaluated considering a 5% mismatch in the load resistors) and *PSRR* versus frequency.

Temperature plays a crucial role in the performance, reliability, and matching of integrated GaN transistors. As the temperature increases, important parameters such as threshold voltage, on-resistance, and current gain degrade. This happens because high temperatures reduce electron mobility in the GaN channel, leading to lower current handling capability and decreased efficiency.

GaN devices typically operate at higher power densities, which generates more heat. Effective thermal management is essential to prevent overheating, as excessive heat can cause performance degradation and reliability issues, including potential breakdown or failure of the device.

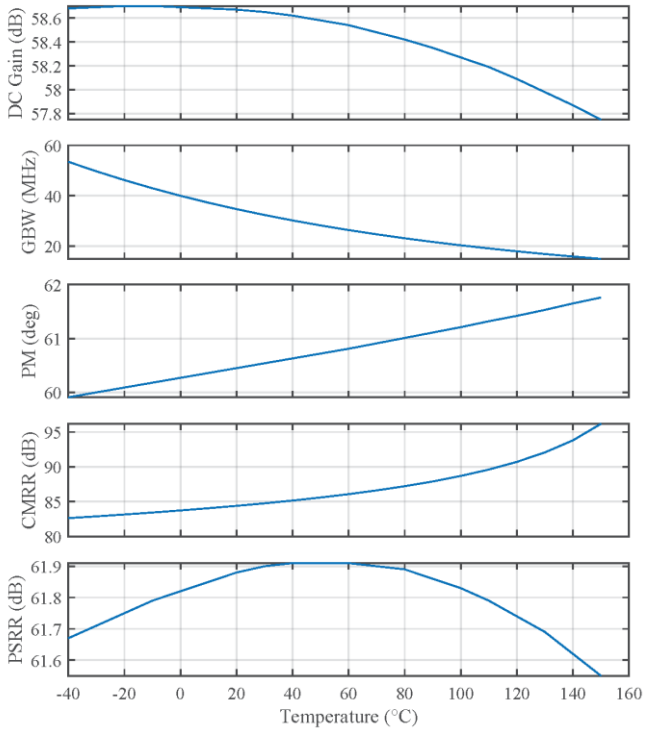

Fig. 6. Simulated DC gain, *GBW*, *PM*, *CMRR* and *PSRR* versus temperature.

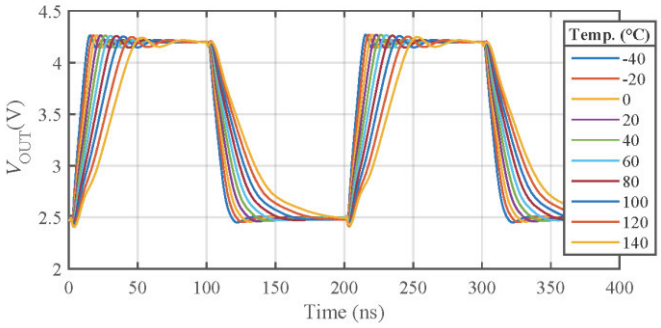

Fig. 7. Simulated time response of the OTA in unity gain to a 1.7-Vpp input step, for different temperatures.

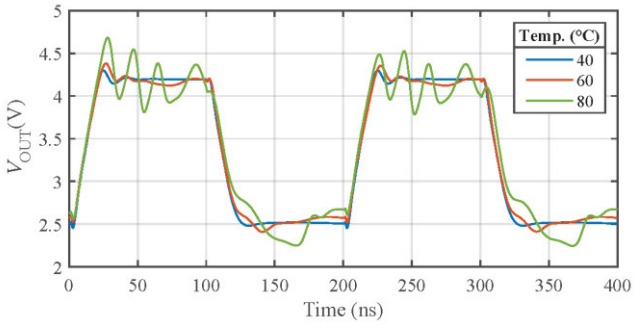

Fig. 8. Simulated time response of the OTA in unity gain to a 1.7-Vpp step, for three different temperatures. The current-setting resistor R_B in Fig. 1 is kept ideally constant with the temperature to emulate the effect of an off-chip component.

To evaluate the effects of the temperature on the above parameters, Fig. 6 illustrates the variation of DC gain, *GBW*, *PM*, *CMRR*, and *PSRR* across the industrial temperature range of −40 °C to 150 °C. The DC gain exhibits a variation of less than 1 dB, while *GBW* ranges from 57 MHz to 20 MHz. The phase margin remains at above 60° throughout the entire temperature sweep. This last result is another confirm of the accuracy of the double pole-zero cancelation technique. Finally, the DC magnitudes of *CMRR* and *PSRR* are consistently greater than 81 dB and 61 dB, respectively.

Equivalent input noise voltage spectral density (white noise) was found to be 5.3 nV/$\sqrt{\text{Hz}}$.

Fig. 7 depicts the time response of the Op-Amp in unity gain configuration to a 1.7-V_{p-p} input step at various temperatures in the whole range from −40 °C to 140 °C. Both the positive and negative slew rates (*SR*) at the room temperature are about 80 V/μs. These parameters degrade with increasing temperature. Notably, while the positive-going step settles within 100 ns at all temperatures, the negative-going step fails to reach steady-state starting from 140 °C. At this purpose, it must be emphasized the importance of an on-chip current-setting resistor (R_B in Fig. 1). To check the effect of using an external (off-chip) current-setting resistor, we assumed R_B as an ideal constant resistor independent of temperature.

Fig. 8 showcases the response to the same input step as in Fig. 7, at three different temperatures (40 °C, 60 °C, and 80 °C). While the response remains acceptable and settles within 50 ns at 40 °C, instability issues become evident at 60 °C and 80 °C. It is therefore confirmed that a tight temperature matching of the resistors used both for biasing and as a load of the differential pairs is mandatory to achieve a stable Op-Amp behavior versus temperature and process spreads.

B. Measurements

The proposed circuit was followed by a common drain transistor integrated in the same die, to avoid the effects of the off-chip testing equipment load. As a drawback, the common drain causes some artifacts in the time response.

Fig. 9 depicts the total measured current consumption of the Op-Amp, I_{OP_AMP}, and the reference current, I_{BIAS}, versus temperature. At 27 °C, for instance, I_{BIAS} is 100 μA and the total Op-Amp current is 295 μA slightly different from what expected (350 μA), due to the inaccurate mirroring action of Q_{E9}, Q_{E10} and Q_{E11} that worsens with temperature. The behavior of these currents shows that both decrease with the temperature although with different coefficients. Indeed, the ratio I_{OP-AMP} to I_{BIAS} is 2.65 at −40 °C, 2.95 at 25 °C, 3.5 at 80 °C, and 5.1 at 140 °C.

Offset at ambient temperature was found to be less than 1 mV in the available 5 samples.

The time response of the Op-Amp in unity gain to a 2-V_{p-p} input step is illustrated in Fig. 10. The positive and negative slew rate values are better than 70 V/μs. Settling time at 1% is around 120 ns.

Fig. 11 illustrates a detail of the same time response at various temperatures, from −40 °C to 150 °C. To enhance visual distinction between the curves, each curve is shifted vertically by 50 mV compared to the previous one. The curve

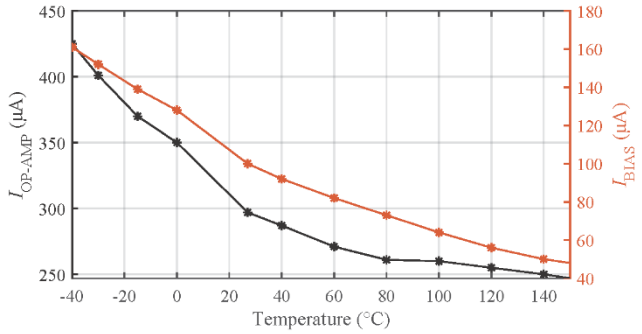

Fig. 9. Measured average current consumption of the Op-Amp, I_{OP-AMP}, and the corresponding bias current I_{BIAS} versus temperature.

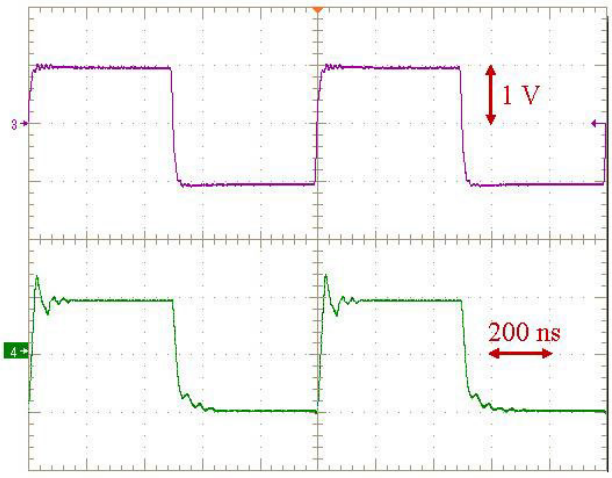

Fig. 10. Measured time response (lower trace) of the Op-Amp in unity gain to a 2-V_{p-p} input step (upper trace).

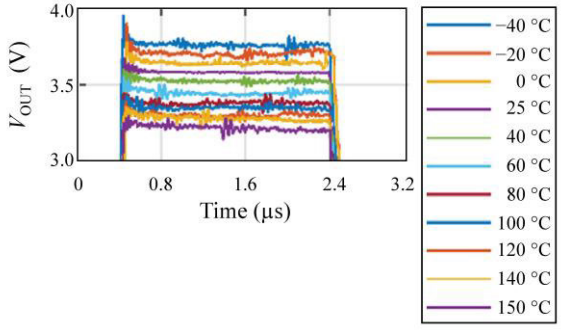

Fig. 11. Detail of the time response of the Op-Amp in unity gain to a 2-V_{p-p} input step for temperatures within -40 °C to 150 °C. The signals are vertically spaced 50 mV apart for better visibility.

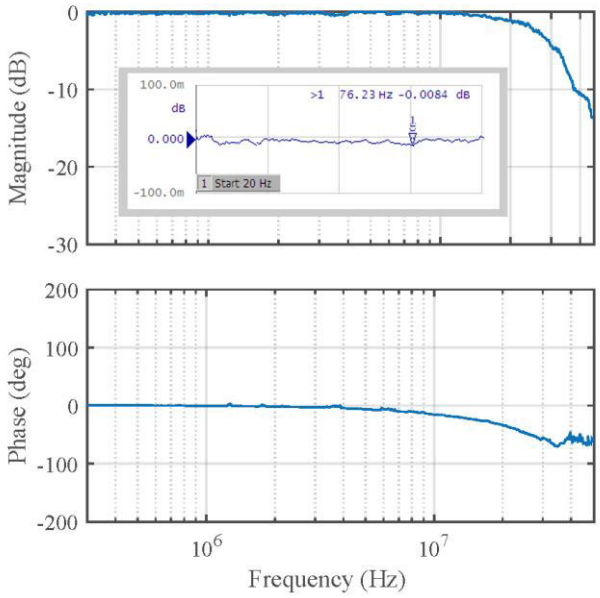

Fig. 12. Measured closed-loop gain (magnitude and phase) versus frequency. The −3 dB frequency is approximately 25 MHz The inset shows a DC gain of approximately −0.0084 dB under worst-case conditions.

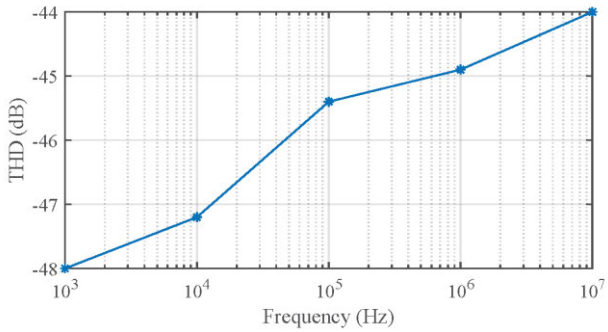

Fig. 13. Measured Total Harmonic Distortion, *THD*, versus frequency for input amplitude equal to 0.6 V.

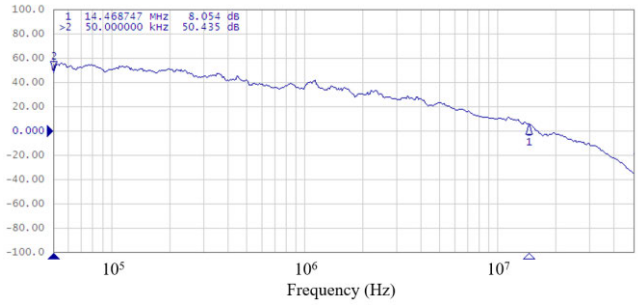

Fig. 14. Measured *PSRR* versus frequency.

representing the output at 25 °C remains unshifted. It is seen that stability is preserved in all cases.

The closed-loop gain magnitude of the Op-Amp in unity gain versus frequency is shown in Fig. 12. The −3 dB frequency is approximately 25 MHz, which gives an indirect measure of the *GBW* in agreement with the value expected. Additionally, the low-frequency gain, depicted in the inset of Fig. 12, is approximately −0.0084 dB, closely matching the predicted value deriving from 60 dB open-loop gain, using the formula $A_{CL} = A_{OL}/(1+A_{OL})$, where A_{CL} and A_{OL} are the DC closed-loop and open-loop gains, respectively.

Fig. 13 shows the measured Total Harmonic Distortion, *THD*, versus frequency for input amplitude again equal to 0.6 V.

Fig. 14 shows the measured *PSRR* versus frequency. At 50 kHz *PSRR* is 50 dB, in reasonable agreement with simulations.

TABLE II
SUMMARY OF OP-AMP PERFORMANCE (@27°C)

V_{DD}	6 V
Standby current	<300 µA
Area	170 µm × 210 µm
DC Gain *	60 dB
GBW	25 MHz
SR	70 V/µs
Settling time 1%	120 ns
THD @10MHz, 0.6-V amplitude	−44 dB
PSRR @50 kHz	50.4 dB
White noise**	5.3 nV/$\sqrt{\text{Hz}}$

*Extrapolated, **Simulation

Table II summarizes the main Op-Amp performance parameters.

V. CONCLUSION

This research paper tackles the difficulties associated with developing GaN-based Op-Amps, which are essential building blocks in analog electronic circuits. Specifically, the proposed circuit is implemented in a GaN-IC process, which presents limited freedom to the designer due to the development phase of the technology.

A novel three-stage Op-Amp design suited for on-chip high-speed ad high-bandwidth feedback circuits is proposed. This design utilizes a cascade of differential stages resistively loaded to achieve a sufficient DC gain (60 dB).

The paper also introduces a new dual single-Miller frequency compensation technique with double pole-zero cancellation to ensure closed-loop stability. Detailed design equations are also given to support this approach.

The designed Op-Amp demonstrates very good performance with a high slew rate exceeding 70 V/μs and a settling time of approximately 120 ns at room temperature with a gain-bandwidth product of 25 MHz, indicating its capability for handling fast signal changes.

Future work will focus on the development of a four-stage gain amplifier for higher DC gain and an output stage to enhance current drive capability.

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Katia Samperi (Graduate Student Member, IEEE) was born in Bronte, Catania, Italy, in 1998. She received the B.S. and M.S. degrees in electronic engineering from the University of Catania, Italy, in 2019 and 2021, respectively, where she is currently pursuing the Ph.D. degree. Her current research interests include wide-bandgap semiconductor, gallium nitride IC design for power applications, and power circuits for new photovoltaic technology.

Urmimala Chatterjee received the bachelor's degree in electronics engineering from West Bengal, India, the master's degree in IC design from NTU-TUM, Munich, Germany, in 2011, and the Ph.D. degree from the Department of Electrical Engineering (ESAT), KU Leuven, in 2016, with a focus on smart power converter design for photovoltaic application. She is currently with IMEC, Leuven, Belgium, working in GaN power electronics, mainly responsible for GaN IC activities and device design. Before joining IMEC, she worked few years in Thales, Belgium, on discrete circuit design for satellite and space applications.

Salvatore Pennisi (Fellow, IEEE) was born in Catania, Italy, in 1965. He received the Graduate degree in electronic engineering and the Ph.D. degree in electrical engineering from the University of Catania, Italy, in 1992 and 1997, respectively. In 2016, he was appointed as a Full Professor with the University of Catania, where he holds undergraduate and graduate courses in electronics and microelectronics. He has published more than 120 articles in international journals (64 of which in IEEE journals) and more than 140 contributions in conference proceedings. He is the co-author of the books *CMOS Current Amplifiers* (Kluwer Academic Publishers, 2001), *Feedback Amplifiers: Theory and Design* (Kluwer Academic Publishers, 2001), and *Liquid Crystal Display Drivers Techniques and Circuits* (Springer, 2009). His main research interests include circuit theory and analog design with an emphasis on low voltage techniques, multistage amplifiers, data converters, high-frequency distortion analysis, driver circuits for liquid crystal displays, and micro-energy harvesting. He is a member of the IEEE CASS Analog Signal Processing Technical Committee. He was an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS and of the *International Journal of Circuit Theory and Applications* (Wiley).

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