A 64-GHz Optical Receiver for 128-GBd Links Using a 55-nm SiGe BiCMOS Traveling-Wave Linear Transimpedance Amplifier

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***Abstract*—We present an optical receiver using a SiGe BiCMOS transimpedance amplifier (TIA) chip with a 3 dB bandwidth over 67 GHz and a transimpedance gain up to 77 dBΩ. This TIA consists of a single-ended input stage and two differential gain stages followed by a differential output stage. These traveling-wave stages feature variable gain and peaking. A TIA channel consumes 487.5 mW, or 2.2 pJ/bit operating at 112 GBd PAM-4, and occupies a chip area of 1.125 mm^2. The THD at 1 GHz (10 GHz) is kept below 2% (5%) for input swings up to 1.6 mApp (1.3 mApp) by reducing the gain. After wire bonding the input of this TIA to a silicon photonic germanium photodiode, a bandwidth of 64 GHz and a group delay variation of 20.3 ps are obtained. Using a 10-tap feedforward equalizer (FFE), opto-electrical eye diagrams are captured and for 128 GBd NRZ, a sensitivity of -5.9 dBm is measured at a bit error rate (BER) of 1E-12. For 112 GBd PAM4, the KP4 sensitivity level is -4.8 dBm. The input-referred noise is measured at 18.8 pA/√Hz.**

***Index Terms*—Optical receivers, Broadband amplifiers, Distributed amplifiers, BiCMOS integrated circuits, High-speed electronics, Silicon photonics, Photodiodes**

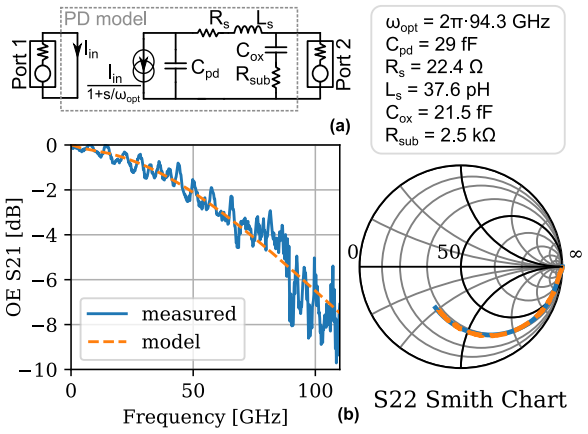

Fig. 1. Equivalent schematic (a) used to model the photodiode. This model is fitted to measurement data of the opto-electronic S21 (b) and the electrical impedance (c) of the photodiode.

I. Introduction

DRIVEN by the explosive growth of artificial intelligence, cloud computing and big data applications, the amount of data center traffic keeps increasing rapidly. This creates a growing need for high-speed interconnects, with the industry looking towards 800 Gbps and 1.6 Tbps links [1], [2]. To achieve such speeds without increasing the amount of lanes, symbol rates of 100 GBd and beyond are being studied [3], [4].

In order to achieve such high symbol rates at the receiver, the transimpedance amplifier (TIA) must exhibit a relatively flat frequency response with a sufficiently high bandwidth [5] while maintaining a low noise performance. The frequency response is often mainly determined by the TIA input impedance, combined with the photodiode (PD) capacitance and interconnect (e.g. bond wire) inductance. In the typically-used shunt-feedback (SFB) TIA topology, these input parasitics can cause excessive amplitude peaking and a steep high-frequency roll-off, often exacerbated by inductive peaking techniques used to extend the bandwidth [6]. Moreover, the loop gain in a SFB topology is constrained by the transition frequency f_T of the transistors used and stability consideridations [7]. At high frequencies, this loop gain deteriorates, leading to an increase in input impedance. In contrast, TIA architectures that avoid feedback mechanisms, such as a resistor with post-amplification or a traveling-wave TIA, are not affected by this limitation. Even though both these architectures are functionally equivalent at DC, the high-frequency performance of the traveling-wave topology is enhanced due to the distribution of the gain cells along the input and output transmission lines [8]. Additionally, the traveling-wave topology causes a filtering effect on the thermal noise of the input line load resistor [9].

Indium Phosphide SFB-TIAs with bandwidths above 100 GHz [10], [11] have been demonstrated before, as well as a 95-GHz [12] and a 92-GHz [13] SFB-TIA implemented in SiGe BiCMOS, but they are only measured electrically and do not account for the bandwidth-limiting effect of connecting a PD. Other direct detection SFB-TIAs in BiCMOS [14]–[16] and standard CMOS [17] exhibit high bandwidths, but their time domain performance is typically measured electrically and only at data rates below 112 Gbps. In [18], a 128 GBd 16QAM coherent BiCMOS SFB-TIA is demonstrated opti-

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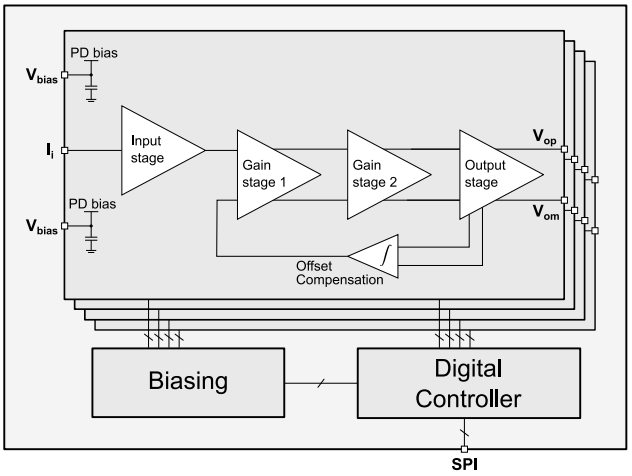

Fig. 2. Block diagram of the 4-channel TIA chip.

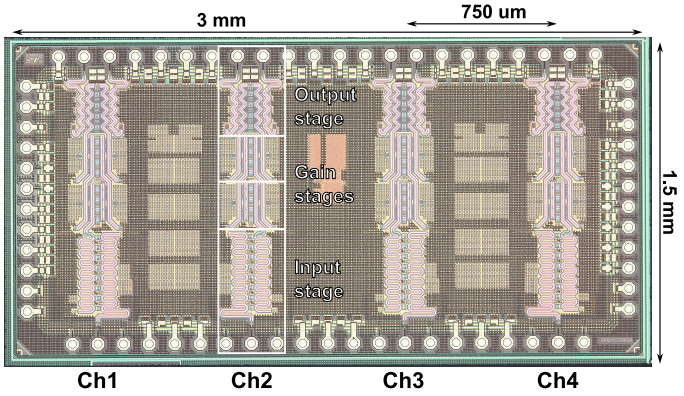

Fig. 3. Micrograph of the 4-channel TIA die.

cally, but its noise level is much higher than typical direct detection receivers since a coherent receiver can typically take advantage of the gain provided by a local oscillator laser. FinFET TIAs [19]–[21] typically make use of a SFB topology as well, but only achieved bandwidths below $50\,\mathrm{GHz}$. Commercial systems exceeding $100\,\mathrm{GBd}$ are already available, with Ciena reporting $200\,\mathrm{GBd}$ systems [22], although detailed implementation specifics remain proprietary.

In this paper, a traveling-wave (TW) topology is used as an alternative to the SFB topology to achieve high bandwidth. A $55\,\mathrm{nm}$ SiGe BiCMOS linear TIA is designed, achieving a bandwidth of $64\,\mathrm{GHz}$ including PD and bond wire parasitics. NRZ and PAM4 eye diagrams are measured at rates up to $128\,\mathrm{GBd}$, and the corresponding sensitivity levels are reported.

This work expands on our previous work [23], providing an accurate opto-electronic model for the photodiode and a detailed discussion of the circuit-level design (Section II). More elaborate measurement results are presented (Section III), including the frequency response, linearity, and noise performance of this receiver. Additionally, the receiver sensitivity is analyzed through bit-error rate (BER) measurements. Section IV compares the measured performance to other state-of-the-art optical receivers.

II. Circuit Description

A. Photodiode Modeling

In high-speed optical receivers, the photodiode (PD) is crucial for achieving optimal performance. To effectively assess the performance of the PD when integrated with the TIA chip, an accurate model of the photodiode is essential. The germanium PD used in this work is part of the iSiPP200 silicon photonics platform and has a responsivity of $0.89\,\mathrm{A/W}$. Its frequency response was measured using an RF probe connected to a ME7848A-200 opto-electronic network analyzer, and is shown in Fig. 1(b). The equivalent circuit model of Fig. 1(a) was then fitted to this data. The carrier transit time is modeled by ω_{opt}, while C_{pd} models the junction capacitance. R_s and L_s mainly describe the series impedance caused by the contacts and interconnects, and C_{ox} and R_{sub} model the parasitic coupling via the substrate.

B. TIA Chip Architecture

The 4-channel traveling-wave TIA was designed and fabricated in a $55\,\mathrm{nm}$ BiCMOS process with a nominal f_T of $320\,\mathrm{GHz}$. Fig. 2 shows the block diagram of this chip. Each channel consists of an input stage, two gain stages and an output stage, all of which are traveling-wave amplifiers. The photodiode anode connects to the single-ended input, but the outputs are differential. The offset added by the two gain stages and the output stage is compensated by sensing the DC differential offset at the output using an operational amplifier and feeding it back to one of the differential inputs of the first gain stage. Simulations indicate that the low-frequency cut-off frequency of this offset compensation loop remains below $300\,\mathrm{kHz}$ across all design corners.

The chip also contains an on-chip reference bias generator and a digital controller, which allows setting the gain and peaking of certain amplifiers. A single $2.5\,\mathrm{V}$ supply is used for the entire chip, apart from the photodiode cathode bias voltage, which is supplied externally. The photodiode cathode is connected to the chip on both sides of the anode to minimize bond wire inductance. Additionally, on-chip decoupling for the cathode bias voltage is implemented near the bond pads.

Fig. 3 shows a micrograph of the die with its 4 TIA channels. The individual traveling-wave stages are indicated on the second channel, which is the channel measured in section III. The chip dimensions are indicated as well, with each channel occupying an area of $1.125\,\mathrm{mm}^2$. The bondpads at the input and output side have a pitch of $125\,\mu\mathrm{m}$.

C. Input Stage

The block diagram of the input stage is shown at the left side of Fig. 4. It has a traveling-wave topology and is made of 8 gain cells, each containing an input TL, gain cell amplifier and output TL. The input TL (T1) is a microstrip line with a width of $1.44\,\mu\mathrm{m}$, yielding a characteristic impedance Z_T of about $70\,\Omega$. The output TL (T2) is $1.08\,\mu\mathrm{m}$ wide and exhibits a Z_T of about $75\,\Omega$. Due to the periodic capacitive loading of the gain cell amplifiers, the equivalent Z_T of the input and output lines drops to about $50\,\Omega$. An additional TL at the input acts as a matching network to absorb the parasitic capacitance of the input bondpad and the ESD diodes

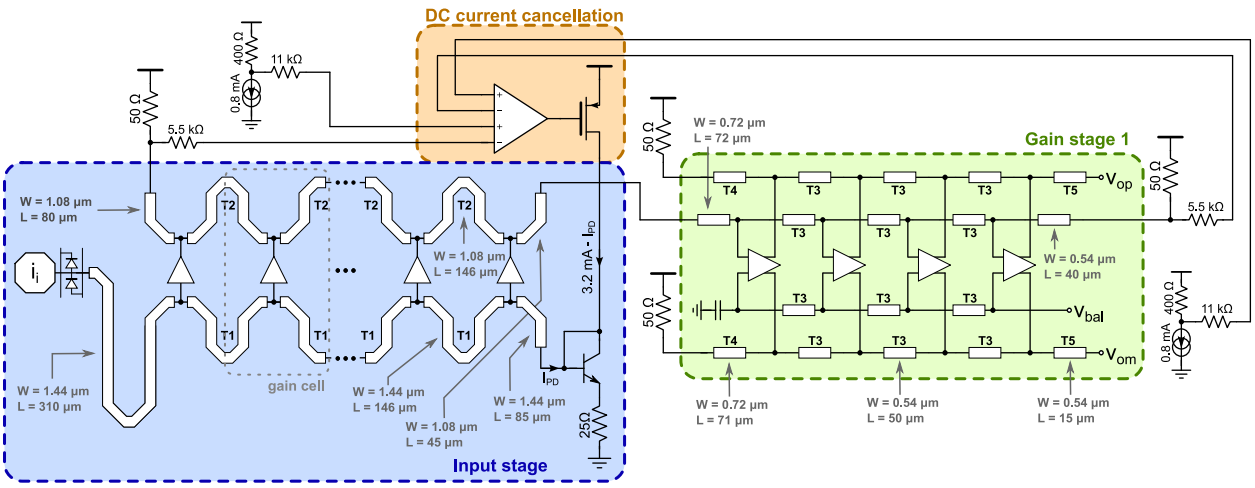

Fig. 4. Circuit diagram of the input stage and first gain stage.

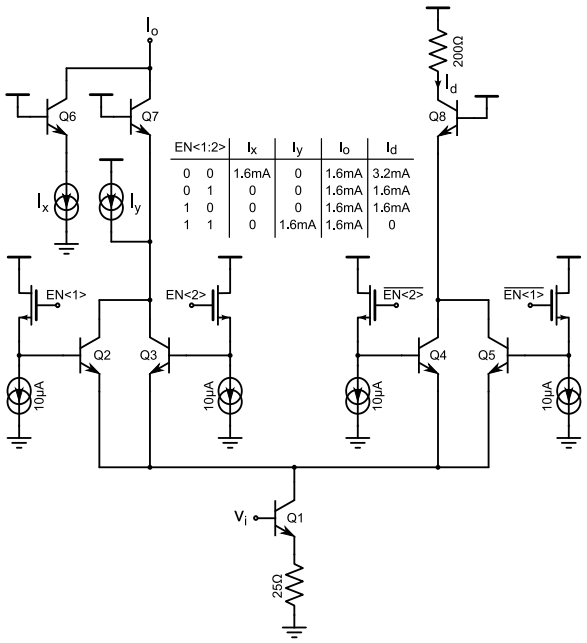

Fig. 5. Circuit diagram of the input stage cell amplifier.

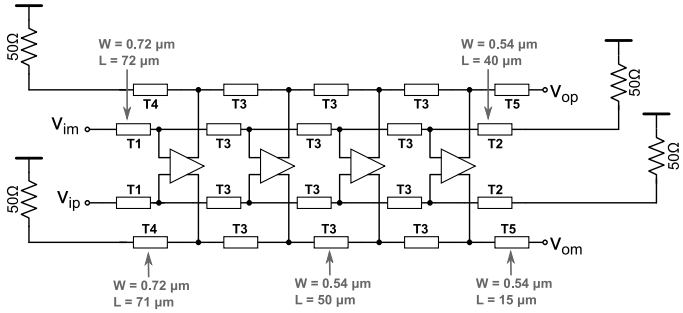

Fig. 6. Circuit diagram of the second gain stage.

(30 fF and 12 fF respectively). A degenerated, diode-connected bipolar transistor with an equivalent impedance of $50\,\Omega$ acts as the termination for the input TL, while allowing the DC input voltage of the gain cell amplifiers to be controlled. The output TL is terminated at the left side with a $50\,\Omega$ resistor and at the right side it is terminated into the input impedance of the first gain stage.

Fig. 5 shows the circuit diagram of the input stage gain cell amplifier. The input transistor Q1 acts as a degenerated common-emitter amplifier. Transistors Q2-5 act as cascodes and can be turned on/off with the digital EN<1:2> signal to steer the signal current towards the output or into a dummy load. In this way, each input stage cell can be fully on, at half gain, or fully off. This reduction in gain is necessary to support linear operation for high input current swings (up to $2\,\mathrm{mApp}$) . In order to keep the DC voltage at the output node constant across gain settings, the current sources I_x and I_y are switched as indicated in the table of Fig. 5, keeping the DC output current (I_o) at a constant value of $1.6\,\mathrm{mA}$. The collector current of Q1 is $3.2\,\mathrm{mA}$, and is also constant for every gain setting.

Because the collector current of Q1 mirrors the collector current of the diode-connected transistor at the end of the input transmission line (Fig. 4), these input transistors are biased by controlling the current through this diode-connected transistor. A differential difference amplifier [24] compares the DC voltage at both ends of the input stage output TL with two co-located reference voltages to control this current, creating a feedback loop that sets the current through each termination resistor at $6.4\,\mathrm{mA}$, i.e., $1.6\,\mathrm{mA}$ per gain cell. This loop also cancels the DC photocurrent I_{PD} (up to $\pm 2\,\mathrm{mA}$), as is indicated in Fig. 4.

D. Gain Stages

The first gain stage comes after the input stage (Fig. 4). It is a differential traveling-wave amplifier, consisting of 4 gain cells. The interstage transmission lines have a width of $0.54\,\mu\mathrm{m}$, corresponding to a characteristic impedance of about $80\,\Omega$. One of the differential inputs is connected to the single-ended output of the input stage, the other input (V_{bal}) is connected to the low-speed output of the offset compensation amplifier. The second gain stage has the same design as the

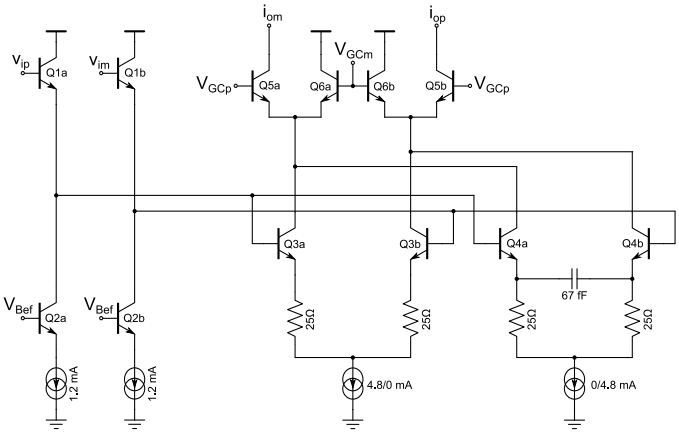

Fig. 7. Circuit diagram of the gain stage cell amplifier.

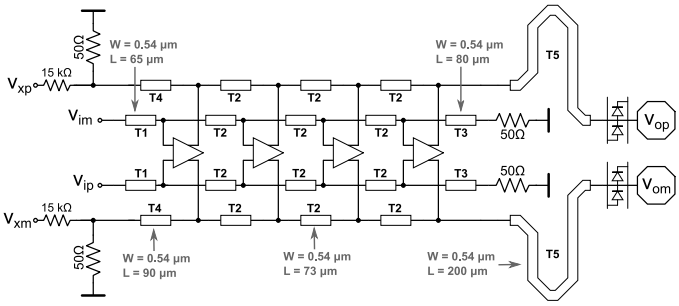

Fig. 8. Circuit diagram of the output stage.

first gain stage, apart from the input since now a differential signal is applied to it (Fig. 6).

Fig. 7 shows the circuit diagram of the cell amplifier used in both gain stages. First, the differential input is buffered by emitter followers (Q1), after which it is amplified by a degenerated differential pair (Q3). A second differential pair (Q4) is placed in parallel, but here a capacitor is placed in between the emitters to provide gain peaking. When this peaked differential pair is enabled, the other is disabled such that the DC gain stays the same. In combination with the differential pair, cascode transistors Q5 and Q6 constitute a signal-summing variable gain amplifier (VGA), which has a very wide attenuation range at both low and high frequencies with low distortion [25].

E. Output Stage

Finally, the output stage (Fig. 8) consists of 4 differential traveling-wave cells as well, but with a different implementation. The transmission lines also have a width of $0.54\,\mu\mathrm{m}$, but they are longer. At the output, an additional TL acts as a matching network to absorb the parasitic capacitance of the output bondpad and the ESD diodes. At the other side of the output TL, the DC levels v_{xp} and v_{xm} are tapped off to feed to the offset compensation amplifier as shown in Fig. 2.

Fig. 9 shows the circuit diagram of the output stage gain cell amplifier. Again, the input is buffered by emitter followers (Q1), after which it is amplified by a degenerated differential pair (Q3) with split tail currents. To support a large linear

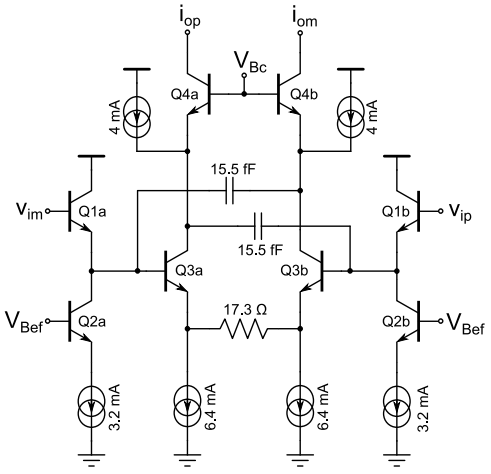

Fig. 9. Circuit diagram of the output stage cell amplifier.

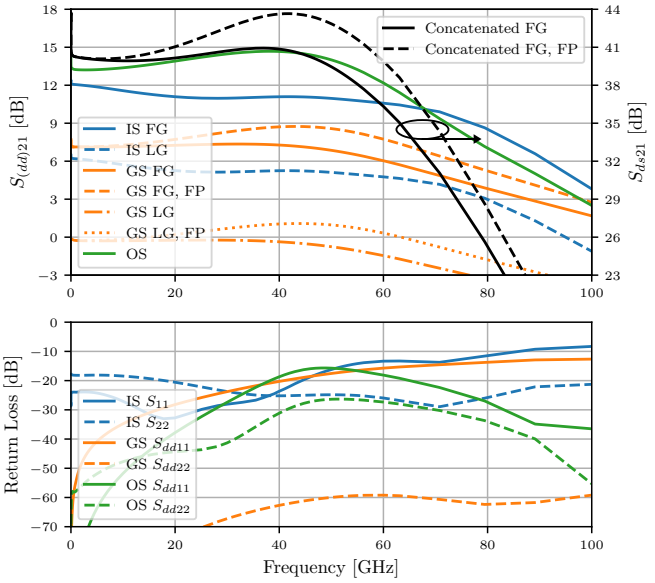

Fig. 10. Simulated S parameters of the different traveling-wave stages, at different settings (IS: Input stage, GS: Gain stage, OS: Output stage, FG: Full gain, LG: Lowered gain, FP: Full peaking). When these stages are concatenated, the black S_{ds21} curves are obtained.

output swing, the tail current is significantly higher than in the gain stage cell amplifiers. In order to maintain enough voltage headroom at the output, $4\,\mathrm{mA}$ is tapped off below the cascode transistors Q4. This leaves a DC output current of $2.4\,\mathrm{mA}$, identical to the output current of the gain stages. Cross-coupled capacitors are used to neutralize the parasitic base-collector capacitance of Q3, reducing its negative effect on the bandwidth.

F. Simulation Results

Fig. 10 shows simulation results of each stage, all terminated with $50\,\Omega$ at the in- and outputs. The simulations were performed in the nominal corner at 70 °C with layout

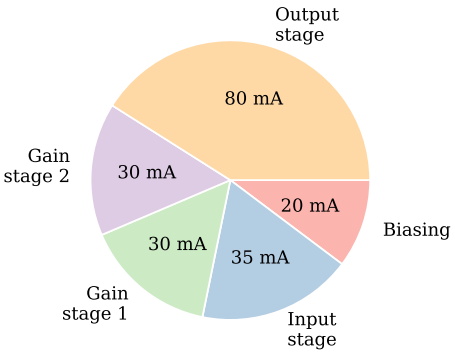

Fig. 11. Current consumption of each building block of a single TIA channel.

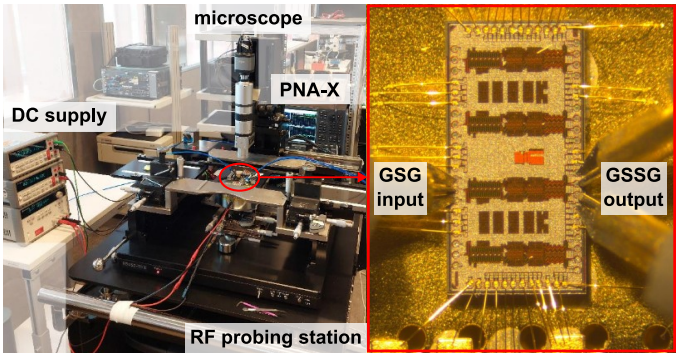

Fig. 12. Frequency domain measurement setup, with the TIA in- & output probed.

parasitics extracted and the transmission lines modeled as S-parameter blocks, extracted using a 3D electromagnetic simulator (EMX).

When driven by a $50\,\Omega$ source, the input stage has a gain of $12.1\,\mathrm{dB}$ (at $1\,\mathrm{GHz}$) and a $3\,\mathrm{dB}$ bandwidth of $74\,\mathrm{GHz}$. If the gain setting is halved (EN<1:2> = 01 for each cell), the gain is reduced to $6.2\,\mathrm{dB}$. The gain stage has a differential gain of $7.1\,\mathrm{dB}$ and a bandwidth of $72.2\,\mathrm{GHz}$. By enabling the gain peaking differential pair (Fig. 7) in each cell, $1.5\,\mathrm{dB}$ peaking is added at $43\,\mathrm{GHz}$, boosting the bandwidth of this stage to $84\,\mathrm{GHz}$. The gain of this stage can be lowered as well, as illustrated in Fig. 10 where the gain is reduced to $-0.25\,\mathrm{dB}$. Finally, the output stage has a differential gain of $13.2\,\mathrm{dB}$ and a bandwidth of $64.4\,\mathrm{GHz}$ with $1.5\,\mathrm{dB}$ gain peaking at $38\,\mathrm{GHz}$. If the input stage is concatenated with 2 gain stages and the output stage as in Fig. 2, a total simulated gain of $40.2\,\mathrm{dB}$ is obtained with a bandwidth of $58\,\mathrm{GHz}$. By enabling the gain peaking in both gain stages, the bandwidth is extended to $66\,\mathrm{GHz}$. The lower graph of Fig. 10 shows that these traveling-wave stages are well matched to the $50\,\Omega$ terminations up to at least $85\,\mathrm{GHz}$.

G. Power Consumption

The TIA consumes a current of $195\,\mathrm{mA}$, and 4 of these TIAs are integrated on a single chip. Since the supply voltage is $2.5\,\mathrm{V}$, the power consumption amounts to $487.5\,\mathrm{mW}$ per channel. At a data rate of $224\,\mathrm{Gbps}$, this receiver hence achieves an efficiency of $2.2\,\mathrm{pJ/bit}$. Fig. 11 shows the current consumption of each block. To support a large linear output swing, the output stage consumes significantly more current than the other stages.

III. Experimental Results

A. S-parameters

To evaluate the electrical response of the TIA chip, a die was assembled on a PCB with bond wire connections for the supply and control lines, as shown on the right of Fig. 12. This assembly was placed into an RF probing station where a GSG RF probe was used to contact the input while a GSSG probe contacted the output. 3-port S-parameters were measured with the PNA-X N5247B vector network analyzer,

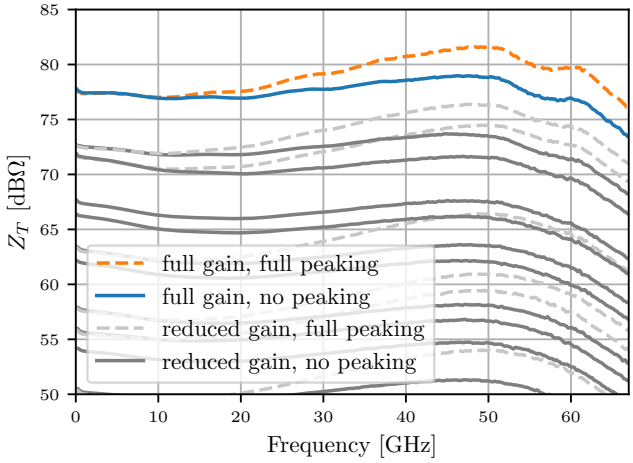

Fig. 13. Measured transimpedance gain for various gain and peaking settings. The colored curves correspond to the maximum gain setting, while the different gray curves represent reduced gain settings.

after a calibration was performed up to the probe tips. The port power at the chip input was kept low ($-40\,\mathrm{dBm}$), ensuring that the TIA operated in its linear regime.

The measured S-parameters can be used to calculate the single-ended to differential transimpedance gain, which is defined in the following way:

$$Z_T = \frac{S_{21} - S_{31}}{1 - S_{11}} \cdot Z_0 \tag{1}$$

with port 1 at the input and $Z_0 = 50\,\Omega$. This is plotted in Fig. 13 for various gain settings and with or without the gain peaking setting enabled in both gain stages. At the maximal gain setting, the low frequency ($1\,\mathrm{GHz}$) transimpedance gain is $77\,\mathrm{dB}\,\Omega$. The $3\,\mathrm{dB}$ bandwidth is $65\,\mathrm{GHz}$ and enabling the peaking setting adds $2.7\,\mathrm{dB}$ gain peaking at $48\,\mathrm{GHz}$, shifting the $3\,\mathrm{dB}$ bandwidth beyond the $67\,\mathrm{GHz}$ measurement range of the PNA-X.

Fig. 14 shows the measured input (S_{11}) and differential output return loss (S_{dd22}) of the TIA, for the same settings as in Fig. 13. The input is well-matched (i.e., $S_{11} < -10dB$) to a $50\,\Omega$ load for frequencies up to $55\,\mathrm{GHz}$. The differential output remains well-matched for the entire measurement range.

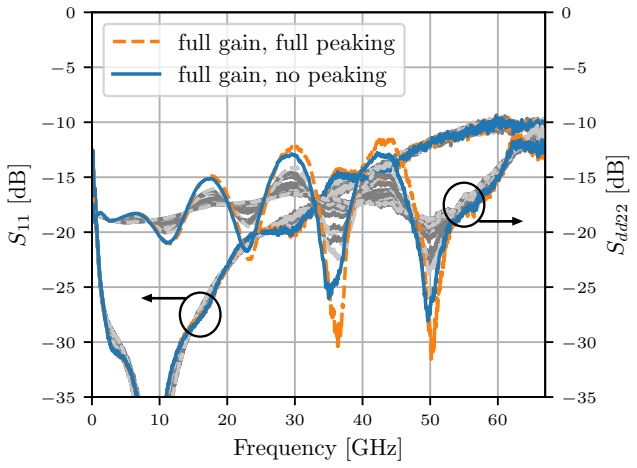

Fig. 14. Measured input and (differential) output return loss, for various settings.

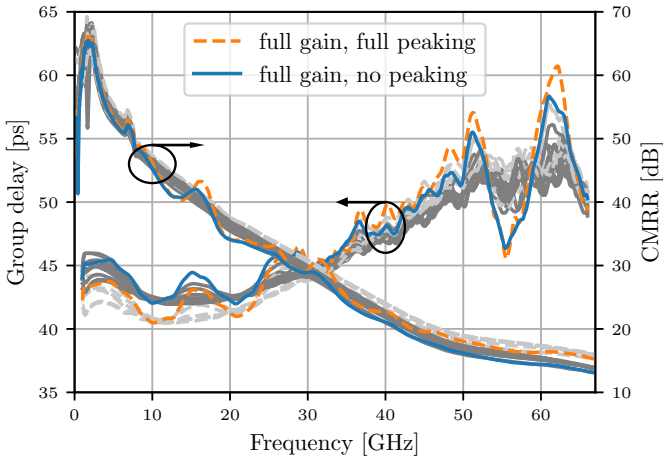

Fig. 15. Measured group delay and CMRR, for various settings.

The measured group delay is shown in Fig. 15. Without any peaking settings enabled, the group delay variation (GDV) is 16.4 ps. Enabling peaking increases the GDV to 20.3 ps. Fig. 15 also shows the measured common-mode rejection ratio (CMRR), which is defined as follows:

$$CMRR = \frac{S_{21} - S_{31}}{S_{21} + S_{31}} \tag{2}$$

again with port 1 at the TIA input, and ports 2 and 3 at the output. The CMRR at low frequencies extends beyond 60 dB, but lowers as the frequency increases. However, at least 13 dB of CMRR is still measured at 67 GHz, and even 15 dB with the peaking setting enabled.

The bandwidth of a TIA receiver is primarily determined by the photodiode and bond wire parasitics. Therefore, a simulation was performed where the measured S-parameter results were combined with a parasitic PD model (see Section II-A) and bond wire inductance according to the circuit diagram in Fig. 16. The three bond wire connections are each modeled by an inductance of L_{bw}, which is varied from 100 pH to 300 pH

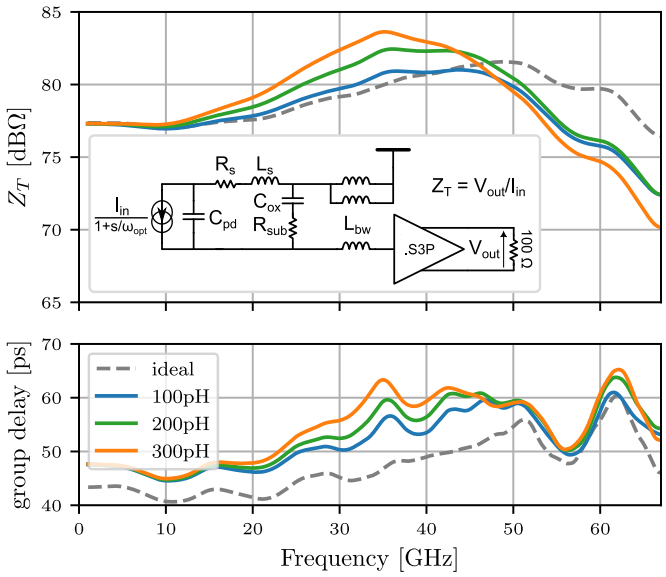

Fig. 16. Effect of photodiode and bond wire parasitics on the measured S-parameter results (full gain, full peaking). The bond wire inductance L_{bw} is varied from 100 pH to 300 pH. The ideal curve represents the situation without parasitics.

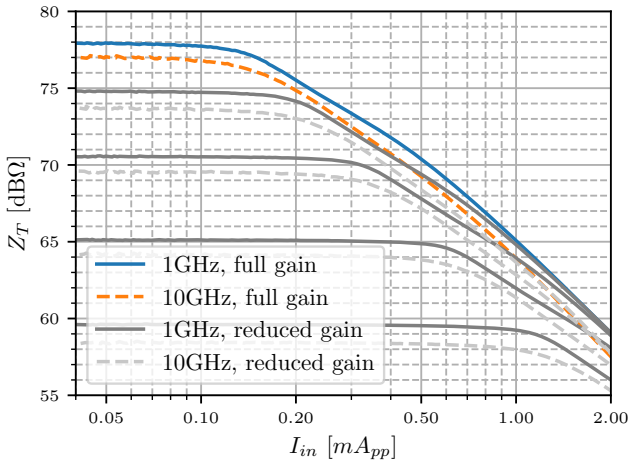

Fig. 17. Measured transimpedance gain as a function of input current swing at 1 GHz and 10 GHz. Curves for various gain settings are plotted.

in Fig. 16. As expected, the parasitics limit the 3 dB bandwidth to 64 GHz for $L_{bw} = 100$ pH and 200 pH and 61 GHz for 300 pH. The 6 dB bandwidth is higher than 67 GHz, unless for $L_{bw} = 300$ pH where it is 65 GHz. More L_{bw} causes the frequency response to peak more (6.5 dB for $L_{bw} = 300$ pH), but this peaking is spread gradually across a wide frequency range. Fig. 16 also shows the effect of these parasitics on the group delay, the total GDV does not increase significantly and stays limited to 20.3 ps.

B. Linearity

Using the differential I/Q mode of the PNA-X, two power sweeps were performed with input signals of 1 GHz and 10 GHz while measuring the power of the fundamental frequency and harmonics at all the ports. Fig. 17 shows the mea-

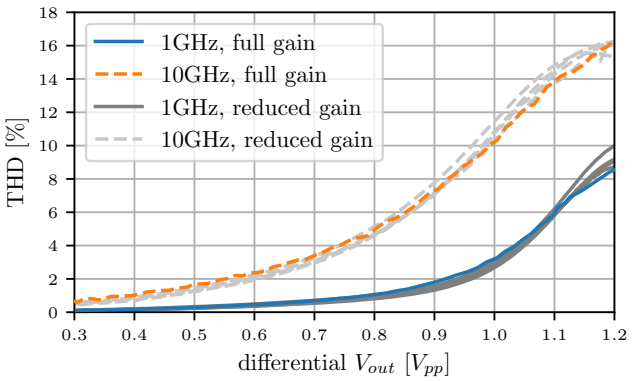

Fig. 18. Measured THD as a function of the resulting differential output voltage, for a fundamental frequency of 1 GHz and 10 GHz. Each curve represents a different gain setting, where the input power swing is swept.

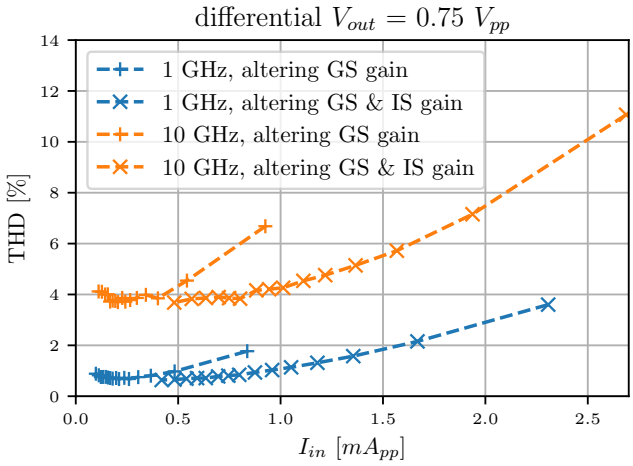

Fig. 19. Measured THD as a function of input current, while the output swing is kept constant at 0.75 Vppd by adjusting the gain settings.

sured transimpedance gain (1) at the fundamental frequency as a function of input current swing. At full gain, the 1 dB compression point occurs at an input swing of 150 µA. To accommodate higher input swings, the gain setting should be reduced.

The total harmonic distortion (THD) is defined as the ratio of the power of the harmonics to the power of the fundamental frequency at the differential TIA output:

$$THD = \sqrt{\frac{P_2 + P_3 + P_4 + P_5 + P_6}{P_1}} \tag{3}$$

with P_i the output power at the ith harmonic. In this case, harmonics of order 7 and above were negligibly small and not taken into account. In Fig. 18, the input current swing is varied, but the THD is plotted as a function of the resulting differential output voltage. The THD curves don't vary much for different gain settings, indicating that the linearity performance is mainly determined by the output stage. At an output voltage of 750 mVpp, the THD is below 1% at a fundamental frequency of 1 GHz. At 10 GHz, this value increases to 4%. This is mainly caused by peaking effects which increase the gain at higher frequencies [26], such as parasitic capacitance across a degeneration resistor decreasing the amount of degeneration at higher frequencies and thus causing more nonlinearity.

Fig. 19 shows the THD for increasing input current swing, while the differential output swing is kept constant at 0.75 Vpp by lowering the gain setting. This allows us to evaluate the linearity performance at high input swings. By reducing the gain stage and input stage gain appropriately, the THD at 1 GHz can be kept below 2% for input swings up to 1.6 mApp. At a fundamental frequency of 10 GHz, it can stay below 5% for swings up to 1.3 mApp.

C. Opto-electrical Eye Diagrams

The experimental setup of Fig. 20 was used to evaluate the performance of this TIA in a direct-detection optical receiver. The arbitrary waveform generator (AWG, M8199B) generates an NRZ or PAM4 signal from a PRBS13 bitstream. This

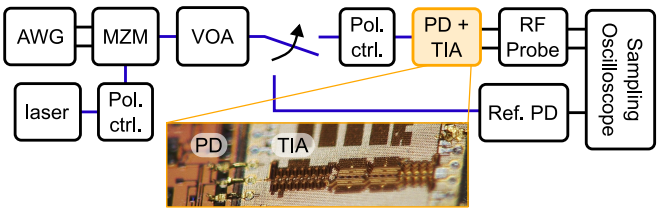

Fig. 20. Experimental setup for the opto-electrical eye diagram measurements.

signal drives the thin film lithium niobate mach-zehnder modulator (MZM), biased at its quadrature point, modulating the 1550 nm optical carrier. The extinction ratio of the transmitted signals is measured to be 3.5 dB, 3.2 dB and 2.9 dB when operating at a symbol rate of 106.25 GBd, 112 GBd and 128 GBd, respectively. A variable optical attenuator (VOA) is used to control the received optical power which is then coupled to the receiver assembly with a fiber probe. A GSSG RF probe is used to contact the differential output of the TIA, where short coax cables are used to connect to the remote sampling heads of the sampling oscilloscope, capturing the output waveforms. A 70 GHz PD (XPDV3120R) connected to a third remote sampling head is used to characterize the transmitter frequency response, which is de-embedded at the AWG such that only the receiver impairments have an impact on the measurement.

The receiver assembly consists of the TIA chip where one channel is wire bonded to the PD which resides on a photonic integrated circuit (PIC), as shown in Fig. 20. The grating coupler incurs a loss of around 3 dB. The PD cathode is biased at 3.3 V, which causes a reverse bias of 2.3 V across the PD.

In Fig. 21, the obtained BER results are plotted as a function of the optical modulation amplitude (OMA) power in the on-PIC waveguide incident on the photodiode. For this experiment, the gain of the TIA was lowered to 57.3 dB Ω and a symbol-spaced feedforward equalizer (FFE) with 3 pretaps and 7 posttaps was used to remove the intersymbol interference (ISI) caused by gain and group delay variation

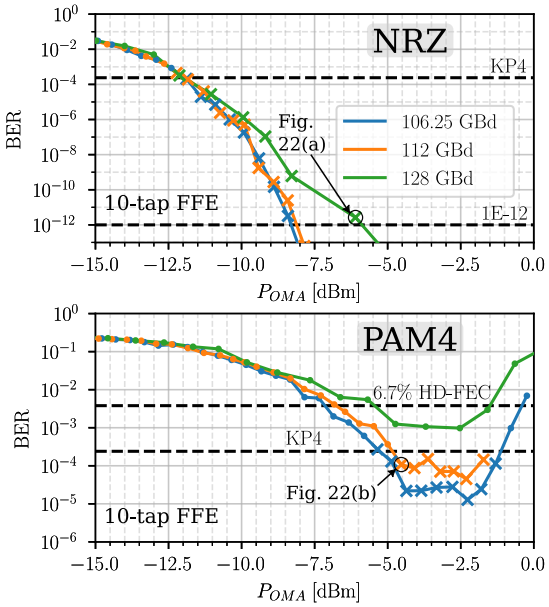

Fig. 21. Measured BER of the receiver assembly as a function of the received OMA power, for NRZ and PAM4 data at symbol rates from 106.25 GBd up to 128 GBd. The point markers indicate results obtained by error counting and the cross markers indicate the estimated BER based on the noise statistics.

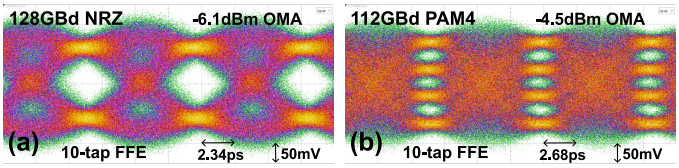

Fig. 22. Measured eye diagrams at the output of the TIA for (a) 128 GBd NRZ and (b) 112 GBd PAM4.

in the transimpedance response (see Fig. 16). Only a limited amount of data could be captured and since the method of BER counting is only statistically significant for high error rates where at least 10 errors occurred, the BER was estimated in the case of less errors. This was done by fitting Gaussian probability distributions to the sampled signal points to describe the noise distribution. The BER results obtained with the counting method are indicated with point markers in Fig. 21, while the results obtained by estimation are indicated with cross markers.

For the NRZ experiments, the receiver exhibits a sensitivity of $-7.8\,\mathrm{dBm}$ and $-7.6\,\mathrm{dBm}$ at a BER of 1E-12 for $106.25\,\mathrm{GBd}$ and $112\,\mathrm{GBd}$, respectively. At $128\,\mathrm{GBd}$, a higher sensitivity level of $-5.9\,\mathrm{dBm}$ is measured. Fig. 22(a) shows a $128\,\mathrm{GBd}$ NRZ eye diagram close to this sensitivity level. Note that due to the inability to capture enough data to be statistically relevant at a BER of 1E-12, these NRZ sensitivity figures were not obtained using error counting. Using PAM4 modulation, a sensitivity of $-5.3\,\mathrm{dBm}$ and $-4.8\,\mathrm{dBm}$ is obtained at the KP4 forward error correction (FEC) BER limit of 2.4E-4 for $106.25\,\mathrm{GBd}$ and $112\,\mathrm{GBd}$, respectively. At $128\,\mathrm{GBd}$ the BER stays above the KP4 limit, but exhibits a $-5.5\,\mathrm{dBm}$ sensitivity when using the 6.7% hard decision (HD) FEC limit at a BER of 3.8E-3. A $112\,\mathrm{GBd}$ PAM4 eye diagram below the KP4 FEC limit is shown in Fig. 22(b). The rise in BER at high optical input powers is due to the TIA being overloaded. While further reducing the TIA gain could prevent this, the gain was held constant for these experiments.

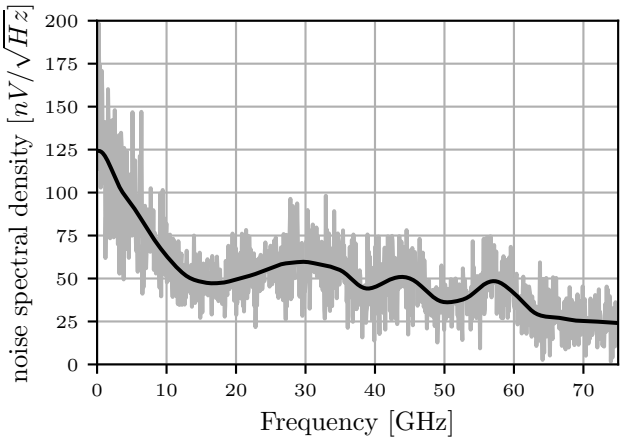

Fig. 23. Measured noise spectral density at one side of the differential output.

D. Noise Performance

To measure the output noise voltage of the TIA, the opto-electrical receiver assembly of Fig. 20 was used while the optical input remained dark. The differential output noise was sampled by the sampling oscilloscope, of which the frontend bandwidth was set to $75\,\mathrm{GHz}$. By calculating the standard deviation of the obtained samples, the integrated root mean square (rms) noise voltage was determined. At the full gain setting, an integrated noise of $33.6\,\mathrm{mVrms}$ is measured at the TIA output. Compared to this value, the noise of the sampling scope ($0.89\,\mathrm{mVrms}$) is negligible. This can be attributed to the high gain of the chip. Dividing the integrated output noise by the midband transimpedance gain ($77\,\mathrm{dB\,\Omega}$) yields the input-referred integrated noise. In this case the input-referred integrated noise amounts to $4.75\,\mu\mathrm{Arms}$. Assuming $64\,\mathrm{GHz}$ noise bandwidth, this corresponds to an averaged input-referred noise current density of $18.8\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$.

To measure the noise spectral density, one side of the differential output was connected to a $75\,\mathrm{GHz}$ spectrum analyzer, while the other side was terminated into $50\,\Omega$. The measured noise spectral density is given in Fig. 23. Integrating this noise density yields a single-ended output noise of $15.5\,\mathrm{mVrms}$. Under the assumption that the single-ended input stage contains all dominant noise sources, the differential spectral noise density at the output will be twice as large. Hence, the integrated differential output noise will be $31.0\,\mathrm{mVrms}$, which agrees with the sampling scope measurement. The reduction in noise spectral density at higher frequencies compared to DC is due to a filtering effect on the noise generated by the input line termination. Because this noise originates at the far end of the input line, it undergoes frequency-dependent destructive interference as it travels through the input stage [9].

TABLE I
COMPARISON WITH STATE-OF-THE-ART HIGH-BAUDRATE RECEIVERS

	[13]	**[27]**	**[17]**	**[14]**	**[15]**	**[16]**	**[28]**	**[18]**	**This work**
Z_T [dBΩ]	47	47	65	71	54	55	66	70	**77**
3 dB BW [GHz]	92[b]	39	60	65	75[b]	75[b]	73	75	**64**
Data rate [GBd]	120 NRZ[c]	40 NRZ	56 PAM4[c,e]	112 NRZ[c] 50 PAM4[c]	100 NRZ[c]	50 NRZ[c]	120 NRZ[c]	128 16QAM	**128 NRZ[d,f] 112 PAM4[d,f]**
Sensitivity [dBm] (BER)	-	-	-5.1[a] (2E-4)	-	-	-	-	-16 (2E-2)	**-5.9 (1E-12) -4.8 (2.4E-4)**
GDV [ps]	3[a]	10	20	8	8	11.8	12	-	**20.3**
Noise [pA/$\sqrt{\text{Hz}}$]	17.7[a]	24	19.3	7.2	10.9	20.4	6.3	46	**18.8**
Power [mW]	48	300	107	345	95	89	145	267	**487.5**
Efficiency [pJ/bit]	0.4	7.5	0.96	3.1	0.95	1.8	1.2	1.0	**2.2**
Technology	55nm BiCMOS	180nm BiCMOS	28nm CMOS	130nm BiCMOS	130nm BiCMOS	130nm BiCMOS	130nm BiCMOS	55nm BiCMOS	**55nm BiCMOS**
TIA topology	SFB	TW	SFB	SFB	SFB	SFB	diff. SFB	diff. CB-SFB	**TW**

[a]Simulated, [b]Without PD, [c]Electrical input, [d]Lowered Z_T setting, [e]Using 3-tap FFE, [f]Using 10-tap FFE

IV. COMPARISON WITH STATE OF THE ART

In Table I, the measured performance of the presented receiver is compared to other state-of-the-art optical receivers. Commercial systems exceeding 100 GBd are already available, but limited information is accessible due to their proprietary nature, which is why they are not included in this table. There is one other TW-TIA in the list [27], but it has a lower gain and bandwidth than our TIA and the time domain experiments are limited to 40 Gbps. Some BiCMOS SFB-TIAs [13]–[16], [18], [28] demonstrate a higher bandwidth than our chip. However, the bandwidth of [13], [15], [16] is measured without taking the effects of connecting to a PD into account (i.e., the electrical bandwidth is reported in this table), while the opto-electronic bandwidth is listed for the other TIAs. Additionally, the time-domain measurements are limited to significantly lower data rates in [14], [16], [17], and they are limited to NRZ waveforms in [13], [15], [28]. Optical sensitivity and BER are reported in [17], but only based on simulation. The only coherent receiver [18] in this list reports a much lower sensitivity, even with a much higher noise level, which is made possible by the coherent mixing with a local oscillator laser of 10.3 dBm. The time-domain measurements of [13]–[17], [28] were performed with the input applied electrically.

The power consumption of our TIA can be mostly attributed to the high-swing output stage (see Fig. 11), which is not included on [13], [15], [16], [27]. However, a relatively high power consumption is a typical disadvantage of a TW topology, since in a traveling-wave amplifier the gain of each cell is added and not multiplied as in a typical cascaded amplifier, and half of the signal power on the output line is lost in the reverse termination [29]. This is also evident from [27], which has a high power consumption as well.

V. CONCLUSION

This paper presents an optical receiver using a SiGe BiCMOS traveling-wave TIA chip with a bandwidth over 67 GHz and a transimpedance gain up to 77 dB Ω. By reducing the gain, the THD at 1 GHz (10 GHz) can be kept below 2% (5%) for input swings up to 1.6 mApp (1.3 mApp). With a silicon photonic PD wire bonded to this TIA, the maximal bandwidth decreases slightly to 64 GHz with a group delay variation of 20.3 ps. Opto-electrical time domain experiments were performed with NRZ and PAM4 data at symbol rates from 106.25 GBd up to 128 GBd, with a transimpedance gain of 57.3 dB Ω. Using a 10-tap feedforward equalizer (FFE), a sensitivity of −7.6 dBm is measured at a bit error rate (BER) of 1E-12 for 112 GBd NRZ and −5.9 dBm for 128 GBd NRZ. When receiving PAM4, the KP4 FEC sensitivity level is −4.8 dBm when operating at 112 GBd. At 128 GBd PAM4, a sensitivity of −5.5 dBm is measured for 6.7% HD-FEC. The integrated input-referred noise of this TIA amounts to 4.75 µArms, i.e., 18.8 pA/$\sqrt{\text{Hz}}$ averaged over its 64 GHz bandwidth. This demonstrates the traveling-wave topology as a promising alternative to the typical shunt-feedback TIAs for the next generation of optical receivers operating at symbol rates above 100 GBd.

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