A 200–256-GS/s Current-Mode 4-Way Interleaved Sampling Front-End With Over 67-GHz Bandwidth Using a Slew-Rate Insensitive Clocking Scheme

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***Abstract*— The surge of data traffic in emerging optical communication applications has led to the development of ultra-fast transceivers with extremely high data throughput. The latest transmitters and receivers aim for symbol rates of 150–200 Gbaud or even higher, striving to achieve bandwidths beyond 70 GHz. However, the current state-of-the-art analog-to-digital converters (ADCs) in advanced CMOS-FinFET technologies can only handle limited analog input bandwidths and sampling rates, becoming a bottleneck in enhancing the overall speed of the transceiver. A time-interleaved sampling front-end acting as an input signal de-interleaver can reduce the sub-ADCs' analog bandwidth and clock jitter requirements. This article investigates a current-mode time-interleaved 1–4 sampling front-end operating at 200–256 GS/s, using a 50% duty-cycle slew-rate insensitive quadrature clocking strategy. The chip was fabricated in a 130-nm SiGe BiCMOS technology and was characterized by single-tone sinusoidal and non-return-to-zero/pulse-amplitude-modulation-4-level (NRZ/PAM-4) measurements at 200, 224, and 256 GS/s. The chip demonstrates a 3-dB analog input bandwidth beyond 67 GHz and a signal-to-noise-and-distortion ratio (SNDR) of 27.8–34.1 dB (at 200 GS/s), 25–36.3 dB (at 224 GS/s), and 22.3–39 dB (at 256 GS/s) for input frequencies from 1.1 to 67.1 GHz. The analog demultiplexing functionality of the sampling front-end is demonstrated with 100, 112, and 128 Gbaud NRZ/PAM-4 measurements. The complete chip consumes a power of 1.1 W at 256 GS/s, corresponding to an efficiency of 4.3 pJ/sample or 4.3 pJ/bit (with two samples per symbol).**

***Index Terms*— BiCMOS integrated circuits, current-mode sampling, demultiplexing, high-speed interleaved sampler.**

I. Introduction

THE next-generation optical communication systems for data-intensive applications such as cloud services, artificial reality/virtual reality, high-performance computing, and autonomous driving expect new technologies and integrated transceiver circuits able to support symbol rates beyond 200 Gbaud. Recently published receiver circuits, such as the transimpedance amplifier (TIA), have shown an electrical 3-dB bandwidth of 75 GHz with a measured baud rate of 128 Gbaud [1]. Lately, state-of-the-art analog-to-digital converters (ADCs) [2], [3], [4], [5], [6] achieved a maximum analog bandwidth and the highest sampling rate of 60 GHz and 200 GS/s [2]. Heavy bandwidth enhancement techniques are utilized to compensate the channel loss in the ADC front-ends [3], [7], [8], [9], [10], [11], [12]. For example, a continuous time linear equalizer (CTLE) with a maximum peaking of 19 dB at 54 GHz was implemented before an ADC sample and hold (S/H), as the sampler only has a 3-dB bandwidth of 34 GHz [7]. Furthermore, in CMOS ADC-based transceivers, digital equalizers are usually exploited for channel loss equalization [3], [4], [8], [9], [12], including the loss from the ADC S/H. However, it is worth noting that digital equalization has become increasingly intricate and power-intensive over time, which comes at the cost of an achievable effective number of bits (ENOBs).

A high-bandwidth pre-sampler acting as an input signal de-interleaver can be used to reduce the sub-ADCs' bandwidth and clock jitter requirements [13], [14], [15], [16], [17], [18]. Recently published time-interleaved 1–2 or 1–4 samplers in silicon-based BiCMOS [13], [14], [15], [16] or InP technologies [17], [18] with f_T/f_{MAX} over 300 GHz can cooperate with CMOS ADCs to push the overall sampling rate beyond 112 GS/s. Among them, the pre-sampler in a 256-GS/s real-time scope [18] using an InP technology has demonstrated the highest sampling rate of 256 GS/s and up to 110 GHz of analog bandwidth. However, this is not a cost-friendly solution for a common data communication system. Some other works reported an analog bandwidth of 100 [19] and 110 GHz [17] in track mode with *S*-parameter measurements. Yet, such small-signal measurements often fall short of accurately capturing the large-signal responses of the sampler in real-world operations.

The pre-samplers are designed to function in either voltage-mode [15], [16], [17] or current-mode [13], [14]. The voltage-mode samplers in silicon technology have presented a sampling rate of up to 200 GS/s [15], [16] and an input signal tracking bandwidth of 20 and 57 GHz at 200 and 128 GS/s, respectively [15]. However, using a switched emitter follower (SEF) in a voltage-mode sampler makes it vulnerable to the

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input signal feedthrough in the hold phase and the base-emitter modulation in the tracking mode. The signal feedthrough is caused by a low-impedance path presented by the base-emitter capacitance in the hold phase, and the base-emitter modulation is because the small current that charges the sampling capacitor distorts the emitter current of the SEF in the tracking mode. Techniques have been investigated to alleviate these issues, for example, using a feedforward capacitor and a switched pre-amplifier (SPA) to silence or attenuate the input signal at the input of SEF in the hold phase [15], [20], [21], [22], [23], [24]. The distortion from the base-emitter modulation can be relieved by injecting a mimic current of the sampling capacitor generated by a dummy branch into the principle sampling path [15], [23], [24], [25]. Both the SPA and dummy branches increase the power consumption and may limit the achievable bandwidth as more loads or cascaded stages are added to the high-speed input signal path.

Compared with voltage-mode samplers, integrating current-mode samplers offers superior immunity to input signal feedthrough in the hold phase and avoids SEF base-emitter modulation in the track mode [13], [14]. Furthermore, in the 1–N current-mode sampler, i.e., the proposed solution in Section III-C, the sub-samplers share the same signal current from the transconductance stage, making the power consumption of the sampler core much lower than the voltage-mode samplers using SEF topology, of which each sub-sampler has its own SEF and pre-amplifier. Published current-mode samplers have shown a sampling rate of up to 128 GS/s with an input signal tracking bandwidth of 36 GHz [14], using non-50% duty-cycle clocks.

The clocking strategy holds significant importance for both current-mode and voltage-mode samplers as it governs their operating principles, performance, and power usage. For example, to ensure the input signal only sees one sampling capacitor at the same time to avoid bandwidth degradation in the voltage sampler, non-overlapping $1/M$ duty-cycle quadrature clocks are required [27], where M is the number of total parallel sub-samplers. To use a 50% duty-cycle quadrature clock strategy in the voltage-mode sampler, each sub-sampler needs an individual input buffer or pre-amplifier to isolate the input signal and the sampling capacitor [15]. While in conventional current-mode samplers [13], [14], 25% duty-cycle quadrature clocks are used, resulting in complex clock generation, distribution, and high power consumption. This work introduces a 256-GS/s sampling front-end based on a current-mode sampling technique utilizing a clock strategy with only 50% duty-cycle clocks. The proposed scheme eliminates the need for multiple input buffers or pre-amplifiers in voltage samplers, as well as the need for non-50% duty-cycle clock generation circuits in current-mode samplers. As a result, it can achieve higher sampling rates while concurrently reducing power consumption, chip area, and overall complexity.

The remainder of this article is organized as follows. Section II briefly discusses the theory of the heterogeneous ADC pre-sampler working principle and the impact of the interconnect bandwidth. Section III presents the proposed current-mode sampler, and Section IV covers the circuit design and implementation. Measurement results are presented and discussed in Section V, and Section VI concludes the article.

II. Heterogeneous ADC Pre-Sampler Working Principle and Impacts of the Interconnect Bandwidth

For sampling rates beyond 200 GS/s, heterogeneous integration of an InP or SiGe BiCMOS sampling front-end and CMOS ADCs is a viable solution [18], [28]. However, the interconnect bandwidth limitation between two separate chips poses challenges. The working principle of a CMOS ADC in conjunction with a 1–2 mode InP or SiGe sampling front-end is illustrated in Fig. 1. The analysis assumes that rank1 and rank2 are on separate chips. The low-pass filter (LPF) between rank1 and rank2 mimics a combination of the parasitic LPF, i.e., the 50-Ω output buffer in rank1 and the 50-Ω input buffer in rank2, and an additional reset-removing LPF for the current-mode sampler (optional), which is not generally required in integrated time-interleaved ADCs.

The continuous-time input signal $x_{\text{in}}(t)$ is buffered and then sampled by a 1–2 sampler at an overall sampling rate of F_s. The sampled output of the mth sub-sampling channel in time domain, $x_{\text{out},m}(t)$, and in frequency domain, $X_{\text{out},m}(f)$, can be expressed as [29]

$$x_{\text{out},m}(t) = x_{\text{in}}(t) \sum_{n=-\infty}^{+\infty} \delta\left(t - \text{nT}_{\text{clk}} - (m-1)\frac{T_{\text{clk}}}{2}\right), \quad m = 1, 2 \tag{1}$$

$$X_{\text{out},m}(f) = \frac{1}{T_{\text{clk}}} \sum_{k=-\infty}^{+\infty} X_{\text{in}}(f - \text{kf}_{\text{clk}}) e^{-\text{jk}(m-1)\pi} \tag{2}$$

where $T_{\text{clk}} = 1/f_{\text{clk}} = 2/F_s = 2T_s$ is the clock period of the sub-sampler. In Fig. 1(b), the spectra are plotted according to 2 at points A and B. Without the parasitic LPF, rank2 will see the same spectra at A and B, and the signals processed by rank2 are in discrete-time mode if rank2 is synchronized with rank1 for both phase and sampling rates ($F_{s,\text{rank2}} = F_{s,\text{rank1}}$).

In practice, the parasitic LPF filters the rank1 outputs. To not lose any frequency component from $X_{\text{in}}(f)$, the minimal required bandwidth of the parasitic LPF is $F_s/(2M)$, where M is the interleaving factor. In Fig. 1(b), we assume the parasitic LPF has the minimal required bandwidth of $F_s/4$ with a brick-wall roll-off. Following low-pass filtering of the rank1 output, the rank2 sub-ADCs only see signal spectra up to $F_s/4$. Each filtered output of rank1 sampler still contains all frequency components of $X_{\text{in}}(f)$, albeit with different phases assigned as illustrated in Fig. 1(b) at points C and D. In this case, the signals processed by rank2 are in continuous-time mode.

Assuming the rank2 sub-ADC has a sampling rate of $F_s/2$ and bandwidth of $F_s/4$, and ignoring the effect of quantization, the rank2 sub-ADC can be regarded as an ideal spectra buffer [C = E and D = F in Fig. 1(b)]. To reconstruct full-rate sampled data at F_s, we need to sample the sub-channel digital signals before multiplexing at $F_s/2$, which again leads to spectrum replicas ($k = -1, 0, 1$) as shown in Fig. 1(b) at point G. The unwanted images cancel each other. The bandwidth of

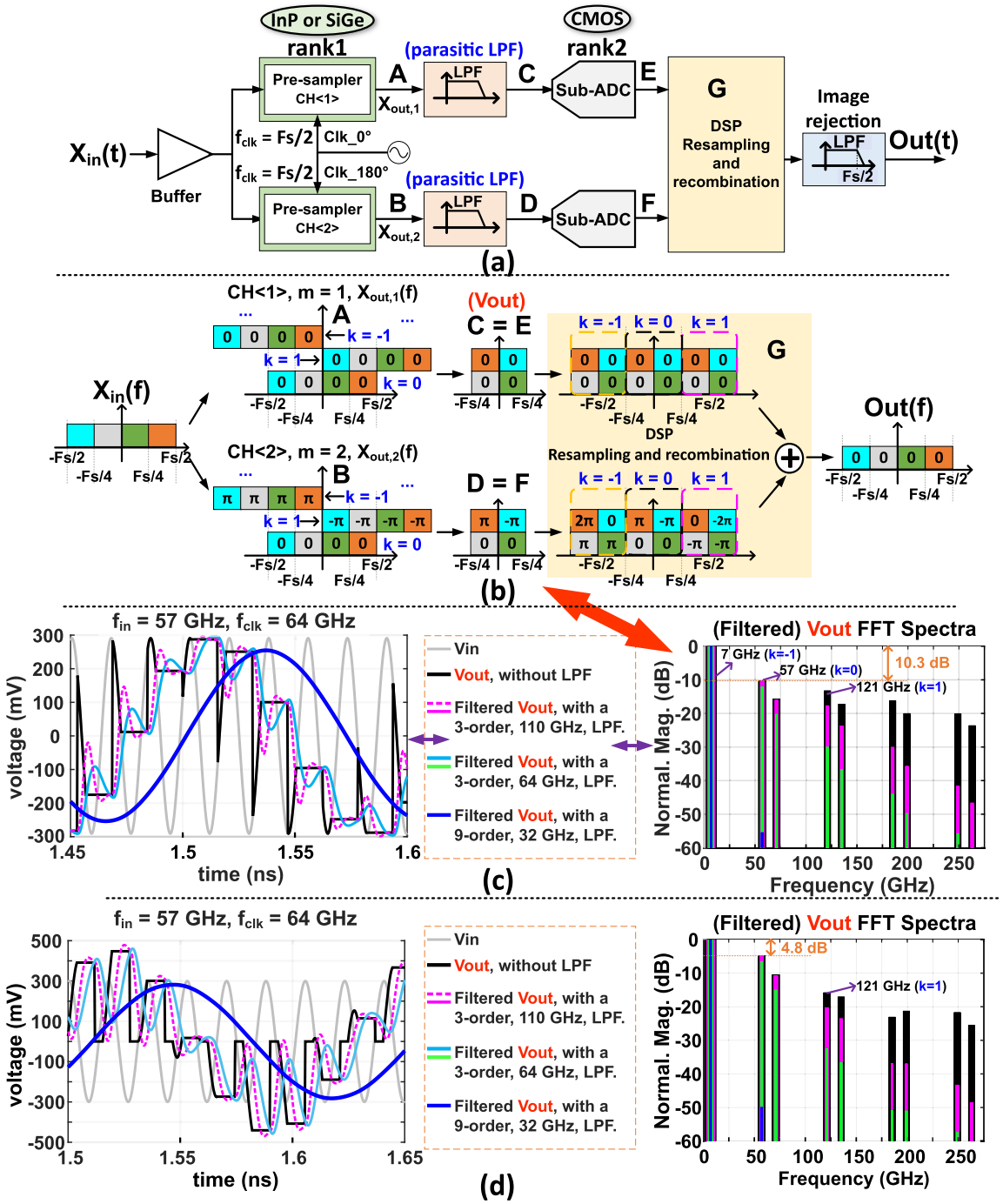

Fig. 1. (a) Heterogeneous ADC pre-sampler working principle and the impacts of the interconnect parasitic LPF. (b) Value in the rectangle represents the phase shift due to the time-interleaved sampling according to (2). Only $k = -1, 0, +1$th replicas are plotted. (c) and (d) Simulated ideal mathematical voltage-mode and current-mode sampler outputs filtered by different LPFs, respectively. For the voltage-mode sampler used in (c), $t_{\text{track}} = 0.25 * T_{\text{clk}}$ and $t_{\text{hold}} = 0.75 * T_{\text{clk}}$. For the current-mode sampler used in (d), $t_{\text{reset}} = 0.25 * T_{\text{clk}}$, $t_{\text{integration}} = 0.25 * T_{\text{clk}}$, $t_{\text{hold}} = 0.5 * T_{\text{clk}}$.

the parasitic LPF is generally higher than $F_s/4$ in practice, and all the replicated spectra delivered to rank2 will eventually be canceled for any bandwidth of the parasitic LPF.

The interconnect bandwidth between two chips can be a limiting factor, especially when rank1 is a current-mode sampler. Considering a hold duration of Δt_H and a parasitic LPF with a frequency response of $H_{\text{LPF}}(f)$, the spectrum of the low-pass filtered rank1 output is

$$X_{\text{LPFout},m}(f) = X_{\text{out},m}(f) \cdot \Delta t_H \text{sinc}(\pi \Delta t_H f) \cdot H_{\text{LPF}}(f). \quad (3)$$

Fig. 1(c) and (d) presents simulated examples of low-pass filtered rank1 outputs and their corresponding spectra, with voltage-mode and current-mode samplers, respectively. The three-order 64 and 110 GHz LPFs represent parasitic interconnect LPFs. To improve the hold phase delivered to rank2, more image terms must be kept in band, and a higher interconnect bandwidth is required. According to Fig. 1(b), to keep three terms in a 4-way interleaved, 256 GS/s, interconnect bandwidth should be larger than 96 GHz (requires spectra at $k = \pm 2$).

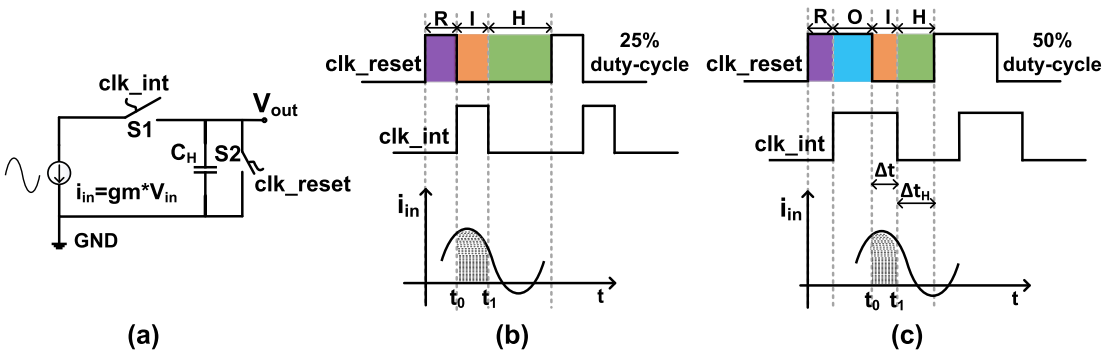

Fig. 2. (a) Simplified schematic of the current-mode sampler. (b) Timing diagram of a conventional current-mode sampler. (c) Proposed timing diagram.

If rank2 is synchronized with rank1 and samples at the correct time in the available acquire window (rank1 hold phase), the signals processed by rank2 are in discrete-time mode. With the presence of the parasitic LPF, the available acquire window decreases, and the synchronization requirements increase to minimize rank2 clock jitter and skew impact. The fastest synchronized time-interleaving sampling is achieved in the Keysight Infiniium UXR-Series 256 GS/s 110 GHz bandwidth oscilloscope, where a 256-GS/s 4-way time-interleaved pre-sampler (rank1) is synchronized with four 64 GS/s time-interleaved samplers (rank2) to provide aligned signals to sixteen 10-bit ADCs [18].

With the interconnect bandwidth decreasing further, and as demonstrated in Fig. 1(c) and (d), only the first Nyquist zone frequency components are left in band (LPF bandwidth = 32 GHz). In this case, the outputs of the LPF can be re-sampled by rank2 at an independent sampling rate from rank1 ($F_{s,\text{rank2}} \geq F_{s,\text{rank1}}$). For example, in Tektronix's DPO77002SX 200 GS/s, 70 GHz bandwidth asynchronous time-interleaving (ATI) real-time scope [28], the pre-sampler and sub-ADCs have a sampling rate of 150 and 200 GS/s, respectively. In this case, the combination of the sampler and the LPF resembles a mixer, and the signals processed by rank2 are in continuous-time mode.

Compared with the voltage-mode pre-sampler, the current-mode pre-sampler has less tolerance for a parasitic LPF because of its inherent reset operation and a shorter hold phase. When synchronization error or skew occurs, rank2 can accidentally sample in the reset phase, causing signal loss. If the interconnect bandwidth is insufficient to keep the hold phase, for example, in the case of the LPF with a bandwidth of 64 GHz in Fig. 1(d), rank2 must be carefully synchronized with rank1 to periodically resample the peak of the filtered output to maximize the gain and minimize the rank2 clock jitter and skew impact. On the other hand, if the reset phase is totally removed, rank2 does not need to be synchronized with rank1. However, the filters potentially introduce extra mismatches.

For the heterogeneous ADC pre-sampler, maximizing the interconnect bandwidth and keeping the hold phase is usually the target, though the required interconnect bandwidth increases with the sampling rate, which has become increasingly difficult as rank1 sub-sampling rates could exceed 50 GS/s for the next-generation ADCs. Regarding a current-mode pre-sampler, further removing the reset phase with an additional reset-removing LPF with a bandwidth of $F_s/(2M)$ between rank1 and rank2 is a possible solution to enhance the synchronization error tolerance. However, the mismatches among these LPFs, passband ripple, and especially the non-brick-wall roll-off of the additional LPF could complicate the digital signal processing (DSP).

III. Proposed Current-Mode Sampler

A. Proposed Single-Channel Current-Mode Sampler

Unlike the voltage sampler that takes the instantaneous value of the input signal at the clock's rising or falling edge, the current-mode sampler captures the average of the input signal in an integration time interval. Fig. 2(a) and (b) depicts the simplified schematic of the conventional current-mode sampler [13], [14], [26] using two phase-shifted but non-overlapping 25% duty-cycle clocks. It has three operations in each signal acquisition period: reset (R), integration (I), and hold (H). In contrast, this work proposes a current-mode sampler using two phase-shifted 50% duty-cycle clocks, as shown in Fig. 2(c) and in [30]. In the proposed solution, the reset clock clk_reset leads the current-steering clock clk_int by a portion of the clock period, and an extra operation called overlap (O) is introduced when both clocks are in high states. The signal acquisition is performed as follows.

- R) Switch S2 turns on while S1 stays off. The previous sampled information is removed by discharging the sampling capacitor C_H.
- O) S2 stays on, and S1 turns on. All the input signal current is conducted to the ground ideally.
- I) S1 remains on, but S2 switches off. The signal current is integrated onto the sampling capacitor C_H, from time t_0 to t_1.
- H) Both S1 and S2 are in the OFF-state. No charge can flow, and the output holds the sampled information.

During (I) phase, assuming an input signal current $i_{\text{in}}(t) = g_m \cos(2\pi f_{\text{in}} t)$ is integrated on the sampling capacitor C_H, we obtain for the sampled output voltage as

$$\begin{aligned} v_o(\text{nT}) &= \int_{t_0=\text{nT}+T_0}^{t_1=\text{nT}+T_1} \frac{1}{C_H} g_m \cos(2\pi f_{\text{in}} t)\,dt \\ &= \frac{g_m \Delta t}{C_H} \text{sinc}\left(2\pi f_{\text{in}} \frac{(t_1 - t_0)}{2}\right) \cos\left(2\pi f_{\text{in}} \frac{(t_0 + t_1)}{2}\right) \\ &= \frac{\Delta t}{C_H} \text{sinc}(\pi f_{\text{in}} \Delta t) \cdot i_{\text{in}}(t_m). \end{aligned} \tag{4}$$

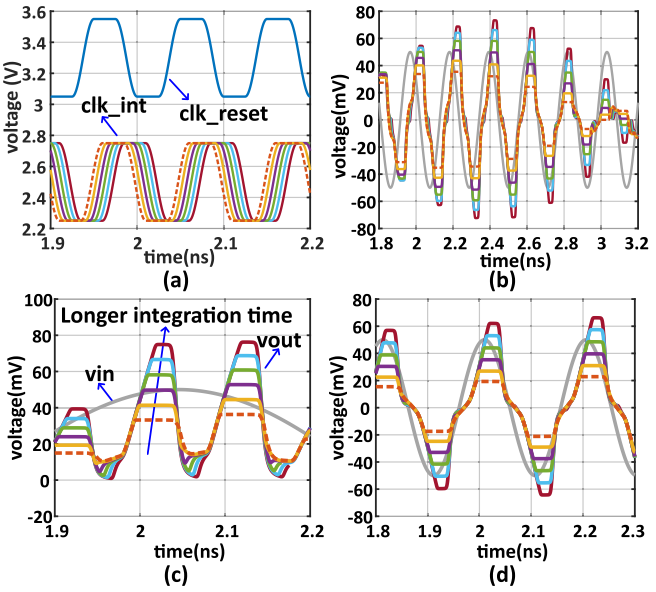

Fig. 3. Simulated example of the proposed solution with overlap time from $0.2 * T_{\text{clk}}$ to $0.45 * T_{\text{clk}}$ (step $= 0.05 * T_{\text{clk}}$) at 10 GS/s. (a) clk_reset and clk_int. (b) $F_{\text{in}} = 4.7$ GHz. (c) $F_{\text{in}} = 1.1$ GHz. (d) $F_{\text{in}} = 5.1$ GHz. Overlap time + integration time equal $0.5 * T_{\text{clk}}$. A shorter overlap time means a longer integration time.

Therefore, the current-mode sampler effectively samples at the middle of the integration phase, i.e., $t_m = (t_0 + t_1)/2$, with a sampler gain given by

$$\text{Gain} = \frac{\Delta t}{C_H}\text{sinc}(\pi f_{\text{in}}\Delta t). \tag{5}$$

This frequency-dependent gain has a -3-dB bandwidth [26]

$$\text{Bandwidth} = \frac{0.44}{\Delta t}. \tag{6}$$

Unlike the voltage sampler, the input signal tracking bandwidth of the current-mode sampler is determined by the equivalent integration time window length $\Delta t = t_1 - t_0$. As illustrated by (5) and (6), there exists a fundamental trade-off in current-mode samplers: a higher tracking bandwidth requires a shorter integration time, leading to a lower gain. In a typical case, as shown in Fig. 2, the proposed 50% clock scheme and conventional non-overlapping 25% clock schemes have a comparable integration time, resulting in similar bandwidth and gain.

B. Jitter and Hold Time Considerations

The proposed clock scheme can modify the overlap by simply delaying or advancing one of the two 50% duty-cycle clocks. This swaps the integration duration with the hold duration, introducing another degree of freedom in the design trade-off. As shown in Fig. 3, by varying the overlap portion of two clocks (hence the integration time window Δt), we can adjust the sampler gain as predicted by (5).

In a similar way, higher bandwidth than the conventional current-mode sampler can be achieved by reducing the integration time window Δt. However, a shorter integration window puts a stricter requirement on clock jitters. If a sinusoidal

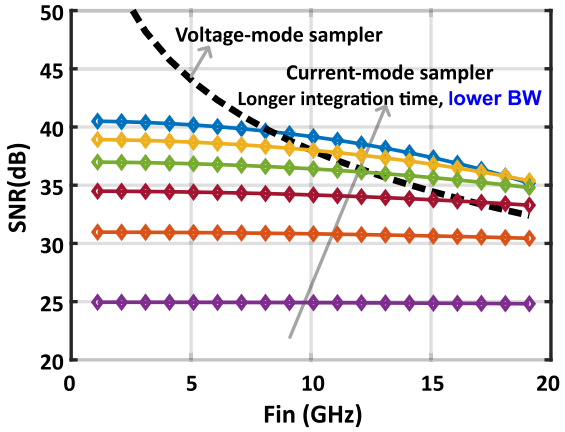

Fig. 4. Plot of jitter-induced SNR for clock overlap times from $0.2 * T_{\text{clk}}$ to $0.45 * T_{\text{clk}}$ (step $= 0.05 * T_{\text{clk}}$) at 10 GS/s with a rms clock jitter of 200 fs. A shorter overlap time means a longer integration time.

signal $i(t) = I_0 \sin(2\pi f_{\text{in}} t)$ is sampled by a current-mode sampler using C_H, the jitter error has a form of

$$e_j = \left(\frac{1}{C_H}\int i(t)\text{dt}\right)' \cdot t_j \tag{7}$$

where the charge-integration and derivative (i.e., estimate the slew rate of the changing signal) processes are canceled, resulting in a simpler form of $i(t) \cdot t_j / C_H$. Therefore, the rms error voltage caused by jitter $t_{j,\text{rms}}$ can be estimated as

$$e_{j,\text{rms}} = \frac{I_0}{\sqrt{2}}\frac{t_{j,\text{rms}}}{C_H}. \tag{8}$$

Assuming the same rms (but uncorrelated) jitter $t_{j,\text{rms}}$ at the rising and falling clock edges (see Fig. 2), the total rms error voltage due to clock jitter can be written as

$$V_{n,tj,\text{rms}} = \sqrt{e_{j0,\text{rms}}^2 + e_{j1,\text{rms}}^2} \tag{9}$$

$$= \frac{I_0 t_{j,\text{rms}}}{C_H}. \tag{10}$$

Based on the gain given in (5) and the rms input amplitude $I_0/(2)^{1/2}$, the sampled rms output is simply

$$V_{s,\text{rms}} = \frac{I_0}{\sqrt{2}}\frac{\Delta t}{C_H}\text{sinc}(\pi f_{\text{in}}\Delta t). \tag{11}$$

Therefore, the signal-to-noise ratio (SNR) of the current mode sampler output due to the clock jitter can be expressed as

$$\text{SNR}_{j,\text{CS}} = \frac{V_{s,\text{rms}}^2}{V_{n,tj,\text{rms}}^2} = \frac{\Delta t^2}{2t_{j,\text{rms}}^2}\underbrace{\text{sinc}^2(\pi f_{\text{in}}\Delta t)}_{\text{BW}=0.44/\Delta t} \tag{12}$$

which is a function of Δt. The SNR of the voltage mode sampler output due to the clock jitter is [29]

$$\text{SNR}_{j,\text{VS}} = \frac{V_{s,\text{rms}}^2}{V_{n,\text{tj,rms}}^2} = \frac{1}{\left(2\pi f_{\text{in}} t_{j,\text{rms}}\right)^2}. \tag{13}$$

Fig. 4 plots an example of the relationship between the jitter-induced SNR and the duration of the integration of the current-mode sampler, and compares it with the jitter-induced SNR of the voltage-mode sampler. A shorter overlapping time results in an extended integration phase, thereby enhancing

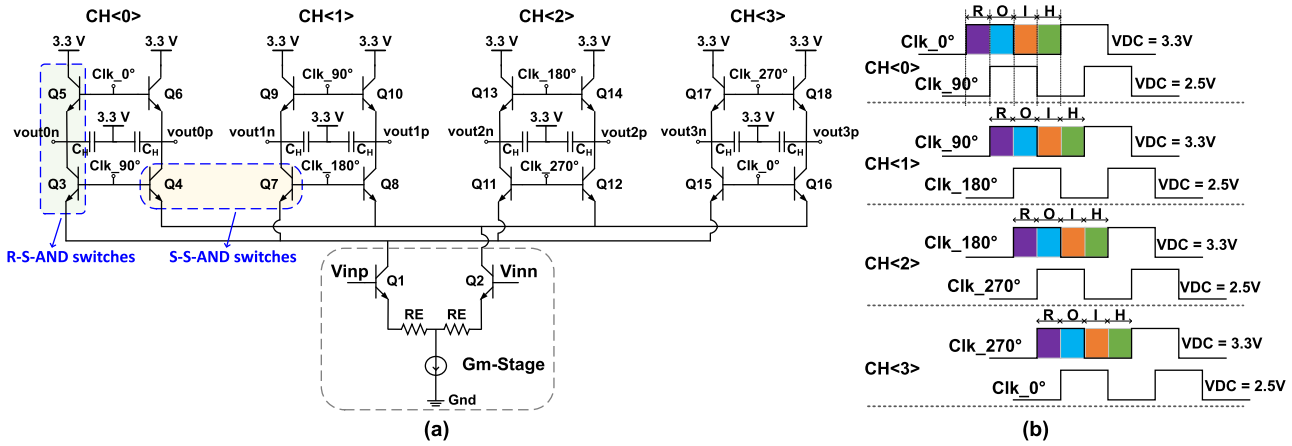

Fig. 5. (a) Proposed 1–4 current-mode sampler core circuit and (b) its timing diagram.

gain, SNR, and consequently improving jitter tolerance. But this is at the cost of decreasing input signal tracking bandwidth. Moreover, with shorter overlap times (longer integration time), the input frequency exerts a stronger influence on the jitter-induced SNR. This observation can be explained by recognizing that the degradation of signal strength with the input frequency [see (11)] increases as Δt increases. Overall, compared with the voltage-mode sampler, the gain, bandwidth, and jitter-induced SNR of the current-mode sampler all depend on the integration time, and they must be traded off.

Another important consideration regarding the new clock scheme pertains to the duration of the hold phase. Upon taking the Fourier transform of (4), we obtain the frequency representations of the sampled signal as

$$V_o(f) = \frac{\Delta t}{T_{\text{clk}} C_H} \sum_{k=-\infty}^{+\infty} I_{\text{in}}(f - kf_{\text{clk}}) \cdot \text{sinc}(\pi (f - kf_{\text{clk}}) \Delta t). \tag{14}$$

Considering a hold phase duration Δt_H, the overall spectra of the output signal become [26]

$$V_{o,h}(f) = V_o(f) \cdot \Delta t_H \text{sinc}(\pi \Delta t_H f). \tag{15}$$

In a typical scenario (as depicted in Fig. 2), the hold phase duration Δt_H reduced from traditional $0.5T_{\text{clk}}$ to $0.25T_{\text{clk}}$, resulting in a broader overall bandwidth according to (15). However, this alteration may pose challenges for the sub-ADC's sampler as a hold time allows for relaxing the jitter requirements for the subsequent samplers. By adjusting the clock overlapping as described earlier, it is possible to achieve a longer hold time duration ($0.5T_{\text{clk}} > \Delta t_H > 0.25T_{\text{clk}}$) and a higher sampler bandwidth. However, this comes at the cost of a lower sampler gain.

C. Proposed 1–4 Current-Mode Sampler With Bandwidth Insensitive to Clock Slew Rate

Fig. 5(a) and (b) demonstrates the proposed 1–4 current-mode sampler core circuit and its timing diagram. A similar sampler core circuit with a different timing scheme has been demonstrated in [14]. Taking the sub-sampling channel CH<0> as an example: Q_3 and Q_4 are the current-steering switches, corresponding to S1 in Fig. 2. Q_5 and Q_6 are implemented as the reset switches, corresponding to S2 in Fig. 2. The clocks driving the reset switches and current-steering switches have a common mode of 3.3 and 2.5 V, respectively. The input signal is first transformed from voltage mode into current mode by the linear transconductance stage (Gm-stage) in Fig. 5, and then it is alternatively steered to the four sub-sampling channels when their integration switches are in the ON-state. The four operations illustrated in Fig. 2 are consecutively performed in each sub-sampler.

As a key feature of the proposed solution, the tracking bandwidth of the 1–4 sampler is insensitive to clock slew rates [30]. The equivalent integrated current pulse per sub-sampler is shaped by two AND operations: 1) a reset-current-steering AND operation (R-S-AND) phase, i.e., the overlap of the reset and current steering clock in channel m, during which the signal current is discarded to the virtual ground during the O phase; and 2) a steering-steering AND (S-S-AND) phase, i.e., the partial overlap of the current steering clock of channel m with the current steering clocks of channel $m + 1$ and channel $m - 1$, resulting in input current sharing between sub-samplers. Taking the sub-sampling channel CH<0> as an example, Q_3 and Q_5 are the R-S-AND switches and the overlap of their ON-state forms the R-S-AND operation (O phase). While for the S-S-AND operation, taking CH<0> and CH<1> as an example, Q_4 and Q_7 are the S-S-AND switches and the overlap of their ON-state forms the S-S-AND operation. Fig. 6(a) demonstrates a simulated example using clocks with different slew rates, where only the R-S-AND operation exists. This is performed by removing all the odd sub-samplers (CH<1> and CH<3>) in Fig. 5 and no phase-overlapped current-steering switches exist. It shows that the overlap time decreases, and the equivalent integration time extends with the clocks' shape changing from square to full sinusoidal wave. Longer integration time results in higher gain but lower input tracking bandwidth.

Fig. 6(b) exhibits another simulated example to show the S-S-AND operation and illustrate how it varies with clocks having different slew rates. The simulations are conducted

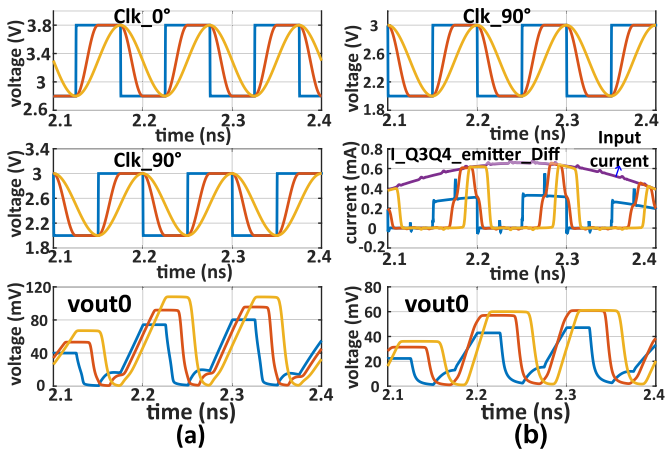

Fig. 6. (a) Simulated examples of sampler only with R-S-AND operation and (b) sampler with S-S-AND operation concerning variable clock slew rates. $f_{clk} = 10$ GHz, $F_{in} = 1$ GHz.

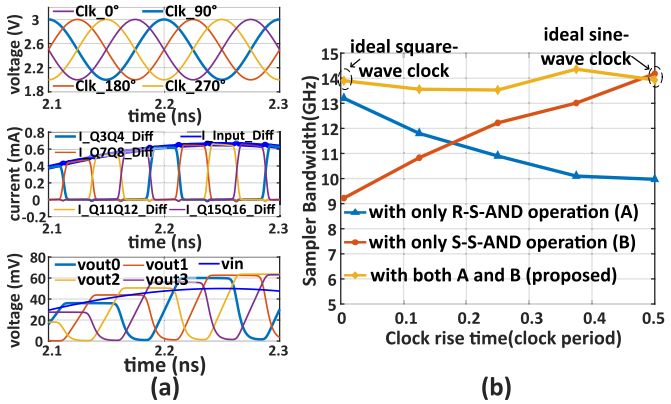

Fig. 7. (a) Simulated current pulses steered to each sub-sampler and the sampled outputs using sinusoidal clocks and (b) simulated example of sampler bandwidth concerning clock slew rates. $F_s = 40$ GS/s, $F_{in} = 1$ GHz.

using the full schematic and clocking scheme shown in Fig. 5. In this case, both the R-S-AND and S-S-AND operations exist. However, the S-S-AND (current steering) is performed before the R-S-AND operation, and the latter has no influence on the former operation. The middle sub-figure in Fig. 6(b) presents the current pulse steered to the sub-sampler with different clock slew rates, and it shows the current-steering clock strongly shapes the steered current pulse shape and hence the S-S-AND operation. The pulsewidth or the equivalent integration time reduces with the clocks changing from a square wave to a full sinusoidal wave, which is the opposite compared with the R-S-AND operation. Fig. 7(a) presents the current pulses steered to all four sub-samplers using sinusoidal shape clocks. Regardless of the small current-sharing intervals at the clock transition points, the S-S-AND operation makes the duty cycle of steered current pulses approximate 25% in Fig. 7(a).

With sinusoidal clocks, the current-steering switches turn on slowly, and their resistance gradually becomes low over time. As shown in Fig. 7(a), the signal current from the Gm-stage always sees one path with lower resistance than the other three because of the relative voltage difference between the current-steering clocks. Therefore, the current pulse steered to each

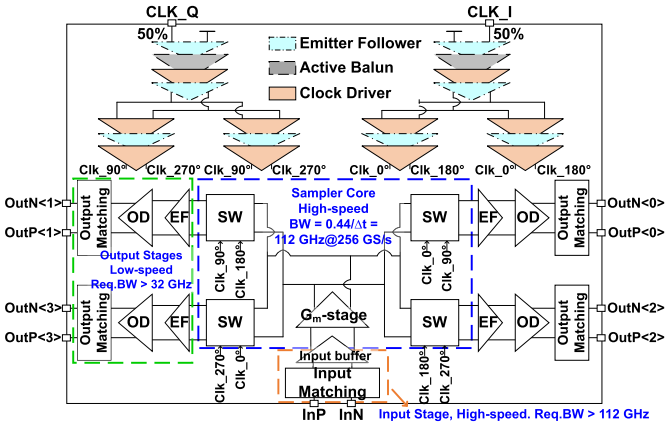

Fig. 8. Complete chip block diagram, with BW requirements indicated.

sub-sampler has a width of around a quarter of the clock period and an amplitude equal to the input signal current. Meanwhile, as shown in Fig. 6(a), with sinusoidal clocks, when the sub-sampler starts to receive signal current, the reset clock starts to fall from its peak, resulting in increasing resistance and less current being conducted on the virtual ground in the O-phase. Eventually, the integration time is a quarter of the clock period.

Fig. 7(b) shows the simulated samplers' bandwidth concerning clock slew rates. Combining both opposite effects brought by R-S-AND and S-S-AND operations in the proposed solution makes the equivalent integration time window per sub-sampler, and hence the sub-sampler bandwidth, independent of clock slew rate.

IV. Circuit Design

The complete block diagram of the chip is shown in Fig. 8. The data path consists of an input stage, a sampler core, and four output stages. The input stage comprises a broadband input-matching network and an input buffer. The sampler core is formed by a Gm-stage and four sampling switches (SW). According to Fig. 1, the input stage and the sampler core are high-speed blocks, requiring bandwidths of up to $F_s/2$, 128 GHz at 256 GS/s. In contrast, the output stages need bandwidths above $F_s/8$, 32 GHz at 256 GS/s. However, the achievable bandwidth of the sample core is limited by its integration time, which is 112 GHz at 256 GS/s. The clock distribution path converts the single-ended clock inputs to the final 50% duty-cycle quadrature clock outputs at 50, 56, and 64 GHz.

A. Input Stage

According to (6), the sampler core features a theoretical bandwidth of 88, 98.6, and 112 GHz at 200, 224, and 256 GS/s, respectively. Hence, the input stage should be designed with a 3-dB bandwidth above 112 GHz while maintaining a low peaking. However, as shown in Fig. 9, the capacitance originating from the RF pads, electrostatic discharging (ESD) diodes, and layout routing accumulates to 80 fF, limiting the achievable bandwidth to 40 GHz if there is no dedicated input matching network. The ESD

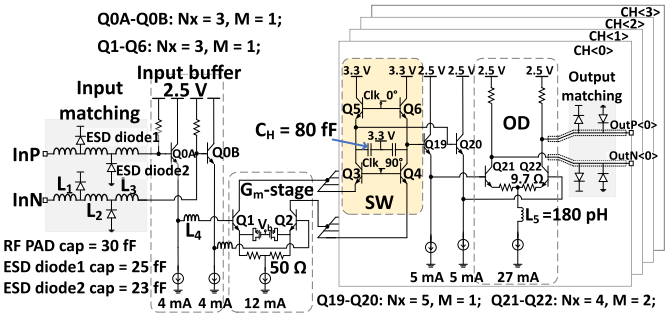

Fig. 9. Data path schematic. The emitter width and length are 70 and 900 nm for all bipolars. Nx is the number of bipolar in parallel in one transistor. M is the multiplier of the transistor.

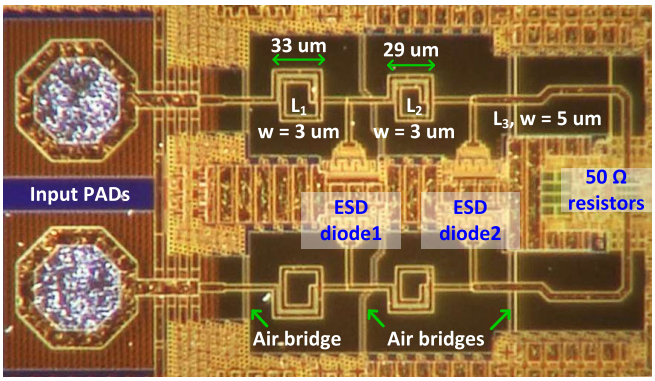

Fig. 10. Photograph of the input matching network from the die micrograph.

protection range is −3.4–3.4 kV for the human body model. A customized input matching network in this work was implemented as an artificial transmission line by distributing capacitance among high-Q inductors to reduce high-frequency signal return loss, Sdd11, and improve the bandwidth of the input stage as a result.

The chip was designed in a technology with six copper metal layers: four thin and two thick copper layers. All the input matching inductors were implemented using the top two thick copper layers (metal 5 and metal 6) with low sheet resistance to minimize the ohmic loss. Fig. 10 shows a photograph of the input matching network from the die micrograph. The vertical distance of inductors to the high-resistance substrate and the horizontal clearance of inductors to well-grounded surrounding ground planes are 8 and >20 μm, respectively, to minimize the high-frequency signal loss caused by the eddy current. L_1 and L_2 are implemented as square-shaped spiral inductors with only 1.5 turns to reduce the capacitance due to the overlaps between the spiral and the center-tap underpass and to alleviate the proximity effect [31], enhancing their self-resonance frequencies. L_3 has a low inductance and was designed as a straight line. Three air bridges using the lowest metal layer (metal first) were routed to connect the inductors' left and right side ground planes to reduce the impact of the parasitic slotline mode due to the asymmetry of the finite-ground planes [32], [33]. Fig. 11(a) and (b) presents the simulated inductance and Q-factor of L_1, L_2, and L_3. It shows the self-resonance frequencies of these inductors are all above 100 GHz.

The inductance of L_1, L_2 and L_3 was chosen considering the capacitance close to them to achieve a characteristic

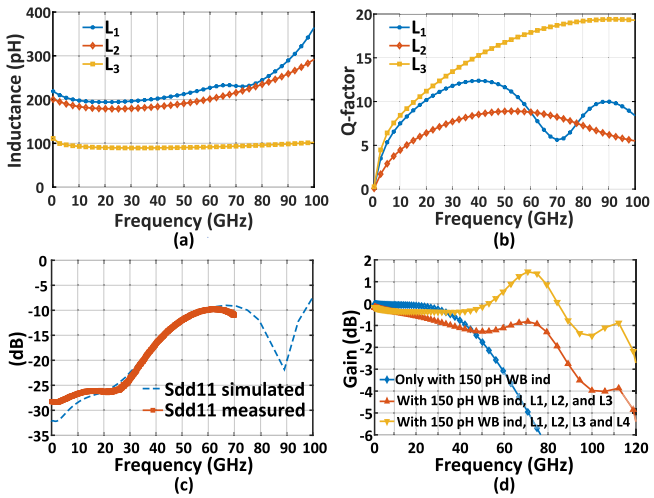

Fig. 11. (a) Electromagnetic simulated inductance and (b) Q-factor of L_1, L_2, and L_3. (c) Comparison of the measured (with probed data input, vector network analyzers (VNA) measurement) and the simulated differential input reflection, Sdd11. (d) Postlayout simulated input-stage transfer functions with different inductor configurations.

impedance of 50 Ω of the artificial transmission line. A parasitic capacitor with larger capacitance is always accommodated with an inductor with higher inductance. Fig. 11(c) compares the simulated and the measured differential input reflection, Sdd11. The measured Sdd11 agrees with the simulated result, and it stays below −9.7 dB for frequencies up to 70 GHz. Fig. 11(d) shows the simulated transfer functions of the input stage with a 150-pH OFF-chip wirebond (WB) inductor. The 3-dB bandwidth of the input stage is improved from 59 to 92 GHz by using L_1, L_2, and L_3. Another parasitic inductor from layout, L_4, between the input buffer and the Gm-stage with an inductance of 71 pH boosts the gain between 30 and 110 GHz and enhances the bandwidth beyond 110 GHz with a maximum peaking gain of 1.46 dB at 70 GHz.

B. Sampler Core

The sampler core was designed using the schematic and timing scheme shown in Fig. 5, targeting a sampling rate beyond 200 GS/s. In the current mode sampler, the single-ended and differential swings of the sampler core output are dominated by the capacitance of the sampling capacitor C_H. Fig. 12 presents a simulated example of the single-ended and differential outputs at 200 GS/s with varying sampling capacitance. As shown in Fig. 12(a), before every signal acquisition, the reset operation pulls up the single-ended outputs to a common mode voltage of 2.76 V. Then, the signal current from the Gm-stage pulls down the single-ended outputs in the integration phase. Integration is a linear operation, and the difference of the single-ended outputs at the end of the integration phase is linearly proportional to the input signal level. As defined in (5) and shown in Fig. 12(b), a smaller sampling capacitor results in a higher differential output swing and a higher single-ended output swing. A larger single-ended output swing means more emitter voltage drop of reset switches, i.e., Q_5 and Q_6 in Fig. 5. The more the emitter voltage drops, the more difficult it is for the reset switches

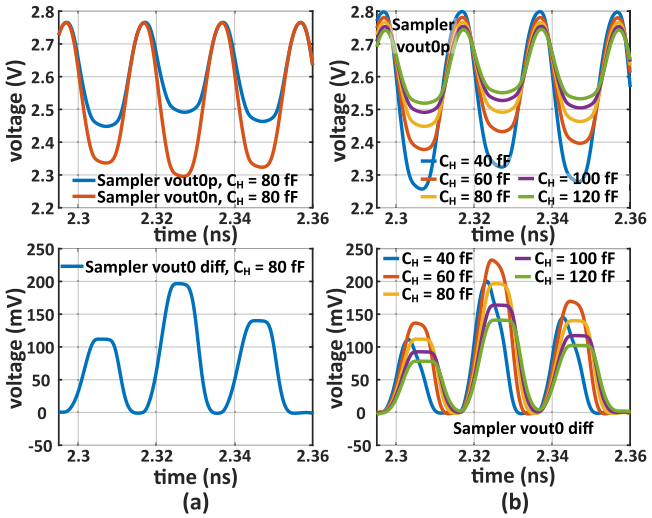

Fig. 12. Simulated sampler core single-ended output waveforms (top two figures) and differential output waveforms (bottom two figures) for $F_{\text{in}} = 7$ GHz, $f_{\text{clk}} = 50$ GHz, (a) with a C_H of 80 fF and (b) with a varying sampling capacitor C_H of CH<0>. The input signal swing is 500 mVppd. The quadrature clocks are ideal 50% duty-cycle sine-wave clocks with a swing of 600 mVppd.

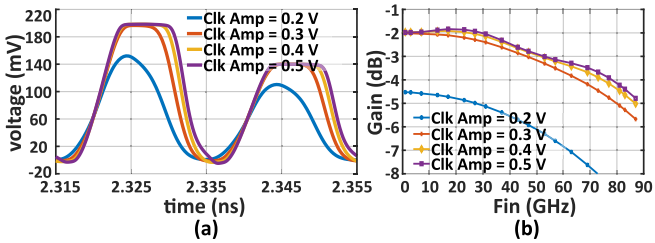

Fig. 13. (a) Simulated sampler core output waveform of sub-sampler CH<0> with $F_{\text{in}} = 7$ GHz at 50 GS/s and (b) transfer functions with different clock amplitudes at 200 GS/s ($f_{\text{clk}} = 50$ GHz). The input signal swings at all frequencies are 500 mVppd. The clock is fully sinusoidal.

to be in OFF-state in the hold phase and the earlier hold-to-reset mode transition for non-square-wave clocks. In addition, large single-ended (common mode) variations also stress the output stage. Therefore, a sampling capacitor with 80 fF capacitance was designed to balance the output swing, hold time, input-referred noise [26], and power consumption of the clock drivers and the output stages.

The swing of the clock should be large enough to ensure the four operations of the sub-sampler are being performed well. Otherwise, the sampler's gain, bandwidth, and hold time will be degraded. Fig. 13(a) shows an example of the simulated sampled output of CH<0> with varying clock swings. It shows that when the clock swing is too low, i.e., Clk Amp = 0.2 V, the hold time disappears because the reset switches Q_5 and Q_8 cannot be turned off in the hold phase. Fig. 13(b) presents the simulated sampler's transfer function regarding different clock swings. It shows a stronger clock results in a higher input signal tracking bandwidth, but the improvement gets smaller when the clock amplitude exceeds 0.3 V. However, a higher clock swing means a higher power consumption of the clock drivers. Eventually, considering the tracking bandwidth, hold time, and power consumption, the final clocks that directly drive the sampler were designed with an amplitude of 0.35 V at 50 GHz.

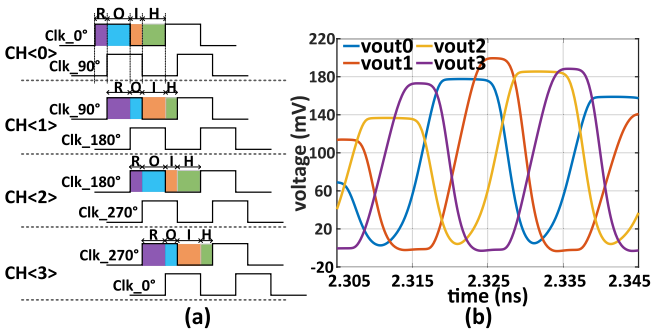

Fig. 14. (a) Timing diagram with a skew between I and Q clocks and (b) simulated sampler differential output waveforms with a 2-ps skew between clk_0° and clk_90° for $F_{\text{in}} = 7$ GHz, $F_s = 200$ GS/s. The input signal swing is 500 mVppd. The clocks are ideal 50% duty-cycle sine-wave clocks with a swing of 700 mVppd.

Timing mismatches among sub-samplers introduces interleaving spurs in the final recombined result, which can dominate the spurious-free dynamic range (SFDR) performance. One timing mismatch in the proposed timing scheme is the phase mismatch of the I and Q clocks. Fig. 14(a) exhibits an example of the timing sequence where the leading time of clk_0° is less than a quarter of the clock period. It shows that the timing mismatch between the I and Q clocks changes the shares of the operations in the sub-samplers. Ideally, the changes are the same in all even or odd channels, which means no mismatch between CH<0> and CH<2>, and no mismatch between CH<1> and CH<3> if there is only I and Q clock phase mismatch. This can be observed from the sampler outputs in Fig. 14(b), where there is a 2-ps skew between the clk_0° and clk_90°. By tuning the phase difference between the I and Q clocks, the gain, bandwidth, and hold time can be optimized in the two 180° phase-shifted sub-sampling channels when the sampler is used in a 1–2 mode. In a real data communication system, the sampler's input might have a small open eye, and the two 180° phase-shifted sub-samplers can be configured to observe (or sample) only the eye open range.

Nevertheless, due to the circuits' device mismatch, common-mode level, and swing differences of the clock buffers, there will be clock timing mismatches among all sub-samplers. These should be minimized, as they will introduce gain and bandwidth mismatches in the proposed solution.

C. Output Stage

The output stage includes a pair of pseudo-differential 5-mA output emitter followers (EFs), a 27-mA differential 50 Ω output driver (OD) with emitter degeneration resistors, and an output matching network implemented by splitting the ESD devices and RF pads in between the transmission lines, as shown in Fig. 9. The EFs and OD were designed to be capable of handling the single-ended and differential output swings of the sampler core as shown in Fig. 12. A 180-pH inductor, L_5, was implemented and connected in series with the tail current in the OD to improve the high-frequency common-mode rejection ratio (CMRR). According to Fig. 1, the output stage needs a 3-dB bandwidth of above $F_s/8$, 32 GHz

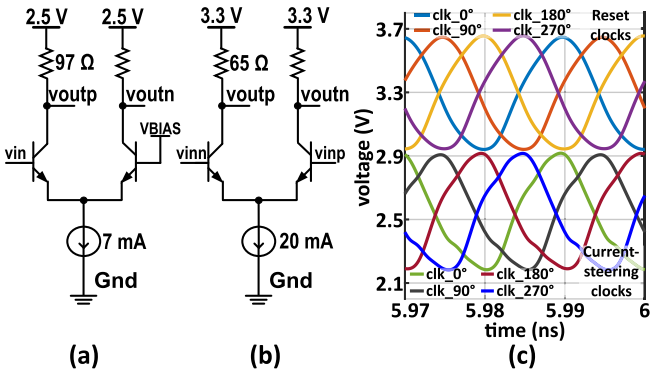

Fig. 15. (a) Schematics of the active balun, (b) last stage clock driver, and (c) simulated clock path output waveforms.

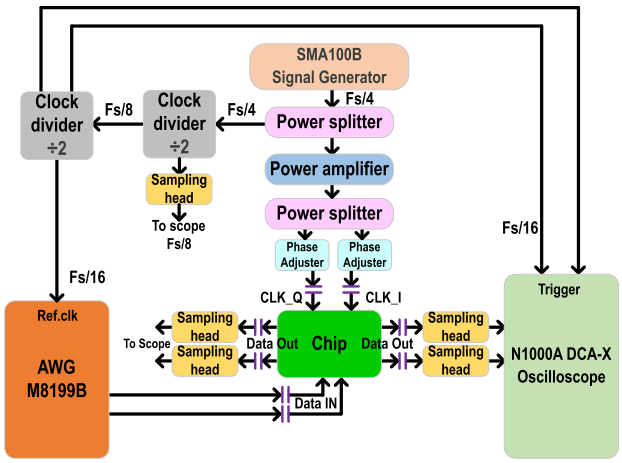

Fig. 16. Testbench schematic.

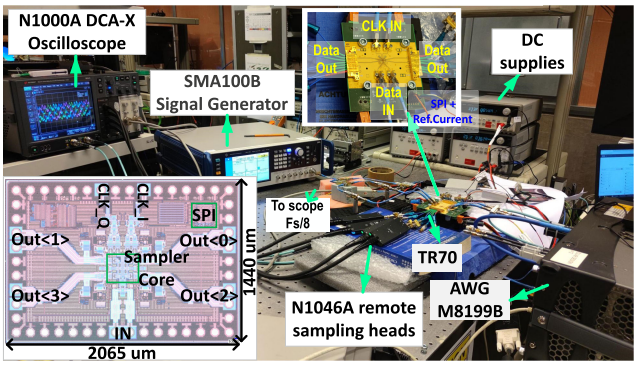

Fig. 17. Chip die micrograph and the measurement setup. In the measurements at 200 GS/s, an Anritsu MG3697C signal generator was used to provide the clock signal. While in the measurements at 224 and 256 GS/s, the signal generator was replaced by the SMA100B.

at 256 GS/s. To observe a high-quality demultiplexed eye, the output stage was finally designed with a 3-dB bandwidth of 48 GHz and a low-frequency gain of 4 dB.

D. Clock Path

The quadrature clock delivery path shown in Fig. 8 consists of active baluns and clock drivers. The active balun converts the single-ended 50% duty-cycle clock input to differential outputs. The following three-stage clock drivers continue to suppress the common mode difference between the 0° and 180° or 90° and 270° clocks. A 2.5-V supply powers the clock path except for the four last-stage clock drivers. The last stage clock driver determines the clock swing that is directly applied to the sampler core. It is designed as a differential amplifier powered by a 3.3-V supply with a single-ended output swing of 0.7 Vpp at 50 GHz. Fig. 15 shows the schematics of the active balun and the last stage clock driver and the simulated clock waveforms that are applied to the sampler core. The dc voltages of the final reset and current-steering clocks were biased at 3.3 and 2.5 V, respectively.

V. Measurement Results

Figs. 16 and 17 present the measurement setup and the die micrograph. The die measures 2.07 × 1.44 mm. The chip was first characterized with measurements using single-tone sinusoidal input signals to determine its frequency response and dynamic performances, i.e., SNR, signal-to-distortion ratio (SDR), SFDR, and signal-to-noise-and-distortion ratio (SNDR). Eventually, to mimic a real-world use case, the data input signal was replaced with large signals of PRBS-15 non-return-to-zero and pulse-amplitude-modulation-4-level (NRZ and PAM-4). During all measurements, the chips' low-speed serial peripheral interface (SPI) and dc pads were wirebonded onto a print circuit board (PCB). For the high-speed paths, in the measurements with sinusoidal inputs, the chip clock input, data input and outputs were wirebonded on high-speed transmission lines on a PCB. In contrast, in the NRZ/PAM-4 measurements at 200, 224, and 256 GS/s, the data input was probed with a 67-GHz RF GSSG probe, while the clock and data outputs were still wirebonded to high-speed transmission lines. The chip consumed 1.3, 1.1, and 1.1 W in measurements at 200, 224, and 256 GS/s, respectively.

Figs. 16 and 17 show the measurement setup. An M8199B Arbitrary Waveform Generator (AWG) generated the input signals for all measurements. The chip outputs were connected to the sampling oscilloscope via remote sampling heads. A signal generator, a power amplifier, and two phase adjusters provided the quadrature clocks with a swing of around 0.4 Vpp at 50, 56, and 64 GHz. The clock inputs, data input, and data outputs were ac coupled through external dc blocks.

A. Single-Tone Sinusoidal Signal Measurement

The loss from the cables, the connectors, and the PCB data input transmission lines was measured and de-embedded to characterize the chip performances. The PCB data output transmission line was not pre-calibrated, and it performed as a low-pass filter with a loss of 3 and 8 dB at 25 and 50 GHz, respectively. An input sine-wave from 1.1 to 67 GHz was applied with a calibrated swing of 500, 580, and 620 mVppd at 200, 224, and 256 GS/s, respectively. Because of the lack of sampling heads (requiring eight same sampling heads, but only four were available), during the measurements, the two 180° phase-shifted outputs, i.e., Out<0> and Out<2>, were measured and captured simultaneously, and then the other two 180° phase-shifted outputs were captured with everything else remained unchanged, just by swapping the sampling heads

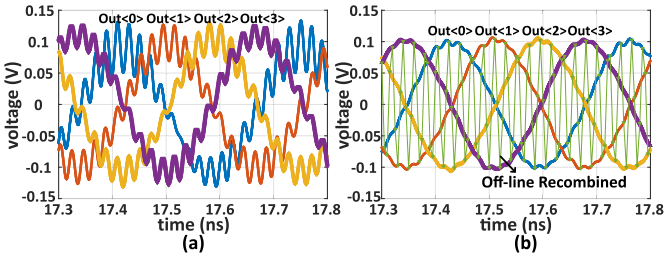

Fig. 18. (a) Measured chip output waveforms and (b) their low-pass filtered results for a 47-GHz 0.5-Vppd sinusoidal input at 200 GS/s.

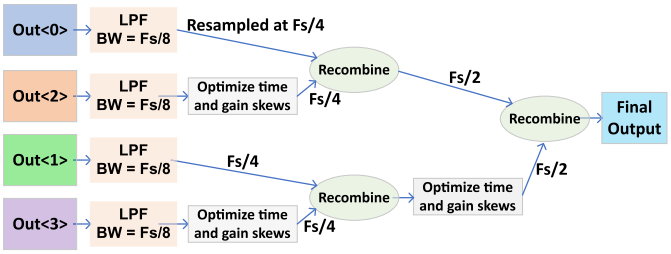

Fig. 19. Offline data recombination and calibration procedures. This calibration method is only intended to observe the chip performance.

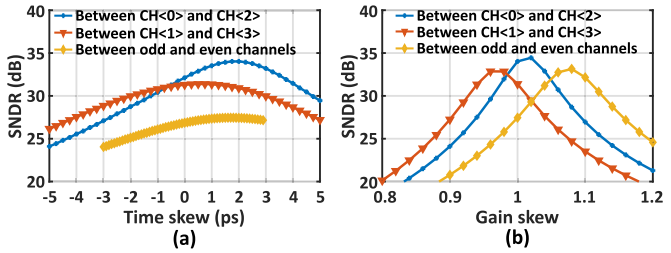

Fig. 20. (a) SNDR of the recombined results with varying time skew and (b) gain skew with $F_{in} = 47$ GHz at 200 GS/s.

between outputs. An auxiliary clock output from the first clock divider with a frequency of $F_s/8$ was used to monitor the clock and data alignment in these captured results.

The chip outputs were offline low-pass filtered and then recombined to observe the overall performance of the sampler. The LPF is a five-order Butterworth LPF with a bandwidth of $F_s/8$. Fig. 18 shows an example of the measured chip output waveforms and the low-pass filtered results with 47 GHz input sinusoidal signal at 200 GS/s. An offline calibration algorithm has been exploited to calibrate the dc offset, gain mismatch, and time skew originating from the sampler and PCB data output path. The calibration procedure is shown in Fig. 19. The re-sampling, calibration, and recombination aim to mimic the last step of the operation in Fig. 1, DSP, resampling, and recombination. It is performed by optimizing the delays and gains within a certain range to find a set of their values corresponding to the highest SNDR of the recombined result. The time and gain skews are defined as the optimized values minus/divided by the corresponding theoretical values. Fig. 20 shows an example of the optimized SNDR with varying delays and gains when combining the measured results of 47 GHz input sinusoidal signal at 200 GS/s. The optimized delays of Out<1>, Out<2> and Out<3> against Out<0> are 6.7, 12, and 17.2 ps, whereas their theoretical values are 5, 10, and 15 ps, respectively. Similarly, their optimized gains are 1.08, 1.02, and 1.04, corresponding to a difference of less than 0.8 dB compared with their theoretical unit gain. Fig. 21 shows the timing mismatch between the optimized and the ideal values at 200, 224, and 256 GS/s and for most frequency points, the delay mismatch stayed within $+/-2.5$ ps. However, it should be noted that one of the biggest contributors to the timing mismatch in Fig. 21 is the PCB output transmission line and cables connected to it (TR70, length = 75 mm, phase matching = $+/-2$ ps, [34]) and there were two different TR70s with the same standard used to capture the four outputs. It is also difficult to de-embed the phase mismatch of the two TR70s (eight separate cables) as the sampling heads must be reconnected to the TR70s for every frequency point measurement, resulting in a possible phase change of the TR70s.

Fig. 22 depicts the spectra of the offline recombined results with input frequencies of 47 at 200 GS/s, 29.1 GHz at 224 GS/s, 1.1 and 67 GHz at 256 GS/s. For the 47-GHz input at 200 GS/s, the highest harmonic is its third harmonic (HD3), located at 59 GHz. In contrast, for the 29.1-GHz input at 224 GS/s and 67.1 GHz at 256 GS/s, the highest harmonics are from their second harmonic (HD2), located at 109.8 and 121.8 GHz, respectively.

The measured chip frequency responses are represented by the fundamental tone amplitudes over frequencies and shown in Fig. 23(a) and (c). The recombined and de-embedded results in Fig. 23(a) and (c) show the chip achieves a 3-dB bandwidth beyond 67 GHz at 200, 224, and 256 GS/s. The measured transfer function at 200 GS/s is compared to the postlayout simulation results. The recombined and de-embedded transfer function indicates a 3-dB bump near 25 GHz at 200 GS/s, caused by the finite roll-off of the low-pass filter. Fig. 23(b) depicts the transfer function mismatch of Out<1>, Out<2> and Out<3> against Out<0> at 200 GS/s, and it shows the mismatches stay within 2 dB.

Fig. 24 presents the measured chip dynamic performances before recombination at 200 GS/s. The SNR of the four outputs is above 30 dB for most input frequency points. Regarding the linearity, the HD3 dominates the SDR of the non-recombined outputs. However, the SDR of the input signal source shown as the reference, AWG, limits the SDR of the sampler outputs for input frequencies around 25 GHz at 200 GS/s. The measured SNDR matches well with the SNDR of the input signal for the non-recombined results, but there is a clear difference compared with the simulated results for input frequencies between 10 and 40 GHz at 200 GS/s.

Fig. 25 shows the recombined results at 200, 224, and 256 GS/s. The SNDR of the recombined results records 30.3–34.1 dB, 27.8–30 dB, and 30–33 dB for frequencies from 1.1 to 17.1 GHz, 19.1 to 37.1, and 39.1 to 67 GHz, respectively, at 200 GS/s. This corresponds to an ENOBs of 4.3–5.4 bits. Fig. 25(b) and (c) shows the recombined results with and without calibration at 224 and 256 GS/s, respectively. At 224 Gs/s, the chip measured an SNDR of 25–36.3 dB, which equals an ENOB of 3.9–5.7 bits from 1.1 to 67.1 GHz. For 256 GS/s, the measured SNDR and the corresponding

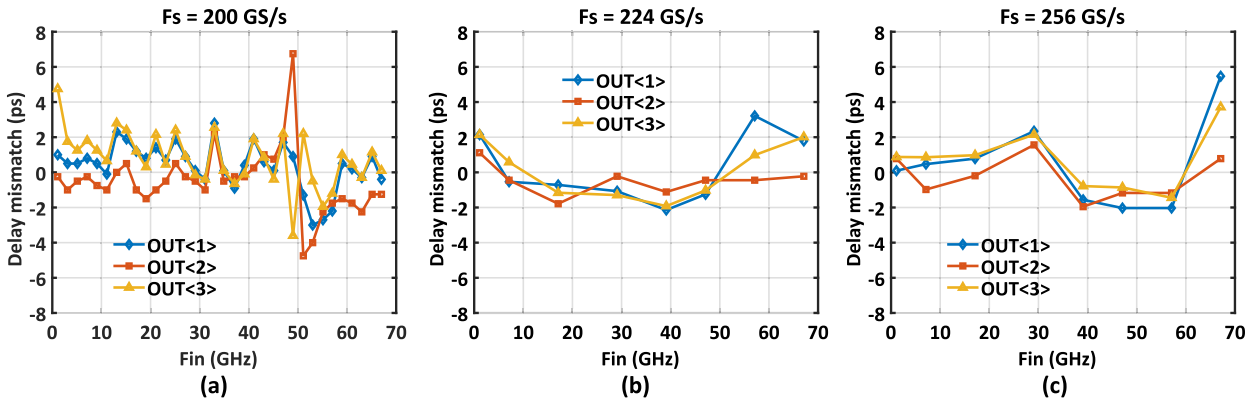

Fig. 21. Delay mismatch between the optimized values and the ideal values, including cable mismatch (+/−2 ps [34]), at (a) 200, (b) 224, and (c) 256 GS/s.

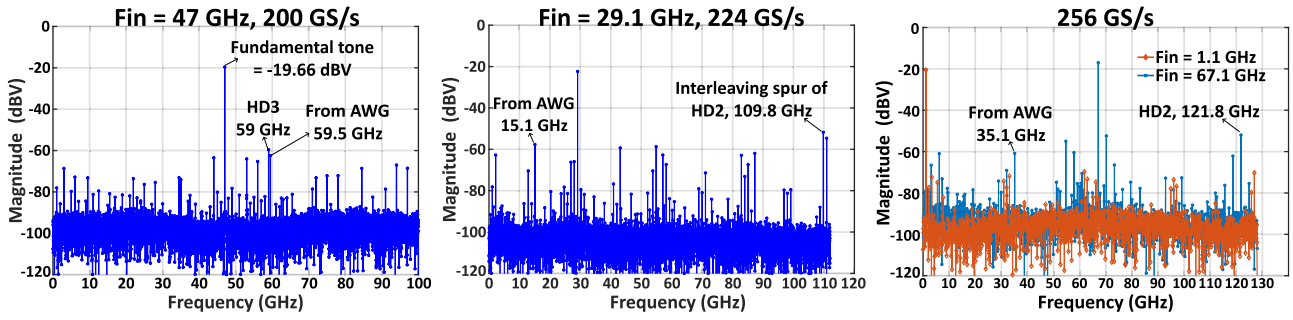

Fig. 22. Spectra of the offline recombined results with $F_{\text{in}} = 47$ GHz at 200 GS/s, $F_{\text{in}} = 29.1$ GHz at 224 Gs/s, and $F_{\text{in}} = 1.1$ GHz, 67.1 GHz at 256 GS/s. The power of the fundamental tone, noise, and harmonics is shown with their amplitudes in dB scale, where an amplitude = 0.1 V, equals −20 dBV.

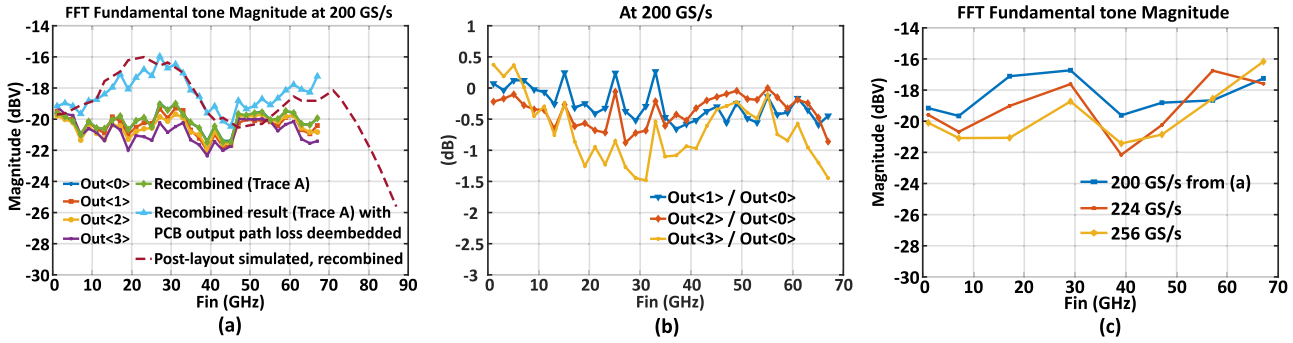

Fig. 23. Measured output waveform fundamental tone amplitude (from FFT spectra, i.e., Fig. 22) over frequencies at 200, 224, and 256 GS/s. (a) and (b) Measured results at 200 GS/s. (c) Presents the recombined and de-embedded results at 224 and 256 GS/s and they were compared with the results at 200 GS/s at the same input frequency points. In Fig. 22(a), the recombined (Trace A) curve is overlapped with the curve of Out<0>.

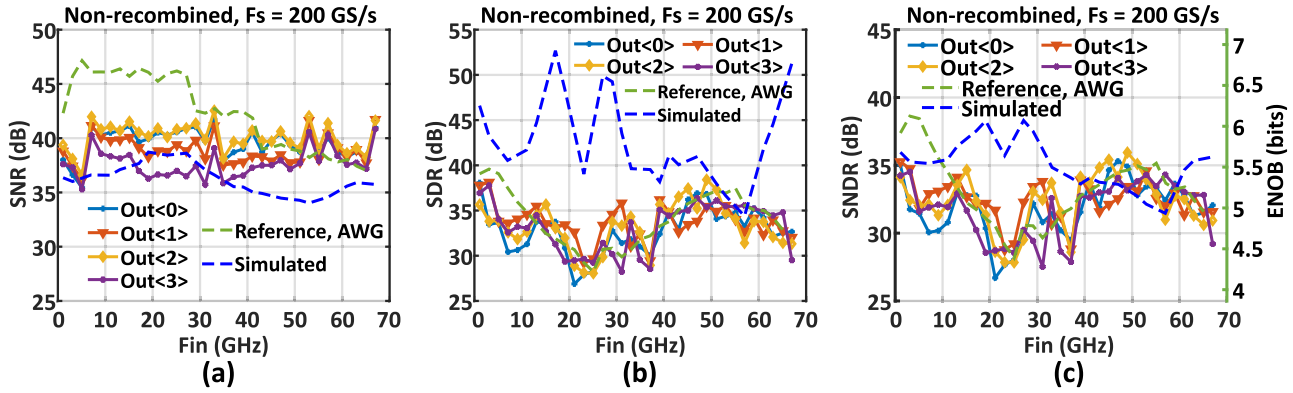

Fig. 24. Measured dynamic performances of non-recombined outputs with 500 mVppd input at 200 GS/s. (a) SNR, (b) SDR, and (c) SNDR.

ENOB amount to 22.3–39.2 dB and 3.4–6.2 bits, respectively. For the recombined results without any calibration, the SNDR stayed above 20 dB for most frequency points. Similar to 200 GS/s, the measured SNDR at 224 and 256 GS/s is still

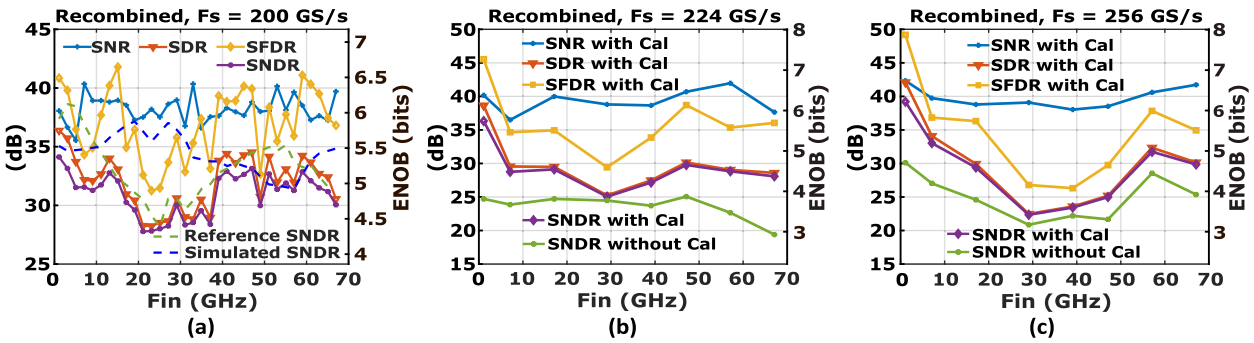

Fig. 25. Measured dynamic performances of recombined outputs with 500, 580, and 620 mVppd input at (a) 200, (b) 224, and (c) 256 GS/s, respectively.

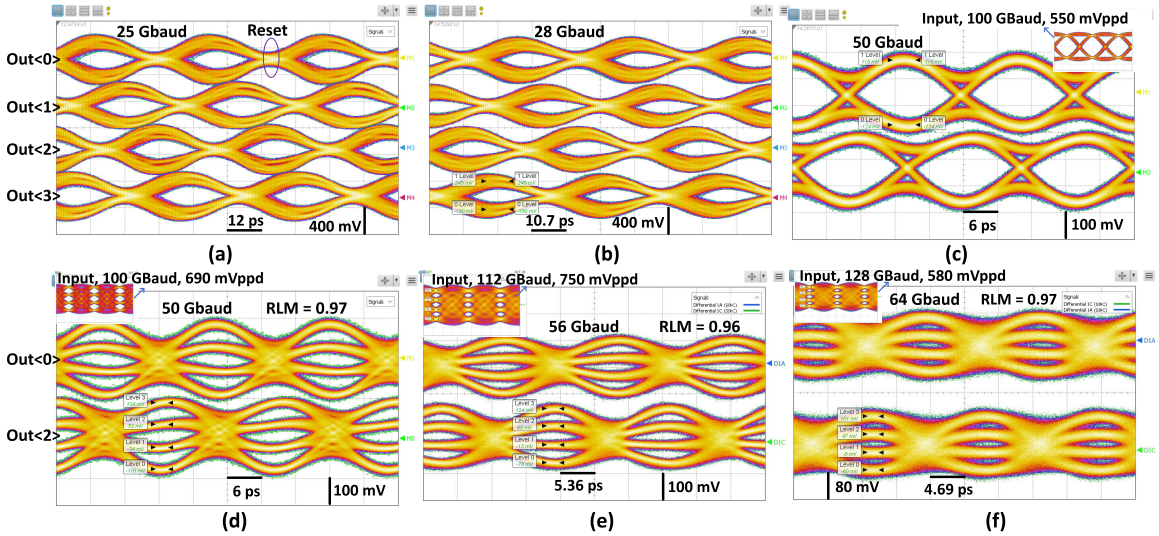

Fig. 26. Measured eye diagrams without post-processing at 100, 112, 200, 224, and 256 GS/s. (a) and (b) Measured in 1–4 mode using a fully wirebonded assembly. (c)–(f) Measured in 1–2 mode using an assembly with a probed data input (with a 67-GHz GSSG probe) and wirebonded outputs. (a) 100 Gbaud input at 100 GS/s. (b) 112 Gbaud input, at 112 GS/s. (c) and (d) 100 Gbaud inputs at 200 GS/s. (e) 112 Gbaud input at 224 GS/s. (f) 128 Gbaud input at 256 GS/s.

limited by the signal applied to the chip, which is shown as the reference SNDR in Fig. 25(a).

B. NRZ/PAM-4 Measurement

The analog demultiplexing functionality of the sampling front-end is shown in Fig. 26 with PRBS-15 NRZ/PAM-4 measurements in 1–4 and 1–2 modes at F_s from 100 to 256 GS/s. In the 1–4 mode, the clock and the input data were aligned with 1 UI delay between sub-samplers to ensure all four sub-samplers sampled the correct input eyes and the outputs were quarter-rate eye diagrams. While working in 1–2 mode, two 180° phase-shifted sub-sampling channels are aligned with the input data, resulting in two half-rate output eye diagrams, while the other two channels capture the input signal crossings. The eye diagrams shown in Fig. 26 are results without DSP, equalization, or calibration. The loss from the data input probe [see Fig. 26(c)–(f)] was not pre-calibrated, and the real eyes applied to the chip are relatively closed compared with the eyes shown as the inputs, especially for the measurement with 128 Gbaud input at 256 GS/s.

C. Performance Comparison

Table I summarizes the performances of the sampling front-end and compares it against the published works. The

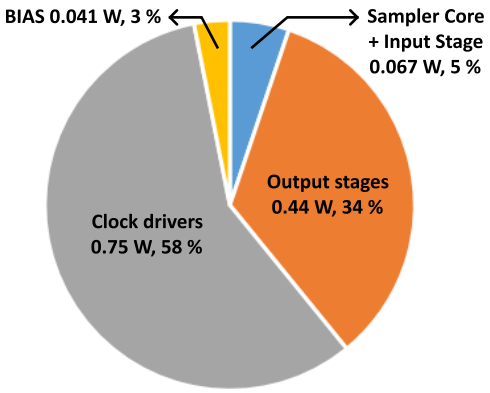

Fig. 27. Chip power breakdown working at 200 GS/s. The power consumption of the clock drivers was optimized to 0.55 W at 224 and 256 GS/s.

chip achieved the highest sampling rate, the highest measured 3-dB analog input bandwidth, and recorded over 30 dB SNDR of the final recombined results for frequencies from 39 to 67 GHz at 200 GS/s. The chip is the first to demonstrate both non-combined and re-combined results to fully characterize a time-interleaved sampler. It also demonstrates a high power efficiency, the best among all implementations having four output 50 Ω drivers for 1–4 analog demultiplexing

TABLE I
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART SAMPLING FRONT-ENDS

	This work			[14] JSSC'2021	[15] JSSC'2022	
Sampling mode	**Current-mode**			Current-mode	Voltage-mode	
F_s **(GS/s)**	**4 x 50 = 200**	**4 x 56 = 224**	**4 x 64 = 256**	4 x 32 = 128	4 x 32 = 128	4 x 50 = 200
Analog input Bandwidth	**>67**	**>67**	**>67**	36	57	20
Output power (dBm) **@Diff Zout = 100 Ω**	**-12.2 @ 1.1 GHz Input=0.5 Vppd**	**-12.6 @ 1.1 GHz Input=0.58 Vppd**	**-13.1 @ 1.1 GHz Input=0.62 Vppd**	-15 @ 14 GHz Input=0.5 Vppd	-17.8 @ 1 GHz Input=0.5 Vppd	-16 @ 1 GHz Input=0.5 Vppd
SNR or SNDR (dB) **@** F_{in} **(GHz)** **Non-Recombined**	**35 @ 1.1 34 @ 47 31.6 @ 67 , SNDR**	**37.9 @ 1.1 29.9 @ 47.1 28.7 @ 67.1 , SNDR**	**40.6 @ 1.1 26.9 @ 47.1 29.9 @ 67.1 , SNDR**	28 @ 2 22 @ 50 , SNDR	20 @ 1 10 @ 53 , SNR	<10 @ 1 <0 @ 20 , SNR
SNDR (dB) **@** F_{in} **(GHz)** **Recombined**	**34.1 @ 1.1 33.2 @ 47 30 @ 67**	**36.3 @ 1.1 29.8 @ 47.1 28.1 @ 67.1**	**39.2 @ 1.1 25 @ 47.1 29.9 @ 67.1**	N.A.	N.A.	N.A.
SFDR (dB) **@** F_{in} **(GHz)** **Recombined**	**41 @ 1.1 40 @ 47 36.8 @ 67**	**45.5 @ 1.1 38.7 @ 47.1 36.1 @ 67.1**	**49.2 @ 1.1 29.8 @ 47.1 34.9 @ 67.1**	N.A.	N.A.	N.A.
Bit rate (Gb/s)	**200**	**224**	**256**	$N.A.^a$	N.A.	N.A.
Power supply (V)	**3.3/2.5**			4.6/3.3	4.85	
Power consumption (W)	**1.3**	**1.1**	**1.1**	3.6	3.5	
Efficiency (pJ/sample)	**6.5**	**4.9**	**4.3**	28.1	27.3	17.5
Technology f_T/f_{MAX} **(GHz)**	**130-nm SiGe BiCMOS 350/450**			90-nm SiGe BiCMOS 300/480	90-nm SiGe BiCMOS 300/480	

[*] *a, Only eye-diagrams with off-line DSP.*

usages [14], [15]. Fig. 27 summarizes the power breakdown of the complete chip. The current-mode logic (CML)-based clock drivers consume more than 50% of the total power. This is also the first published demonstration of analog demultiplexing functionality on 100, 112, and 128 Gbaud NRZ/PAM-4 input at 200, 224, and 256 GS/s without DSP, respectively.

VI. CONCLUSION

This article presents a 1–4 time-interleaved current-mode sampler operating at a sampling rate of up to 256 GS/s, the highest in silicon-based samplers. Because of the proposed clock strategy, the analog input signal tracking bandwidth of the sampler is insensitive to the clock slew rate. Targeting a high input bandwidth, the chip was implemented with a broadband input matching network with a measured return loss lower than -9.7 dB for frequencies up to 70 GHz. The chip measured an input signal tracking bandwidth beyond 67 GHz and an SNDR of more than 27.8, 25, and 22.3 dB for frequencies from 1.1 to 67 GHz of the final offline recombined results at 200, 224, and 256 GS/s. Thanks to the use of only 50% duty-cycle clocks, the complete chip consumes a power consumption of 1.1 W, resulting in a power efficiency of 4.3 pJ/sample at 256 GS/s. In the NRZ/PAM-4 measurement, the chip demultiplexed the high-speed input to quarter-rate or half-rate outputs, best among the SiGe 1–4 samplers. This article reports a sampler that achieved the best SNDR, the highest input bandwidth, and the best power efficiency among the reported 1–4 samplers with four outputs at up to 256 GS/s.

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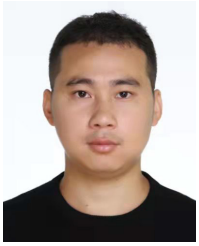

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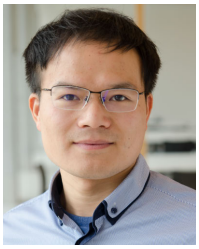

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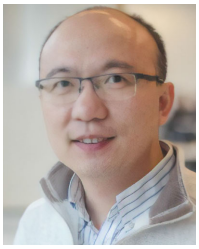

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