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Reliability of high-performance monolayer MoS_2 transistors on scaled high-κ HfO_2

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The successful integration of ultrathin high-κ insulators is essential for the advancement of ultra-scaled field-effect transistors (FETs) based on two-dimensional (2D) semiconductors in future technology nodes. However, defects within the high-κ stack or at the interfaces can significantly degrade the performance of these "interface-only" devices, raising questions regarding their long-term reliability. Here, we study the reliability of monolayer MoS_2 FETs on ultra-thin high-κ HfO_2. Interestingly, we observe a two-stage threshold voltage shift (ΔV_{TH}) under positive bias temperature stress (PBTS) and hot carrier degradation (HCD). This two-stage ΔV_{TH} is absent in devices fabricated on exfoliated hBN, suggesting that the donor state generation (negative ΔV_{TH}) is induced by atomic-layer-deposition (ALD) processes in HfO_2-based devices. Elastic Recoil Detection Analysis (ERDA) indicates that hydrogen, likely from the ALD precursor, is a probable cause, highlighting the need for ALD process refinement to improve 2D FET stability for CMOS compatibility.

Two-dimensional semiconducting transition metal dichalcogenides (2D TMDs) have emerged as promising materials for next-generation ultra-scaled FETs. Unlike silicon, these 2D semiconductors possess sizable bandgap and exhibit decent carrier mobility even at layer thicknesses below 1 nm[1,2]. Their inherently atomic thickness ensures excellent electrostatic control over the channel potential, effectively reducing short-channel effects (SCEs) and allowing for further scaling of the channel length below 5 nm[2,3]. Additionally, the formation of 2D van der Waals (vdWs) heterostructures through vdW forces introduces the possibility of monolithic 3D integration with low-thermal budget[4]. This unique property facilitates the integration of different materials, paving the way for the integration of multifunctional devices on a single chip, including photonic and memory units, without the constraints of lattice matching[4–9].

While significant advancements have been achieved in both n-type[10–13] and p-type[14–17] TMDs, leading to high-performance FETs with current densities in the hundreds of μA/μm at scaled biases, several unresolved questions about how to achieve optimal overall performance of TMD transistors remain. Many of these questions arise from these devices being "interface-only" transistors, thus exhibiting an increased sensitivity to their interface and oxide traps, and defects created during fabrication[2,12,18–21]. One crucial question is: "Can these 2D transistors offer the necessary stability and reliability for Front-End-of-Line (FEOL) and Back-End-of-Line (BEOL) logic applications?" Notably, the stability of current 2D FETs significantly lags behind their silicon-based counterparts, often by two orders of magnitude[19,20,22–25]. There are two primary strategies to address the reliability challenges in 2D FETs: Firstly, by employing less defective, crystalline insulators that form a (quasi) van der Waals interface with the 2D semiconductor channel; Secondly, by deliberately selecting gate oxide stacks that have defect bands isolated from the Fermi window of the semiconductor channel[19,25].

However, the first strategy, e.g., using crystalline hBN as a gate insulator, has several technological challenges. Current state-of-the-art crystalline hBN is unsuitable for use as a scaled gate insulator because of its small dielectric constant. Additionally, hBN can be grown only at temperatures above 1200 °C. Direct growth of hBN on 2D TMDs is even more challenging. Beyond the pursuit of a new high-κ crystalline insulator material compatible with low-thermal budget processing, a more viable solution is the integration of atomic layer deposition (ALD) of ultra-thin high-k oxides in 2D FETs and the selection of the most favorably matched 2D channel/3D oxide interface[19,25]. Yet, most reliability studies have been centered on technologically less relevant low-κ and thick dielectrics (EOT > 30 nm), e.g. by using substrate SiO_2 as the gate oxide[19,20,22–25].

In this Article, we systematically study the reliability of 2D monolayer (1 L) MoS_2 FETs with ultra-thin ALD HfO_2 (6 nm) and compare the degradation mechanism with exfoliated h-BN (12 nm) gate dielectrics. Our findings reveal a two-stage threshold voltage shift in the HfO_2 dielectric scenario. We attribute this anomalous threshold voltage shift to the presence of hydrogen-assisted donor traps in 2D semiconductors on scaled high-κ

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HfO_2 (*EOT* ~ 1.5 nm). Our findings indicate that the ALD process must be optimized to improve the reliability of 2D transistors, especially eliminating hydrogen-related defect generation or other possible residuals in the ALD gate dielectric.

Results

Gate stack requirements for high-performance 2D scaled FETs

A comparison between amorphous HfO_2 and crystalline hBN dielectric for scaled FETs is illustrated in Fig. 1a. Identifying the optimal insulator for 2D materials necessitates a comprehensive understanding of the gate stack requirements for high-performance scaled FETs. These requirements include low gate leakage current, an equivalent oxide thickness (*EOT*) of less than 1 nm, a low interface trap density (D_{it}) of less than 10^{11} $cm^{-2}eV^{-1}$ (SS < 70 mV/dec), a low active oxide trap density (D_{ot}) of less than 10^{18} $cm^{-3}eV^{-1}$, high breakdown voltage, and manufacturing compatibility[12,19,20,26]. Interface traps (D_{it}), which typically have fast trapping/de-trapping rates, can degrade not only *SS* but also mobility and leakage current due to impurity scattering and trap-assisted tunneling. Typically, these interface traps can be either donor or acceptor-like, determined by their thermodynamic trap level position with respect to the Fermi level, as shown in Fig. 1a. In contrast, border traps (D_{ot}) in the gate oxide close to the channel determine the long-term stability and reliability of FETs[19,20,25]. Similar to interface traps, the border traps in the oxide can be either donor or acceptor-like, as shown in Fig. 1a. These border traps are energetically aligned within distinct defect bands that are broader in amorphous oxides such as SiO_2 and HfO_2 but are more discretely distributed in degenerate energy levels in crystalline insulators. For example, in hexagonal boron nitride (hBN), the overall density of border traps is significantly reduced. As a result, TMD devices on hBN are expected to outperform those on HfO_2 gate dielectrics in terms of reliability. To uncover the reliability physics of devices on ALD ultra-thin HfO_2 (6 nm) gate dielectrics, we fabricated 2D 1L-MoS_2 FETs and employed various electrical characterization methods to understand degradation mechanisms. Detailed fabrication and electrical characterization are provided in Methods.

Supplementary Fig. 1 outlines the fabrication process of 1L-MoS_2 n-type FETs. Figure 1b depicts a schematic and an SEM image of a device, respectively. A representative 1L- MoS_2 FET, with an *EOT* of approximately

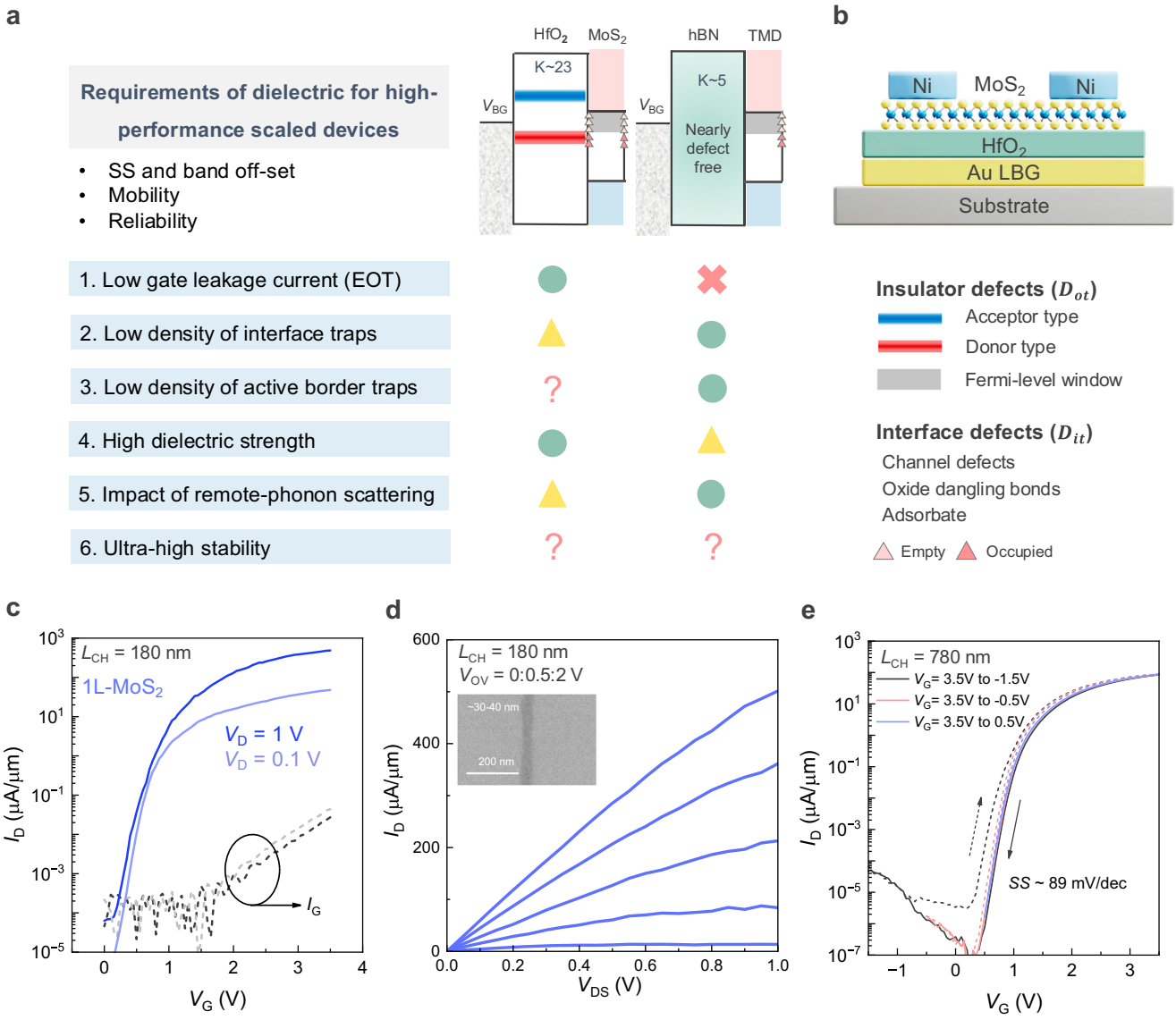

Fig. 1 | Gate stack requirements for high-performance 2D scaled FETs. **a** Comparison between high-κ HfO_2 and crystalline hBN dielectric for scaled FETs. **b** Schematics of a 1L-MoS_2 FET on high-κ HfO_2. **c** I_D-V_G, and **d** I_D-V_D of 1L-MoS_2 FETs on high-κ HfO_2 with W_{CH} of 30 nm and L_{CH} of 180 nm. The inset is a scanning electron microscopy (SEM) image of nanoribbon 1L-MoS_2 material after patterning. **e** Hysteresis characterization of a long-channel device (L_{CH} = 780 nm) on high-κ HfO_2 across varying V_G sweep ranges.

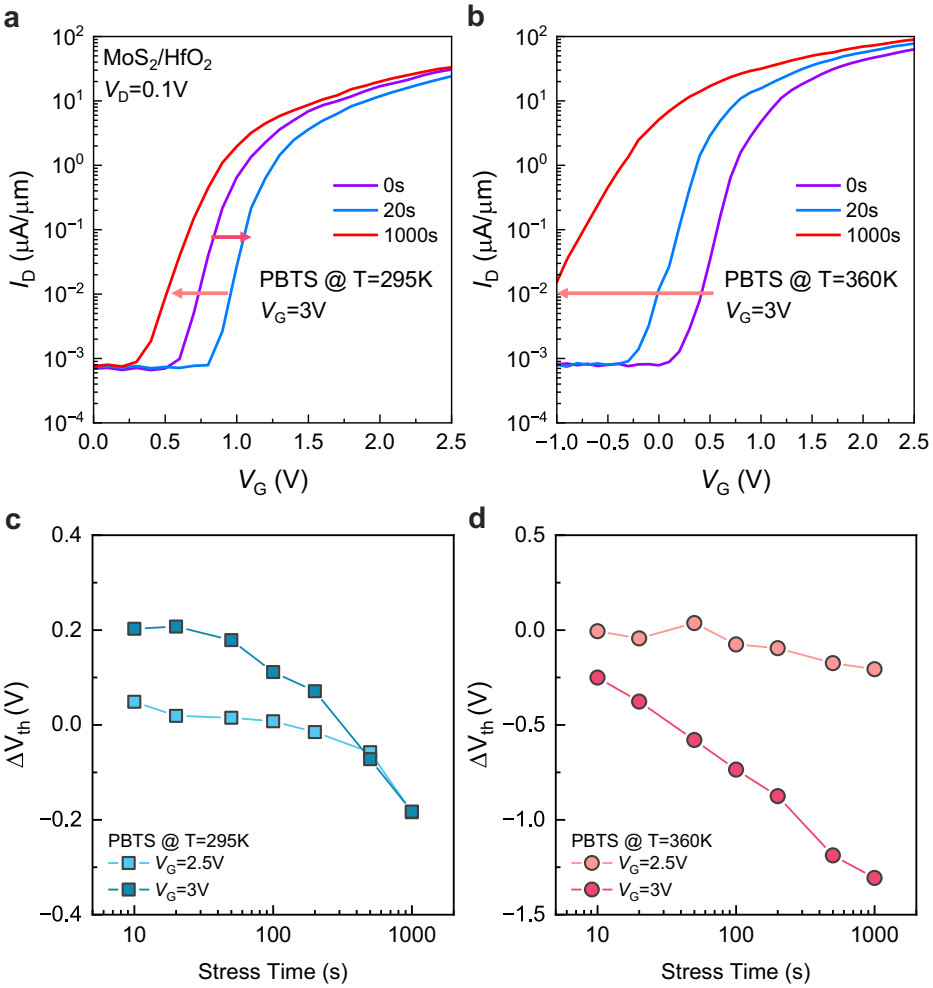

Fig. 2 | Positive bias temperature stress (PBTS). Evolution of I_D-V_G characteristics under gate bias stress of 1L-MoS_2 LBG FETs under PBTS condition (V_G = 3 V) from 0 s to 1000 s at **a** room temperature 295 K and **b** elevated temperature 360 K. ΔV_{TH} (t) for various PBTS conditions at **c** 295 K and **d** 360 K.

1.5 nm, a channel length (L_{CH}) of 180 nm, and a channel width (W_{CH}) of 30 nm, achieved a high on-current of approximately I_{ON} = 485 μA/μm at V_D = 1 V and V_{OV} = 2 V, as illustrated in Fig. 1c, d. This remarkable on-current and superior off-state (*SS* < 100 mV/dec and low leakage current) can be attributed to the superior electrostatics of our scaled high-k gate stack[12,18]. To understand the device stability, we first performed hysteresis measurements, since both hysteresis and bias temperature instability (BTI) can elucidate the microscopic origin in the charge state of border traps[23,27–30]. Figure 1e shows the hysteresis characterization of a long-channel device (L_{CH} = 780 nm) with varying V_G sweep ranges. Notably, hysteresis increases as the end-scan voltage becomes more negative, implying that the Fermi level in the deep off-state (V_G = −1.5 V) is adjacent to a defect band in the insulator while the hysteresis is relatively small (~20 mV) when V_G is scanned from 3.5 V to 0.5 V. In addition, we did not observe significant differences in hysteresis behavior between devices with different channel lengths. This observation aligns with predictions from a defect band model, as illustrated in the band diagram (Fig. 1a), where the gray window in the 2D channel refers to the Fermi-window moving from the on-state to the off-state. It is crucial to select an insulator whose defect bands, if any, are energetically far away from the conduction band edge of the semiconductor channel. Thus, employing high-κ HfO_2 dielectrics in 2D MoS_2 devices helps improve the reliability of 2D FETs.

Positive bias temperature stress (PBTS)

Figure 2a, b shows the time evolution of transfer characteristics (I_D-V_G) of 1L-MoS_2 FETs under a PBTS of 3 V at 295 K and 360 K, respectively. Figure 2c, d summarizes the resulting ΔV_{TH} of temperature and field-dependent PBTS. Surprisingly, the FETs exhibit an anomalous positive-to-negative transition in ΔV_{TH} at 295 K. A pronounced negative ΔV_{TH} is apparent under a 3 V PBTS at 360 K, implying a strong field and temperature-dependent activation of donor-trap formation. Notably, this two-stage degradation phenomenon observed at 295 K has been reported for oxide semiconductors (OS) FETs[31–34] and is for the first time reported here for 2D semiconductors. The two-stage ΔV_{TH} has been proposed to originate from a two-component degradation process. The initial positive ΔV_{TH} is typically attributed to electron trapping at the channel/oxide interface (N_{IT}) or within the oxide (N_{OT})[35,36]. Subsequently, a shift to negative ΔV_{TH} is associated with the possible generation of donor-like states via hydrogen (H) interaction[31–34]. Note that an interplay between different types of defects has already been observed for 2D FETs[37]. However, a two-stage voltage shift has not previously been observed. The Δ*SS* data under PBTS (V_G = 3 V) at 360 K, as depicted in Supplementary Figure 2a, suggests that this donor-like trap generation is more likely due to interface trap (D_{it}) generation instead of bulk or border trap generation as evident from increasing Δ*SS* with increasing stress time. Consequently, these newly generated donor-like traps should occur inside the channel and not the bulk insulator. It is important to highlight that, given the intrinsic nature of 2D FETs being "interface-only" transistors, defects in the channel can essentially be regarded as interface traps. A recovery test was also performed after subsequent stress with a V_G of 0 V for 2000 s, as shown in Supplementary Fig. 2b. The ΔV_{TH} results of recovery cycles after PBTS (V_G = 3 V) at 360 K imply such donor-like trap generation is permanent and unrecoverable. More detailed studies using an extended measure-stress-measure (eMSM) technique to extract the permanent component (P) and recoverable component (R) are needed[38–40].

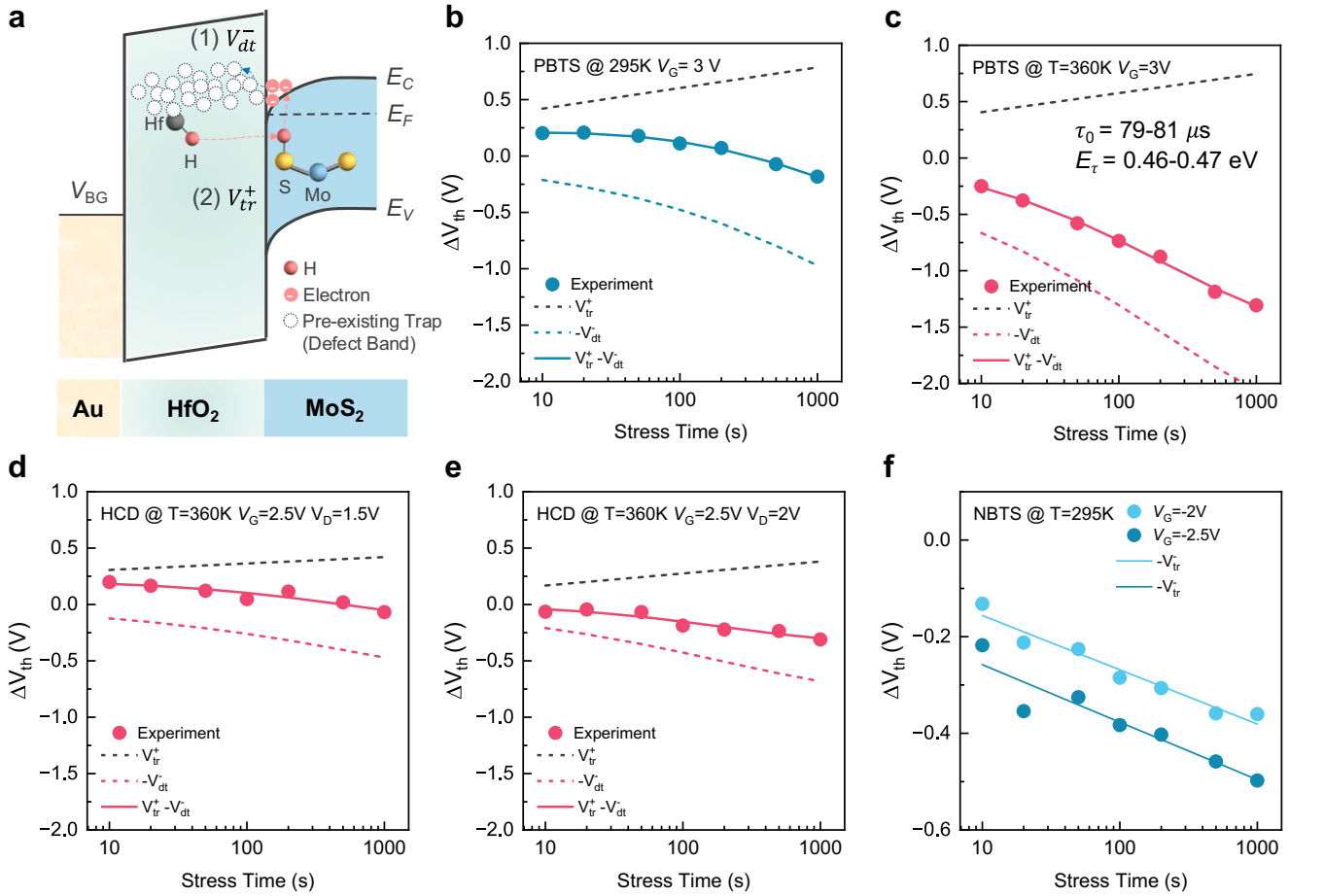

Fig. 3 | Reliability modeling and analysis of 1L-MoS_2 FETs on HfO_2 dielectric. **a** Band diagram of 1L-MoS_2 FETs on HfO_2 dielectric during PBTS and HCD. Decomposition of ΔV_{TH} under PBTS at 295 K with $V_G = 3$ V **b** at 295 K and **c** at 360 K. Decomposition of ΔV_{TH} at 360 K under HCD with **d** $V_G = 2.5$ V, $V_D = 1.5$ V and **e** $V_G = 2.5$ V, $V_D = 2$ V. **f** NBTS fitting results of ΔV_{TH} (t) at 295 K with $V_G = -2$ and -2.5 V.

Reliability modeling and analysis of 1L-MoS_2 FETs on HfO_2 dielectric

Such two-stage ΔV_{TH} shift can be explained by considering the reaction and diffusion of hydrogen due to residual hydrogen atoms in the low-temperature grown ALD oxide layer[33,34] and electron trapping in existing border traps, as shown in the band diagram (Fig. 3a). In particular, hydrogen can penetrate into a 2D channel and react with sulfur, forming sulfur vacancies. These vacancies act as newly generated donor traps. A similar phenomenon has been identified in high-hydrogen-concentration SiO_2 gate dielectrics[41], while it is first reported here for ALD HfO_2. With this qualitative understanding, we can quantitatively model the two-state ΔV_{TH} by a two-component degradation[32]. The observed changes in ΔV_{TH} can consistently be modeled across PBTS data in Fig. 2 using an uncorrelated sum of these two components, i.e.,

$$\Delta V_{th}(t) \equiv V_{tr}^{+}(t) - V_{dt}^{-}(t) = B_{tr}\log\left(\frac{t}{\tau_{tr}}\right) - C_{dt}\left(1 - e^{-\left(\frac{t}{\tau_{dt}}\right)^{\beta}}\right) \quad (1)$$

where B_{tr} and C_{dt} are voltage- and temperature-dependent prefactors of electron trapping in pre-existing states and donor-trap formation, respectively. The corresponding characteristic time-scale factors, τ_{tr} and τ_{dt}, also depend on voltage and temperature, while the power exponent β does not. The stretched-exponential functional form for donor-trap formation is empirical, but its general form and the exponent β can be physically justified[32]. Note that although the model is empirical, similar to the Reaction-Diffusion (RD) model, this simplified model remains widely used for reliability modeling in advanced devices like FinFETs[42–44] and oxide transistors[32–34,45]. Figure 3b, c presents the fitting results for PBTS ($V_G = 3$ V) at 295 K and 360 K, expressed as $\Delta V_{th}(t) = V_{tr}^{+}(t) - V_{dt}^{-}(t)$. Notably, $V_{tr}^{+}(t)$ increases with an increasing vertical electric field. The negative contribution from the donor traps, denoted as $V_{dt}^{-}(t)$, is relatively small at low PBTS of $V_G = 2.5$ V (Supplementary Fig. 3a, b, dotted blue line) but significantly increases at high PBTS and 360 K (Fig. 3b, c, dotted red line). This suggests a strong field and temperature dependence of the donor-trap formation, i.e., $\tau_{dt}(T) = \tau_0 e^{\left(\frac{E_\tau}{kT}\right)}$[36] (β~0.38–0.39, $\tau_0 = 79$–81 μs, and $E_\tau = 0.46$–0.47 eV are determined by fitting, in line with $E_\tau = 0.48$ eV reported in In_2O_3[32]). This phenomenon can be explained by the enhanced release of hydrogen atoms from HfO_2 at higher V_G, considering the high hydrogen concentration in low-temperature ALD dielectrics[33,34]. Additionally, the elevated temperature accelerates the chemical reaction of creating shallow donor levels. Note that any superposition of positive and negative components can produce a good fit. Therefore, the data set is designed to fit PBTS at different temperatures (Fig. 3b, c), where the donor trap generation is strongly temperature-activated[46].

In addition to hydrogen-related donor state generation, the abnormal PBTS observed in HfO_2-based devices could be caused by a variety of factors, including oxide defects on both the gate and channel sides and potential contamination from mobile impurities due to the wet transfer process. However, we can rule out gate-side defects and contaminations from the transfer process for the following reasons. First, gate-side defects are unlikely to be the primary cause of the abnormal ΔV_{TH} shift. This is supported by the fact that the subthreshold slope (ΔSS) coincides with the ΔV_{TH} shift during PBTS as shown in Supplementary Fig. 2, suggesting that

the donor-like trap generation is more likely related to interface trap generation rather than gate-side defects. Secondly, comparing the PBTS behavior of hBN-based devices and HfO_2-based devices (Supplementary Fig. 1), both of which used the same wet transfer process, suggests that impurities from the transfer process are not the main cause of the abnormal PBTS observed in HfO_2-based devices. This is further supported by the absence of this abnormal behavior in hBN devices.

Figure 3d, e illustrates that hot carrier degradation (HCD) under different V_G and V_D conditions can be interpreted via Eq. (1) as well. The $V_{dt}^{-}(t)$ component is characterized by a voltage- and temperature-independent time exponent (β~0.38–0.39). Interestingly, positive PBTS induces a more pronounced negative shift compared to HCD. This is ascribed to the higher and more uniform vertical field induced by strong PBTS, a feature arising from the atomically-thin channel relative to its length – a critical distinction from classical devices. While hot carrier degradation (HCD) in silicon FETs is regarded as a primary reliability concern in scaled devices, our understanding of HCD in 2D material-based devices remains limited[47]. There is an urgent need for more comprehensive reliability modeling and experimental investigations to elucidate the underlying physics of HCD degradation. This is especially crucial considering that the atomic thinness of 2D materials might render them particularly susceptible to hot carrier-triggered dissociation. To summarize, the data decompositions we performed demonstrate the versatility of Eq. (1) in describing both PBTS and HCD through combinations of the two degradation components. The similarities between PBTS and HCD concerning voltage and temperature dependence imply that similar mechanisms are likely driving these phenomena. The time evolution of transfer characteristics (I_D-V_G) of 1L-MoS_2 FETs and ΔV_{TH} during stress and recovery cycles under a HCD of V_D = 1.5 and 2 V at 360 K can be seen in Supplementary Fig. 4.

For NBTS, as depicted in Fig. 3f, ΔV_{TH} can be described only by $V_{th}(t) \equiv -V_{tr}^{-}(t) = -B_{tr}\log\left(\frac{t}{\tau_{tr}}\right)$, which implies electron de-trapping from pre-existing defects in the dielectric. Notably, $V_{tr}^{-}(t)$ increases with an increasing vertical electric field, similar to PBTS. This absence of $V_{dt}^{-}(t)$ in NBTI suggests that the H interaction exhibits a polarity dependence. One possible explanation is that positively charged H can react with sulfur in 1L-MoS_2, creating donor-like sulfur vacancies. In contrast, in the case of NBTS, the positively charged H cannot react and diffuse into the 1L-MoS_2, as shown in the band diagram (Fig. 3a). Supplementary Fig. 5a, b displays the detailed time evolution of transfer characteristics (I_D-V_G) of 1L-MoS_2 FETs under a NBTS of −2 V at 295 K and 360 K. The Δ*SS* data under NBTS (V_G = −2 V and V_G = −2.5 V) at 295 K is shown in Supplementary Fig. 5c. In contrast to the Δ*SS* data under PBTS (V_G = 3 V) at 360 K, as shown in Supplementary Fig. 2a, Δ*SS* in NBTS remains unchanged, indicating that NBTS and PBTS have fundamentally different physical origins.

Reliability mechanisms and benchmark

To investigate the physical origin of this observed donor state generation during PBTS, we have performed Elastic Recoil Detection Analysis (ERDA) characterization to measure the levels of hydrogen in ALD HfO_2, as shown in Fig. 4a and Supplementary Fig. 6. More details on ERDA characterization are provided in Methods. From this analysis, we found that hydrogen accounts for ~2% in atomic fraction, as illustrated in Fig. 4a and Supplementary Fig. 6. In addition to hydrogen, we also observed a small amount of carbon residuals, which could come from the precursors or the photoresist during lithography. Interestingly, our analysis showed that the tetrakis(dimethylamido)hafnium (TDMAH) precursor used in ALD HfO_2 contains approximately five times higher levels of hydrogen compared to the $HfCl_4$ precursor. These findings suggest that hydrogen is more likely responsible for the observed donor-like state generation due to its strong absorption and diffusion through 2D monolayer, according to some previous works[14]. Similar findings on hydrogen-induced anomalous NBTS have been reported in recent studies on oxide semiconductor-based transistors[1–4].

Figure 4b illustrates how hydrogen-assisted donor states, such as sulfur vacancies, are generated. Before stress is applied, we assume that the 2D semiconductor has no intrinsic defects, and the Fermi level aligns at the charge-neutral position. Note that the distribution of the density of states (DOS) depends on the band structure and dimensionality of materials. During stress, the Fermi level moves deeper into the conduction band, creating mobile carriers in the channel. Simultaneously, donor state generation occurs, possibly due to hydrogen drifting and moving into the channel and reacting with sulfur to form sulfur vacancies. Note that for PBTS, the most likely H diffusion is a positive ion due to lower formation energy[48]. After stress is applied, to maintain charge neutrality, the Fermi level settles between the donor states and the conduction band. These donor states are associated with positively charged states due to the thermal broadening of the Fermi distribution. This explains why the donor state generation can be regarded as positively charged (negative shift of V_{TH}), which in turn affects the subthreshold slope (SS). Many studies using density functional theory (DFT) calculations have shown that sulfur vacancies are the most common defects in 2D TMDs[49,50]. Additionally, scanning tunneling microscopy (STM) clearly shows the donor states around sulfur vacancies[51].

Discussion

To further confirm the H-related donor trap generation in ALD high-κ dielectrics, we have performed the same reliability characterization from above on 1L-MoS_2 FETs using exfoliated hBN as the dielectric. The detailed time evolution of I_D-V_G of devices under a PBTS and HCD can be seen in Supplementary Fig. 7a, b. Remarkably, the two-stage ΔV_{TH} shift is entirely absent in both PBTS and HCD, even at elevated temperatures (Supplementary Fig. 7c). It is worth to note that the reliability characterization of 1L-MoS_2 FETs on thick hBN (around 90 nm) has been previously reported[22].

Figure 4c shows a benchmark plot, illustrating the reliability of 2D TMD FETs with various gate dielectrics. In general, 1L-MoS_2 FETs on scaled high-k HfO_2 demonstrate better stability than on thicker dielectrics. In our analysis of reliability mechanisms, as depicted in Figs. 3a and 4b, we find that interface trap generation plays a crucial role in crystalline insulators, while in ALD high-κ dielectrics, a combination of electron trapping in pre-existing defects and hydrogen-assisted donor trap generation primarily contributes to degradation. Fabrication-related defects represent another degradation factor in ALD high-κ dielectrics, which cannot be purely explained by the defect band theory of dielectrics[25]. Consequently, steps towards enhancing stability should include optimization of the ALD process and strategic tailoring of the defect band's position[25]. Further improvement in ALD dielectric processes with dual-gate encapsulation and interfacial layer engineering is key for the reliability of 2D FETs to meet commercial technology standards.

In conclusion, we systematically characterize PBTS, HCD, and NBTS to elucidate the degradation mechanisms of 1L-MoS_2 FETs using scaled high-κ HfO_2 and crystalline h-BN as dielectrics. Our detailed analysis and modeling highlight the significant role of the gate dielectric and its interface on 2D TMD reliability. It is not only the electron trapping but also the hydrogen-assisted donor trap generation that significantly impacts the stability of 1L-MoS_2 FETs on high-κ HfO_2. In contrast, for devices utilizing h-BN dielectric, the reliability is predominantly determined by interface trap generation, mirroring the behavior observed in silicon transistors. These findings collectively indicate that high-performance 2D monolayer transistors can achieve acceptable reliability by optimizing the ALD process and selecting the most favorably matched 2D channel/3D oxide combinations. Further investigation is essential for other promising insulators and 2D channel combinations for p-FETs, such as the Al_2O_3/HfO_2 gate stack on WSe_2.

Methods

Material

1L-MoS_2 film was purchased from 2D semiconductor cooperation.

Device fabrication on scaled ALD HfO_2

The fabrication starts with patterning of a 3 nm Cr/ 12 nm Au local bottom gate (LBG), followed by the deposition of 6 nm ALD HfO_2 at 200 °C (κ ~ 15

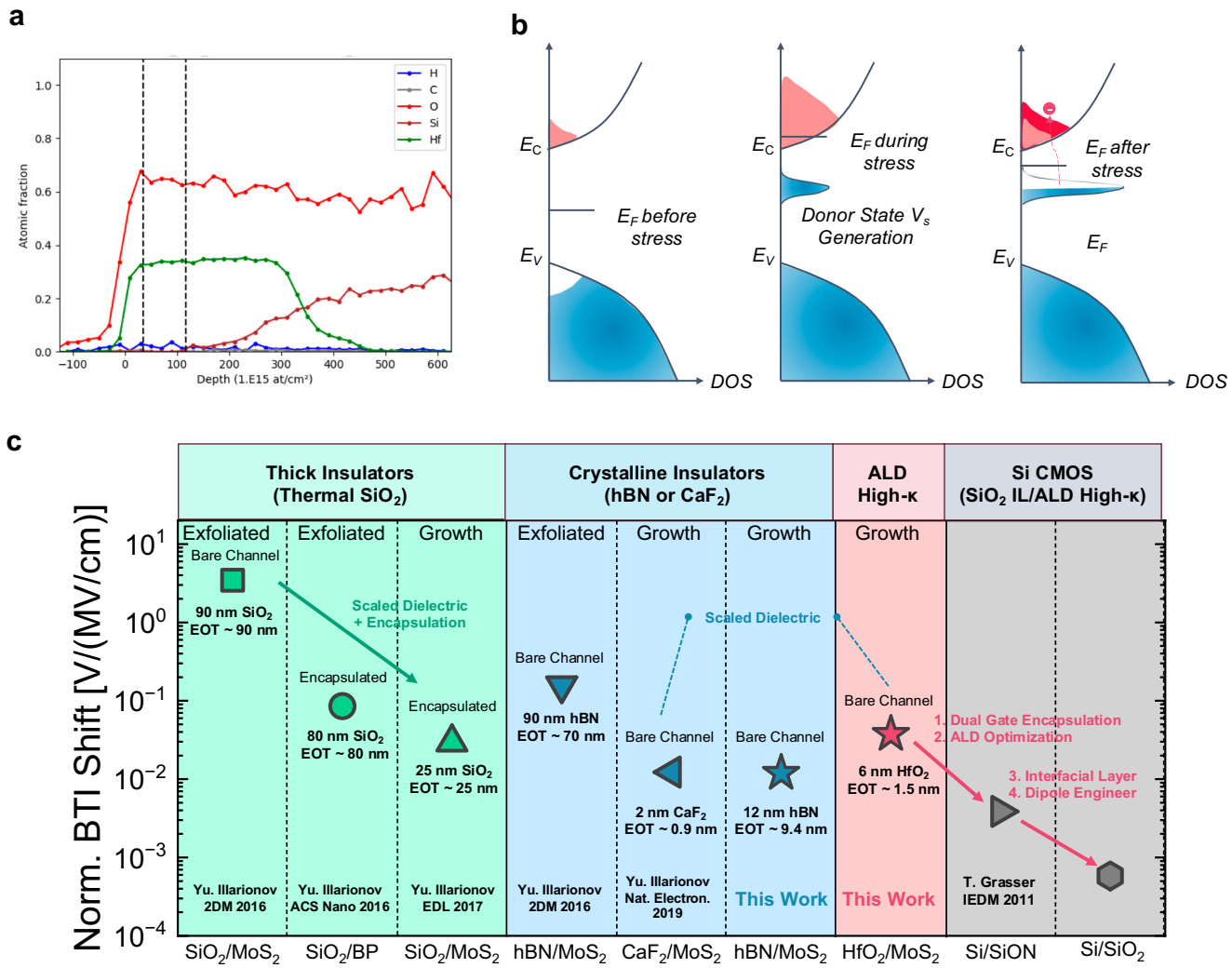

Fig. 4 | Reliability mechanism of 1L-MoS_2 FETs with HfO_2 gate dielectric. **a** Characterization of hydrogen concentration by elastic recoil detection analysis (ERDA). **b** Schematics of hydrogen-assisted donor state generation within MoS_2 channel. **c** Benchmarking of reliability of 2D FETs with different gate dielectrics. Four potential dielectric stacks and process optimization to further improve device reliability.

and EOT ~ 1.5 nm), serving as the bottom gate dielectric. Subsequently, 1L-MoS_2 crystals are wet-transferred onto the LBG substrate. To define the FET channel, we utilize reactive ion etching with Cl_2/O_2 at a power of 40 W for 15 seconds. 60 nm Ni source/drain (S/D) contacts are patterned using e-beam lithography and e-beam evaporation. The detailed steps can be seen in Supplementary Fig. S1.

Device fabrication on exfoliated hBN

We mechanically exfoliated multi-layer hBN flakes from bulk hBN crystal, purchased from 2D Semiconductors, on polydimethylsiloxane stamps in an argon-filled glovebox. Subsequently, a custom-built dry transfer tool was employed to transfer the hBN on top of the LBG. The remaining device fabrication is similar to the one described in the above section.

Electrical measurements

The DC electrical measurements were performed in a probe station under vacuum (~1×10^{-5} torr) at room temperature. The reliability characterization is carried out under the same vacuum conditions at both room temperatures 295 K and 360 K for accelerated testing purposes and leverages stress-measure-stress (SMS) and recovery techniques. V_{TH}–values are extracted using the constant current method at $I_D = 0.1$ μA/μm at $V_D = 0.1$ V.

Elastic recoil detection analysis (ERDA)

The ERDA is a technique used to determine the depth profiles of elemental concentrations in thin films using ion beams. This ion beam analysis technique allows us to probe the atomic areal densities. The results are reported in units of 10^{15} atoms/cm^2. The compositions are based on the slab regions as indicated with vertical lines in the depth-profile spectrum. Note that the concentrations refer to atomic fractions: i.e., at%, not weight %.

Data availability

The data that support the findings of this work are available from the corresponding author upon reasonable request.

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Author contributions

H.-Y.L., J.A., and Z.C. proposed the original idea. H.-Y.L. performed device fabrication, device characterization, and data analysis. S.-H.Y. helped with device characterization. K.-A.K and D.C. conducted ERDA characterization. R.T. helped with device fabrication. H.-Y.L., J.A., and Z.C. wrote the paper, and all authors discussed and revised the final manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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