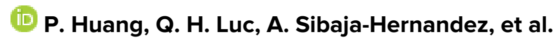
AIP Advances

Investigation of device transport characteristics enhancement of $In_{0.53}Ga_{0.47}As$ MOSFET through *in situ* NH_3/N_2 remote-plasma treatment

Cite as: AIP Advances **11**, 015050 (2021); https://doi.org/10.1063/5.0037378
Submitted: 14 November 2020 • Accepted: 26 December 2020 • Published Online: 28 January 2021



P. Huang, Q. H. Luc, A. Sibaja-Hernandez, et al.

View Online

Export Citation

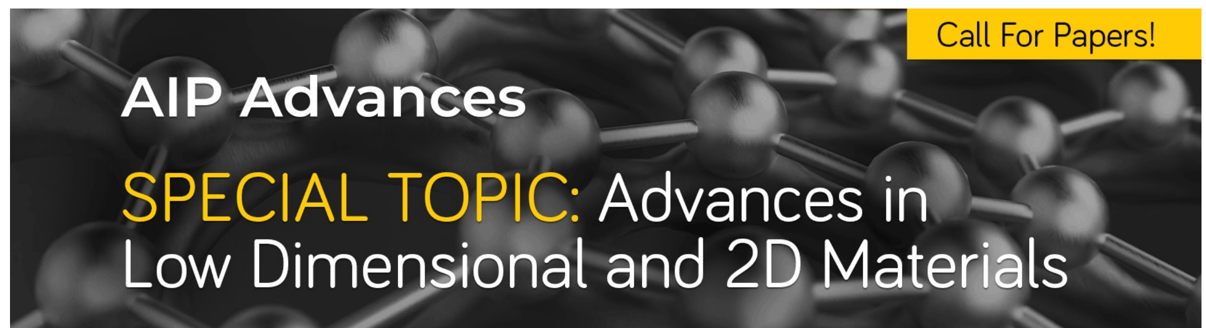
CrossMark

ARTICLES YOU MAY BE INTERESTED IN

Effects of oxide traps, interface traps, and "border traps" on metal-oxide-semiconductor devices
Journal of Applied Physics **73**, 5058 (1993); https://doi.org/10.1063/1.353777

Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces
Journal of Applied Physics **108**, 124101 (2010); https://doi.org/10.1063/1.3520431

Room-temperature deposition of a poling-free ferroelectric AlScN film by reactive sputtering
Applied Physics Letters **118**, 082902 (2021); https://doi.org/10.1063/5.0035335



AIP Publishing

© 2021 Author(s).

Investigation of device transport characteristics enhancement of $In_{0.53}Ga_{0.47}As$ MOSFET through *in situ* NH_3/N_2 remote-plasma treatment

Cite as: AIP Advances 11, 015050 (2021); doi: 10.1063/5.0037378
Submitted: 14 November 2020 • Accepted: 26 December 2020 •
Published Online: 28 January 2021

View Online

Export Citation

CrossMark

P. Huang,[1] Q. H. Luc,[2] A. Sibaja-Hernandez,[3] C. W. Hsu,[2] J. Y. Wu,[1] H. L. Ko,[1] N. A. Tran,[2] N. Collaert,[3] and E. Y. Chang[1,2,4,a)]

AFFILIATIONS

[1] International College of Semiconductor Technology, National Chiao Tung University, Hsinchu 30010, Taiwan
[2] Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan
[3] Imec, Leuven 3001, Belgium
[4] Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan

[a)] **Author to whom correspondence should be addressed:** edc@mail.nctu.edu.tw

ABSTRACT

In this work, we demonstrated considerable enhancement of the transport characteristics of n-type $Al_2O_3/In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors (n-MOSFETs) with the assistance of *in situ* NH_3/N_2 remote-plasma (RP) treatment. According to the measurement and simulation results, the RP treated sample shows superior device performances as compared to the control sample without plasma treatment including (a) improved on-current (I_{on}) from 8.5 mA/mm to 17 mA/mm, (b) improved transconductance (G_m) from 16.05 mS/mm to 28.52 mS/mm, (c) suppressed subthreshold swing from 189 mV/dec to 170 mV/dec, (d) suppressed drain induced barrier lowering from 36 mV/V to 28 mV/V, (e) intensified peak effective mobility (μ_{eff}) from 1896 cm^2 V^{-1} s^{-1} to 2956 cm^2 V^{-1} s^{-1}, and (f) reduced acceptor-type density of interface trap state ($D_{it,A}$) to 44%. By using TCAD simulation, device output performance is found to be dramatically impacted by the trap state (especially acceptor-type) at the Al_2O_3/InGaAs interface.

© 2021 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/). https://doi.org/10.1063/5.0037378

I. INTRODUCTION

$In_xGa_{1-x}As$ materials featuring light effective electron mass (m_e), high injection velocity (V_{inj}), and electron mobility (μ_e) (Refs. 1 and 2) are considered as remarkable channel materials in fabricating n-type metal-oxide-semiconductor field-effect transistors (n-MOSFETs) for the advanced digital, analog, and high-speed electronic devices (Ref. 3). With the continuous down-scaling of device critical dimension, high-κ gate dielectrics are integrated into the technology nodes to suppress the leakage current (Ref. 4). Among the enormous diversity of high-κ dielectrics, Al_2O_3 is widely used for $In_xGa_{1-x}As$ MOSFET due to its outstanding properties including high thermal stability, high breakdown voltage, and proper band-offset (Ref. 5). Although Al_2O_3 has much lower dielectric permittivity compared to Hf-based dielectrics, which are extensively used in silicon technology, it possesses a more favorable interface quality. However, several obstacles need to be addressed in the Al_2O_3/InGaAs system. For instance, a high density of interface state (D_{it}) gives rise to Fermi level pinning (Ref. 6) and induces a scattering potential to the mobile channel charge, which is known as Coulomb scattering (Ref. 7). In addition, surface roughness scattering (Ref. 8), which originates from the surface irregularity, induces a perturbation potential to the channel charges and results in mobility degradation. Moreover, fixed oxide charge (N_{fix}) shifts the device flat-band voltage (V_{FB}) from the ideal value (Ref. 9), causing a long-term reliability issue. The above-mentioned issues consequently cause degradation in device performance and reliability. Besides these deteriorating effects due to the interface and the gate dielectric, the low conduction band density of states (DOS) also limits the device performance (Ref. 10). As a result, the on-current (I_{on}) and the transconductance (G_m) of the InGaAs transistors can be even lower than its silicon counterpart (Refs. 11 and 12), which limits the device performances. Many groups have been devoted to the optimization of the growth of high-κ dielectric and the interface

© Author(s) 2021

passivation techniques to improve the device performance. Atomic-layer-deposition (ALD), which controls the growth of the gate dielectric within a single atomic layer, is well known for its "self-cleaning" effect (Refs. 13 and 14). The self-cleaning effect in ALD assists in removing the surface dangling bonds on the InGaAs surface and in decreasing the number of interface traps. Interface engineering such as chemical solution treatment (Refs. 15–18) or plasma treatment (Refs. 19–25) as the pre-/post-gate deposition helps in removing the InGaAs native oxides (As_2O_3, As_2O_5, Ga_2O_3, and In_2O_3) and the interface traps. In this work, we applied an *in situ* remote-plasma treatment (RP treatment) using the NH_3/N_2 gas mixture while depositing the Al_2O_3 through ALD to further improve the quality of the high-κ/InGaAs interface. In addition, a control sample (Ctrl) without RP treatment is fabricated as a reference. With the assistance of the measurement and simulation results, the origin of the enhanced device performance is clearly elaborated. This paper is organized as follows: the device fabrication and simulation setup are described in Sec. II and the measurement results are shown in Sec. III. TCAD simulations are carried out to elucidate the physical phenomena behind the measured results. Therefore, Sec. IV will be devoted to the combination of TCAD simulations and discussion. Finally, the conclusions will be given in Sec. V. It is noteworthy that these results can be extensively applied to other categories of high-κ gate dielectrics as well.

II. DEVICE FABRICATION AND SIMULATION SETUP

A. Device fabrication

The epitaxial layers used in this work were grown by molecular beam epitaxy (MBE) consisting of a 2-in. p^+-InP substrate, a 100 nm *p*-InP buffer layer (1×10^{18} cm^{-3} doped by beryllium), and a 50 nm *p*-InGaAs channel layer (5×10^{16} cm^{-3} doped by beryllium). The device fabrication begins with field oxide deposition followed by mesa isolation through photolithography to define the active area. Next, the samples were soaked in dilute HCl and $(NH_4)_2S$ solution, which is known as chemical pre-treatment, to remove the native oxide. Then, 5 nm Al_2O_3 accompanied by NH_3/N_2 remote-plasma treatment with a power of 150 W with a duration time of 120 s was deposited as a gate dielectric using Ultratech Fiji G2 ALD. Meanwhile, the control sample (Ctrl) without NH_3/N_2 RP treatment was also fabricated. Both of the samples were annealed at N_2 ambient in the condition of 400 °C, 2 min sequentially. Moreover, 150-nm TiN was deposited as a gate electrode by physical vapor deposition (PVD) followed by the formation of source/drain (S/D) regions through Si implantation with a dose of 1×10^{14} cm^{-2} at 20 keV and activation with rapid thermal annealing (RTA) in the condition of 650 °C, 15 s. Furthermore, Au/Ge/Ni/Au and AuBe were deposited by electron beam evaporation as the source/drain and the backside electrodes, respectively. Finally, post-metallization annealing was performed in the condition of 270 °C, 30 s to achieve a preferable ohmic contact. Figures 1(a) and 1(b) show the device structure and process flow for the fabricated MOSFET, while the sample treatment conditions, as well as device critical dimension, are listed in Tables I and II, respectively.

TABLE I. Sample conditions and treatment methodologies.

	$(NH_4)_2S$ chemical	NH_3/N_2 remote-plasma treatment
Ctrl sample	Yes	No
RP treatment sample	Yes	Yes

TABLE II. Device critical dimension.

Symbol	Quantity	Unit
L	Gate length	6 μm
W	Gate width	100 μm
L_{ext}	S/D extension length	20 μm
T_{ox}	Gate oxide thickness	5 nm
ε_{ox}	Gate oxide dielectric constant	8.9

B. Simulation setup

The Sentaurus TCAD S-process and S-device tools (Refs. 26 and 27) were used to measure the device characteristics and study

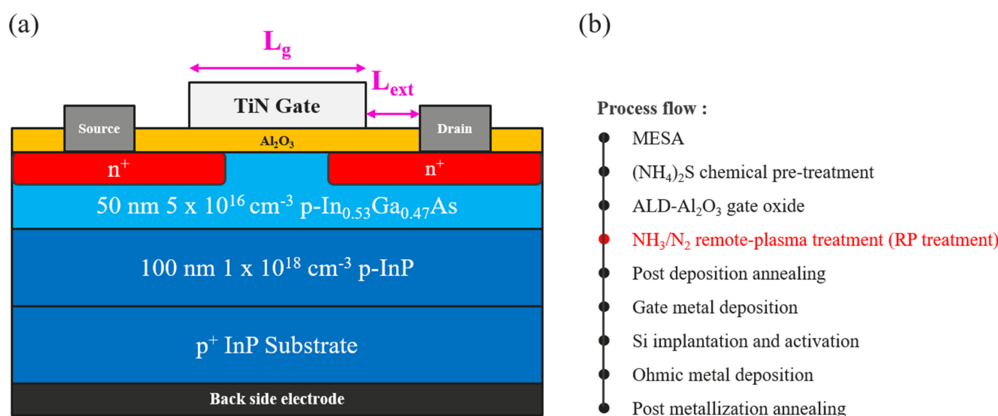


FIG. 1. (a) $In_{0.53}Ga_{0.47}$As MOSFET device structure, L_g is the physical gate length (6 μm) and L_{ext} is the source/drain extension length (20 μm). This figure is not to scale. (b) Process flow of inversion mode $In_{0.53}Ga_{0.47}$As MOSFET.

© Author(s) 2021

the physical mechanisms. The accuracy of the simulation is verified through the comparison between measurement and simulation results. The physical models used in the simulation are summarized as follows: (a) Fermi–Dirac statistics for low conduction band DOS semiconductors, which means that the Fermi level could be very close to or even beyond the conduction band edge, with the density-gradient quantum correction model that was used to capture the carrier and electrical potential distributions in InGaAs. (b) The inversion-and-accumulation-layer mobility model was used to describe the doping-dependence of the mobility and the mobility degradation at the high-κ/InGaAs interface due to acoustic phonon and surface roughness scattering. (c) The interface trap scattering model was included to describe the Coulomb scattering of the channel mobile carriers by the interface traps. (d) A multi-valley model with conduction band non-parabolicity was used to depict the band structure of InGaAs precisely. (e) Shockley–Read–Hall with doping-dependent carrier lifetimes, band-to-band tunneling, and Auger recombination models were all included to describe the device characteristics in the sub-threshold and off-state regions.

III. MEASUREMENT RESULTS

A. Split-CV measurement

The principle of split-CV measurement can be found in Ref. 28. In this measurement, a DC bias from −2 V to 2 V combined with a small amplitude (=25 mV) AC signal (frequency from 10 kHz to 1 MHz) was applied to the gate electrode using a 4284A LCR meter. Typically, the drain to source voltage (V_{ds}) is kept as low as possible to obtain uniform carrier distribution in the inversion channel. The split-CV measurement results are shown in Figs. 2(a) and 2(b), where C_{gc} refers to channel capacitance. From these results, we can easily observe that the "humps," located at the gate to source voltage (V_{gs}) = −1 V to −0.5 V, were suppressed after RP treatment. These humps are attributed to the interaction between the interface states and the channel carriers. In addition to the inhibition of the "humps," the results also show that V_{FB}, extracted according to (Ref. 29), shifts from −0.14 V to −0.43 V after RP treatment. Frequency dispersion observed in the inversion region is not discussed in this paper since it relates to the long life-time traps inside the gate dielectric, not the interface states (Ref. 30).

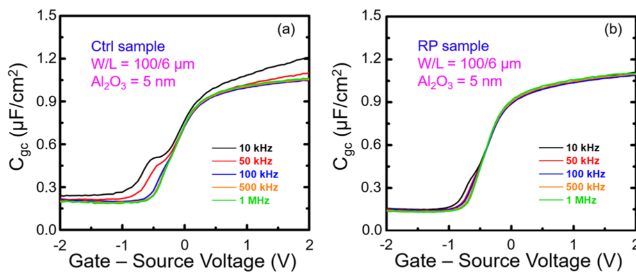


FIG. 2. C_{gc} vs V_{gs} measured at V_{ds} = 0.05 V for (a) the Ctrl and (b) RP treatment samples. The measurement frequency range is from 10 kHz to 1 MHz. The suppression of the humps indicates the successful reduction of interface states. The extracted flat-band voltage, V_{FB}, according to Ref. 27 is −0.14 V and −0.43 V for the Ctrl and the RP treatment samples, respectively.

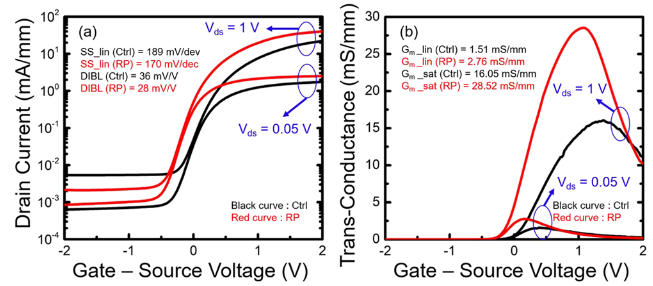


FIG. 3. DC characteristics of $In_{0.53}Ga_{0.47}As$ MOSFET with physical channel length = 6 μm and channel width = 100 μm for Ctrl and RP treatment samples, respectively: (a) I_{ds}–V_{gs} and (b) G_m–V_g curves. The devices were biased at linear (V_{ds} = 0.05 V) and saturation (V_{ds} = 1 V) regions.

B. DC measurement

DC characteristics including drain current (I_{ds}) and transconductance (G_m) vs V_{gs} shown in Figs. 3(a) and 3(b) was measured by using a Keysight HP 4156 precision semiconductor parameter analyzer. For the measurement conditions, V_{gs} is swept from −2 V to 2 V, while V_{ds} is biased in the linear region (V_{ds} = 0.05 V) and the saturation region (V_{ds} = 1 V). After RP treatment, on-current (I_{on}) increases from 8.5 mA/mm to 17 mA/mm, and off-current (I_{off}) decreases from 5.3 × 10^{-3} mA/mm to 2.1 × 10^{-3} mA/mm at V_{ds} = 1 V. The sub-threshold swing (SS) was improved from 189 mV/dec to 170 mV/dec, and the drain induced barrier lowering (DIBL) was improved from 36 mV/V to 28 mV/V. In Fig. 3(b), G_m increases dramatically from 1.51 mS/mm to 2.76 mS/mm and from 16.05 mS/mm to 28.52 mS/mm in linear and saturation regions, respectively.

C. Extraction of effective mobility

The effective mobility of electron, which is important in characterizing the device transport properties, can be calculated from the results of split-CV and DC measurements according to Eqs. (1) and

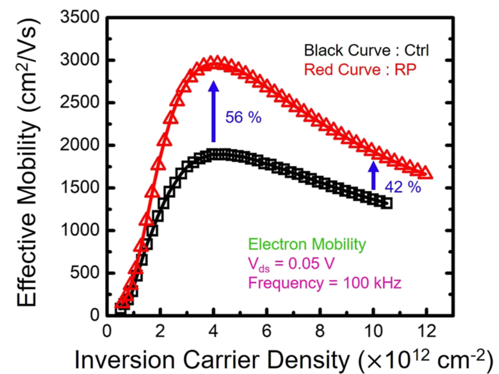


FIG. 4. Effective mobility (μeff) vs inversion carrier density for Ctrl and RP samples, respectively. The results are extracted at V_{ds} = 0.05 V and frequency = 100 kHz. The result of the RP treatment sample improved by 56% and 44% at N_{inv} = 4 × 10^{12} cm^{-2} and 1 × 10^{13} cm^{-2}, respectively, as compared to that of the control sample.

© Author(s) 2021

(2) from Ref. 31,

$$N_{inv} = 1/q \times \int_{-\infty}^{V_{gs}} C_{gc}(V_{gs}) \times dVgs, \quad (1)$$

$$\mu_{eff} = (I_{ds}/V_{ds}) \times (L/W)/(q \times N_{inv}), \quad (2)$$

where N_{inv} is the inversion carrier density in the channel and q is the elemental charge of the electron. The extracted effective mobility, at $V_{ds} = 0.05$ V and frequency = 100 kHz, is shown in Fig. 4. It can be seen that after the RP treatment, peak mobility increases from 1896 $cm^2 V^{-1} s^{-1}$ to 2956 $cm^2 V^{-1} s^{-1}$ around $N_{inv} = 4.5 \times 10^{12} cm^{-2}$, and the mobility near $1 \times 10^{13} cm^{-2}$ increases from 1366 $cm^2 V^{-1} s^{-1}$ to 1935 $cm^2 V^{-1} s^{-1}$.

IV. SIMULATION RESULTS

A. Pre-processing of simulation works

In order to understand the mechanism of the influences of RP treatment on the device characteristics in depth, we applied TCAD simulation to reproduce the measurement results with the help of physical models as mentioned in Sec. II B. Prior to the reproduction of the measurement results, some critical parameters need to be determined including (a) Ohmic contact resistance of the S/D region and (b) doping profile of the silicon implantation. The device contact resistance was obtained by transmission line measurement (TLM) with the assistance of the Keysight HP 4156 precision semiconductor parameter analyzer, and the implantation profile were obtained by a point to point correction Secondary Ion Mass Spectrometry (PCOR-SIMS^{SM}) measurement. These parameters were subsequently inserted into the TCAD tool to obtain reliable results. TLM results are shown in Fig. 5(a), the extracted contact resistivity (R_c) values are equal to 4.5×10^{-6} Ω cm^2/5×10^{-6} Ω cm^2, and the sheet resistance (R_{sh}) are equal to 130 Ω/sq/117 Ω/sq for the Ctrl/RP treatment samples, respectively. On the other hand, the SIMS profiles are shown in Fig. 5(b) in log and the linear scale. The negligible difference in the resistance value can be attributed to the slight migration of Si dopants toward the Al_2O_3/InGaAs interface.

B. Split-CV simulation and interface trap extraction

We brought about the fitting results of the split-CV measurement through physical models according to the measurement shown in Figs. 2(a) and 2(b). The fitting steps are described below, first of all, the doping profile of the MOSFET needs to be determined from SIMS; second, the thickness of the Al_2O_3 was obtained from the JEOL JEM-F200 transmission electron microscopy (TEM), and the dielectric constant was calculated to be 8.9 from the CV measurement; finally, D_{it} was input into the TCAD tool to simulate the effect of interface traps. According to the measurement methodology, the AC signal that is applied to the gate electrode induces a periodic change in the surface potential (Φ_s) of InGaAs and modifies the occupancy of the carrier in the interface states. The interface states, hence, contribute to an additional parallel capacitance, which is a function of Φ_s, to the split-CV measurement results (Ref. 32),

$$C_{it} = dQ_{it}/d\Phi_s, \quad (3)$$

where C_{it} is the capacitance induced by interface states and Q_{it} is the charge density of interface traps. The amount of Q_{it} is given by (Ref. 33)

$$Q_{it} = q \times \left(\int_{\Phi_s}^{+\infty} D_{it,D} \times dE - \int_{+\infty}^{\Phi_s} D_{it,A} \times dE \right), \quad (4)$$

where $D_{it,D}$ is the donor-like interface trap density and $D_{it,A}$ is the acceptor-like interface trap density. This increase in the total gate to channel capacitance brings in overestimation of the channel charge density and leads to an underestimation of the effective mobility. The simulation results of split-CV measurements are shown in Figs. 6(a) and 6(b). Two measurement conditions were selected to obtain the response of interface states in both high (1 MHz) and low (10 kHz) frequency regions.

The profile of interface trap distribution is shown in Fig. 7, where E_t is the energy position of the interface trap, E_v is top of the valence band, and E_c is the bottom of the conduction band. The distribution of the D_{it} profile is very similar to what was reported in Ref. 34. Acceptor traps distributed near the conduction band and donor traps are close to the valence band. Peak positions of donor-like and acceptor-like traps are located at $E_t - E_v = 0.05$ eV and 1.2 eV, respectively. It can be observed that $D_{it,A}$ is dramatically reduced (44% lower), while there is only a negligible change in the $D_{it,D}$ after RP treatment. This does make sense since the donor-like interface traps mainly affect the subthreshold region in the transistor and not much difference is observed in the SS after RP treatment. The considerable reduction in the acceptor traps is from the passivation of As–As antibonding states as reported in Refs. 35 and 36, which shows the same region of the trap position as in this work.

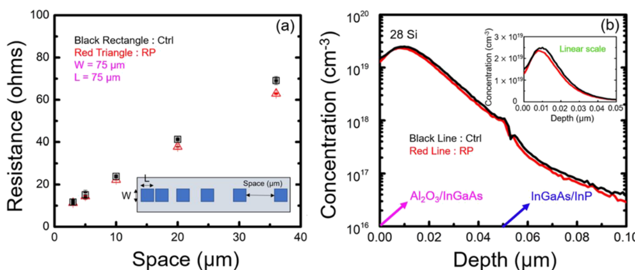


FIG. 5. (a) TLM results for Ctrl and RP treatment samples. The light blue region in the lower-right figure is covered by Al_2O_3. (b) SIMS measurements of the Si_{28} profile for the Ctrl and RP treatment samples. The dopant profiles start from the Al_2O_3/InGaAs interface.

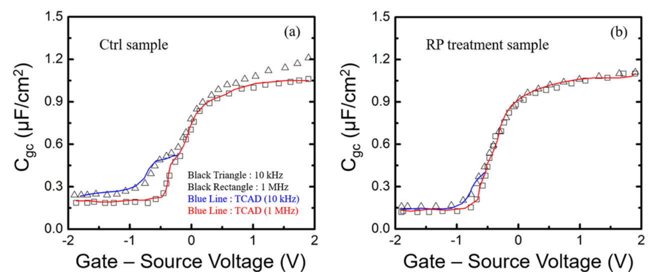


FIG. 6. Reproduction of the split-CV measurement at V_{ds} = 0.05 V, frequency = 10 kHz, and 1 MHz for Ctrl (a) and RP treatment (b) samples using TCAD simulation.

© Author(s) 2021

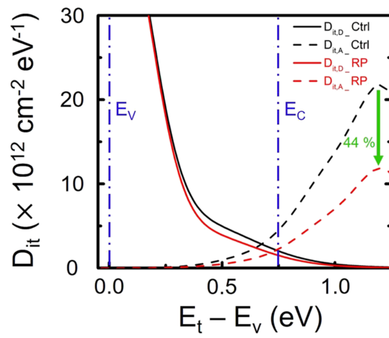


FIG. 7. Distribution of interface traps used in the reproduction of split-CV measurement. Black curves stand for donor-like interface traps, while red curves stand for acceptor-like interface traps. There is a considerable decrease in the acceptor-like traps for 44% lower at E_t–E_v = 1.2 eV after RP treatment.

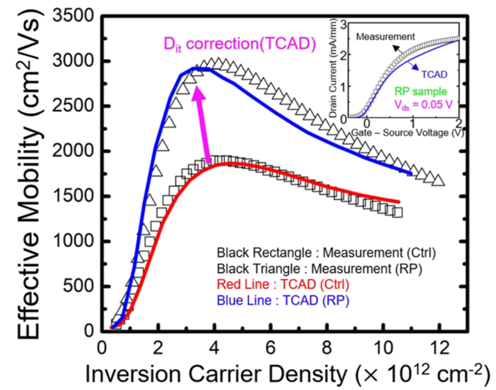


FIG. 9. Reproduction of the effective mobility measurement. The open symbols show the extracted effective mobility from measurements, and the curve lines are the TCAD results. The inset shows the comparison between measured and simulated I_{ds}–V_{gs} curves of the RP treatment sample at V_{ds} = 0.05 V.

C. Simulation and fitting of DC measurement results

Combining the above-mentioned measurements and the simulations of the CVs, we performed a TCAD to fit the DC performance of the Ctrl sample. The results are shown in Figs. 8(a) and 8(b). Applying the D_{it} profile (Ctrl) shown in Fig. 7 allows us to obtain a good agreement with the measurement results in both sub-threshold and on-state regions. The device off-state region can be fitted by adjusting the carrier lifetime in the simulations.

D. Simulation of effective mobility results

According to the good fitting results of split-CV as well as DC measurement results using TCAD, we demonstrated the fitting of the effective mobility curve of the Ctrl sample from the simulation. Figure 9 shows the good effective mobility overlaps between measurements and simulations. Since we have carefully fitted the split-CV and DC measurement results for the Ctrl sample, it is clear that we could obtain a good match between simulations and measurements presented as the red curve. Then, we simply modify the D_{it} profile from the Ctrl to RP treatment sample as shown in Fig. 7 to obtain a new effective mobility curve presented as the blue curve. The comparison between measured and simulated I_{ds}–V_{gs} curves of the RP sample at V_{ds} = 0.05 V, at which we extracted the effective

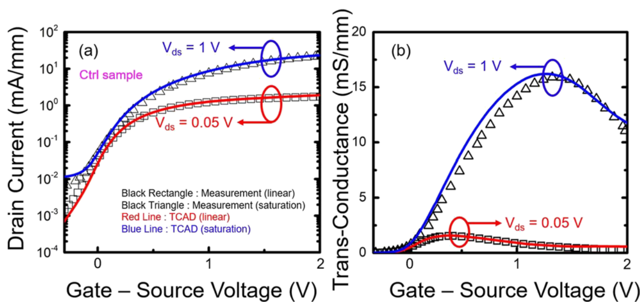


FIG. 8. (a) and (b) I_{ds}–V_{gs} and G_m–V_{gs} TCAD reproduction results for the Ctrl sample in the linear (V_{ds} = 0.05 V) and saturation (V_{ds} = 1 V) regions. Symbols stand for the measurement results, while solid lines stand for the simulation results.

mobility, is shown in the inset in Fig. 9 in the linear scale. Interestingly, the simulations of the RP treatment sample show good agreement with the measured results. This suggests that the improvement in the effective mobility is mainly coming from the reduction of interface trap scattering, especially the acceptor traps (As–As antibonding states) inside the conduction band. This result is consistent with the research result in Ref. 37. Besides, the small discrepancy ineffective mobility of the simulated RP sample could indicate that interface trap scattering is not the only degradation factor in the channel. However, it is worth noting that the enhanced simulated mobility is correctly captured without the introduction of additional parameters in the TCAD simulations. We could observe from the inset in Fig. 9 that there is a mismatch between the measurement result and the simulation. This indicates that other components might affect the transfer characteristics. According to Ref. 38, the shift of the peak mobility position toward higher inversion carrier density is either coming from the reduced remote phonon scattering or surface roughness scattering. These additional scattering effects could also be responsible for the mismatch in the peak μ_{eff}. In this paper, we only focus on the interface trap scattering since it is the dominating factor in determining effective mobility. More specific experiments (e.g., atomic force microscope for the surface roughness) or measurements (temperature variation) must be done to support the further calibration of the theoretical models. In the TCAD simulation, the total mobility of the device consists of several terms according to Matthiessen's rule shown in the following equation:

$$1/\mu_{eff} = 1/\mu_{dop} + 1/\mu_{ph} + 1/\mu_{sr} + 1/\mu_{it}, \quad (5)$$

where μ_{dop} is the mobility term from the impurity scattering, μ_{ph} is the lattice phonon scattering mobility, μ_{sr} is the surface roughness mobility, and μ_{it} is the interface trap scattering mobility. In this work, interface trap scattering is the dominant effect in causing mobility degradation. The formula for μ_{it} is shown in Eq. (6) from Refs. 39 and 40,

$$\mu_{it} = (T/300\,K) \times (1/E_{\perp}) \times (1/N_{it}^2) \times \exp(d/K), \quad (6)$$

© Author(s) 2021

where T is the transistor temperature in kelvin, $E_\perp$ is the electric field normal to the current flow in the channel, N_{it} is the interface trap density, d is the distance of the channel carrier from the interface, and k is the fitting parameter. This model treats the interface trapped charges as 2D-Coulomb scattering centers.

E. Simulation of traps-free interface

Supported by the good agreement in the simulation results while changing only the D_{it} profile, we can obtain an estimation of the device effective mobility after removing all the interface traps using the TCAD tool as a design guideline for the researchers. Effective mobility considering no interface traps (No_D_{it}) in the TCAD simulations is shown in Fig. 10(a). After removing all the interface traps, we can obtain a peak mobility of 6180 $cm^2 V^{-1} s^{-1}$ at $N_{inv} = 2.1 \times 10^{12}$ cm^{-2}. In Fig. 10(b), the simulated electron carrier density at the cut line x–x′ in the middle of the channel region at V_{gs} = 2 V and V_{ds} = 0.05 V for conditions including Ctrl, RP treatment, and No_D_{it} is shown. It can be seen that the interface traps capture the channel mobile carriers during the device operation, leaving fewer conducting carriers in the channel. These captured electrons hence form scattering centers, which results in the deterioration of the device performance.

However, in reality, it is impossible to reach an ultrahigh effective mobility value by removing all the interface traps. Deep acceptor traps have been proved to dominate the mobility degradation in previous paragraphs; therefore, we reveal a guideline in improving effective mobility by merely reducing the number of acceptor traps. The result is shown in Fig. 11, where $D_{it,A}'$ is the number of reduced acceptor traps and $D_{it,A}$ is the number of acceptor traps refers to the RP treatment sample in Fig. 7. We can see that by reducing the number of acceptor traps to one order of magnitude lower, we can obtain effective mobility that is already very close to the "ideal" value (without D_{it}). This gives us the possible solution that by focusing on the removal of acceptor traps, we can greatly improve the device effective mobility.

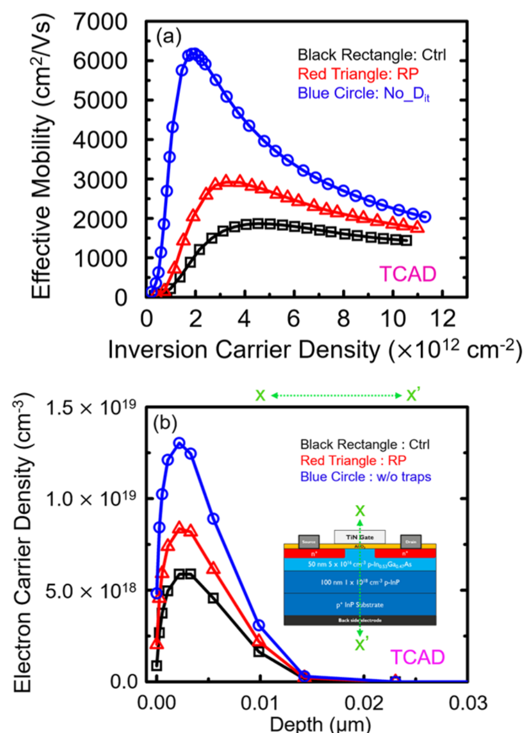


FIG. 10. (a) Effective mobility of InGaAs MOSFET extracted from simulations of Ctrl, RP treatment, and No_D_{it} samples. The peak value of effective mobility without D_{it} is 6180 $cm^2 V^{-1} s^{-1}$ and (b) simulated electron carrier density at the cut line x–x′ in the middle of the channel region.

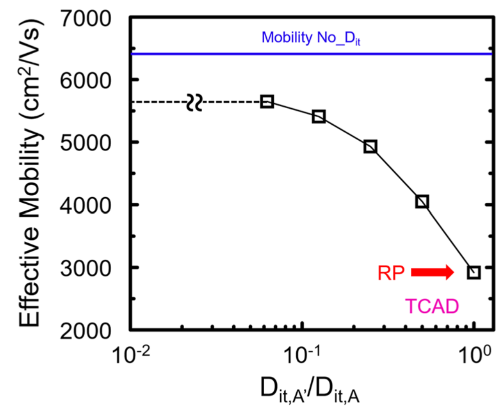


FIG. 11. The increase in effective mobility following the reduced $D_{it,A'}/D_{it,A}$ ratio. The blue line is the effective mobility for the sample without D_{it}.

V. CONCLUSIONS

In situ remote-plasma NH_3/N_2 treatment is proved to provide beneficial effects for enhancing the device electrical characteristics including (a) on-current, (b) transconductance, and (c) effective electron mobility. We have used TCAD simulations with a consistent set of model parameters and two different profiles of interface traps to explain the physical mechanisms behind the split-CV, DC, and effective mobility results observed in the measurements. The main factor affecting the device characteristics after the RP treatment is the reduction of the acceptor-like interface traps (As–As antibonding states). We have estimated that by further suppressing the acceptor D_{it} by one order of magnitude, the effective mobility can be significantly enhanced. The decreased donor-like interface traps are responsible for the improved subthreshold swing in the MOSFET and the suppressed humps in the CV curve. This study provides a guideline for fabricating more robust device transport characteristics for future III–V CMOS electronics.

ACKNOWLEDGMENTS

This work was financially supported by the "Center for the Semiconductor Technology Research" from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education (MOE) in Taiwan. This work was also supported, in part, by the Ministry of

© Author(s) 2021

Science and Technology, Taiwan, under Grant No. MOST 109-2634-F-009-029 and the National Chung-Shan Institute of Science and Technology [Grant No. NCSIST-402-V209(109)].

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1] S. Takagi, T. Iisawa, T. Tezuka, T. Numata, S. Nakaharai, N. Hirashita, Y. Moriyama, K. Usuda, E. Toyoda, S. Dissanayake, M. Shichijo, R. Nakane, S. Sugahara, M. Takenaka, and N. Sugiyama, "Carrier-transport-enhanced channel CMOS for improved power consumption and performance," IEEE Trans. Electron Devices **55**(1), 21–39 (2008).

[2] D.-H. Kim, J. del Alamo, D. A. Antoniadis, and B. Brar, "Extraction of virtual-source injection velocity in sub-100 nm III–V HFETs," in *Proceedings of IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2009), pp. 1–4.

[3] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," Nature **479**, 317–323 (2011).

[4] R. D. Clark, "Emerging applications for high κ materials in VLSI technology," Materials **7**(4), 2913–2944 (2014).

[5] Y. Xuan, H. C. Lin, P. D. Ye, and G. D. Wilk, "Capacitance-voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effect transistor using atomic-layer-deposited Al_2O_3 gate dielectric," Appl. Phys. Lett. **88**(26), 263518-1–263518-3 (2006).

[6] N. Newman, W. E. Spicer, T. Kendelewicz, and I. Lindau, "On the Fermi level pinning behavior of metal/III–V semiconductor interfaces," J. Vac. Sci. Technol., B **4**, 931–938 (1986).

[7] S. Potbhare, N. Goldsman, G. Pennington, J. M. McGarrity, and A. Lelis, "Characterization of 4H-SiC MOSFET interface trap charge density using a first principles Coulomb scattering mobility model and device simulation," in *Proceedings of International Conference on Simulation of Semiconductor Processes and Devices* (SISPAD, Tokyo, Japan, 2005), pp. 95–98.

[8] F. Wang, S. P. Yip, N. Han, K. W. Fok, H. Lin, J. J. Hou, G. Dong, T. F. Hung, and K. S. Chan, "Surface roughness induced electron mobility degradation in InAs nanowires," Nanotechnology **24**(37), 375202 (2013).

[9] B. Shin, J. R. Weber, R. D. Long, P. K. Hurley, C. G. Van de Walle, and P. C. McIntyre, "Origin and passivation of fixed charge in atomic layer deposited aluminum oxide gate insulators on chemically treated InGaAs substrates," Appl. Phys. Lett. **96**(15), 152908-1–152908-3 (2010).

[10] M. V. Fischetti, L. Wang, B. Yu, C. Sachs, P. M. Asbeck, Y. Taur, and M. Rodwell, "Simulation of electron transport in high-mobility MOSFETs: Density of states bottleneck and source starvation," in *Proceedings of IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2007).

[11] E. G. Marin, F. G. Ruiz, A. Godoy, I. M. Tienda-Luna, and F. Gámiz, "Mobility and capacitance comparison in scaled InGaAs versus Si trigate MOSFETs," IEEE Electron Device Lett. **36**(2), 114–116 (2015).

[12] T. K. Agarwal, M. Rau, I. Radu, M. Luisier, W. Dehaene, and M. Heyns, "Performance comparison of s-Si, $In_{0.53}Ga_{0.47}As$, monolayer BP, and WS_2-based n-MOSFETs for future technology nodes—Part I: Device-level comparison," IEEE Trans. Electron Devices **66**(8), 3608–3613 (2019).

[13] C.-H. Chang, Y.-K. Chiou, Y.-C. Chang, K.-Y. Lee, T.-D. Lin, T.-B. Wu, M. Hong, and J. Kwo, "Interfacial self-cleaning in atomic layer deposition of HfO_2 gate dielectric on $In_{0.15}Ga_{0.85}As$," Appl. Phys. Lett. **89**(24), 242911 (2006).

[14] M. L. Huang, Y.-C. Chang, C.-H. Chang, Y. J. Lee, P. Chang, J. Kwo, T.-B. Wu, and M. Hong, "Surface passivation of III-V compound semiconductors using atomic-layer-deposition-grown Al_2O_3," Appl. Phys. Lett. **87**(25), 252-104–252-106 (2005).

[15] H. C. Lin, W. E. Wang, G. Brammertz, M. Meuris, and M. Heyns, "Electrical study of sulfur passivated $In_{0.53}Ga_{0.47}As$ MOS capacitor and transistor with ALD Al_2O_3 as gate insulator," Microelectron. Eng. **86**(7-9), 1554–1557 (2009).

[16] M.-S. Park, M. Razaei, K. Barnhart, C. L. Tan, and H. Mohseni, "Surface passivation and aging of InGaAs/InP heterojunction phototransistors," J. Appl. Phys. **121**(23), 233105 (2017).

[17] Y.-C. Fu, U. Peralagu, D. A. Millar, J. Lin, I. Provey, X. Li, S. Monaghan, R. Droopad, P. K. Hurley, and I. G. Thayne, "The impact of forming gas annealing on the electrical characteristics of sulfur passivated $Al_2O_3/In_{0.53}Ga_{0.47}As$ (110) metal-oxide-semiconductor capacitors," Appl. Phys. Lett. **110**(14), 142905 (2005).

[18] É. O'Connor, S. Monaghan, K. Cherkaoui, I. M. Povey, and P. K. Hurley, "Analysis of the minority carrier response of *n*-type and *p*-type $Au/Ni/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ capacitors following an optimized $(NH_4)_2S$ treatment," Appl. Phys. Lett. **99**(21), 212901 (2011).

[19] H.-J. Oh, A. B. S. Sumarlina, and S. J. Lee, "Interface engineering for InGaAs n-MOSFET application using plasma $PH_3–N_2$ passivation," J. Electrochem. Soc. **157**(11), H1051–H1060 (2010).

[20] P. Rodriguez *et al.*, "Cleaning of InGaAs and InP layers for nanoelectronics and photonics contact technology applications," ECS Trans. **69**(8), 251–259 (2015).

[21] P. Rodriguez, L. Toselli, E. Ghegin, N. Chevalier, N. Rochat, E. Martinez, and F. Nemouchi, "*In situ* cleaning of InGaAs surfaces prior to low contact resistance metallization," Microelectron. Eng. **156**, 91–96 (2016).

[22] Q. H. Luc, E. Y. Chang, H. D. Trinh, Y. C. Lin, H. Q. Nguyen, Y. Y. Wong, H. B. Do, S. Salahuddin, and C. C. Hu, "Electrical characteristics of n, p-$In_{0.53}Ga_{0.47}As$ MOSCAPs with *in situ* PEALD-AlN interfacial passivation layer," IEEE Trans. Electron Devices **61**(8), 2774–2778 (2014).

[23] Q. H. Luc, H. B. Do, M. T. H. Ha, C. C. Hu, Y. C. Lin, and E. Y. Chang, "Plasma enhanced atomic layer deposition passivated $HfO_2/AlN/In_{0.53}Ga_{0.47}As$ MOSCAPs with sub-nanometer equivalent oxide thickness and low interface trap density," IEEE Electron Device Lett. **36**(12), 1227–1280 (2015).

[24] Q. H. Luc, K. S. Yang, J. W. Lin, C. C. Chang, H. B. Do, S. H. Huynh, M. T. H. Ha, T. A. Nguyen, Y. C. Lin, C. Hu, and E. Y. Chang, "$In_{0.53}Ga_{0.47}$ as FinFET and GAA-FET with remote-plasma treatment," IEEE Electron Device Lett. **39**(3), 339–342 (2018).

[25] Q. H. Luc, S. P. Cheng, P. C. Chang, H. B. Do, J. H. Chen, M. T. H. Ha, S. H. Huynh, C. C. Hu, Y. C. Lin, and E. Y. Chang, "Effects of *in-situ* plasma-enhanced atomic layer deposition treatment on the performance of $HfO_2/In_{0.53}Ga_{0.47}AS$ metal-oxide-semiconductor field-effect transistors," IEEE Electron Device Lett. **37**(8), 974–977 (2016).

[26] Sentaurus™ Process User Guide, Version Q-2019.12, Synopsys, Inc., 2019.

[27] Sentaurus™ Device User Guide, Version Q-2019.12, Synopsys, Inc., 2019.

[28] D. K. Schroder, *Semiconductor Material and Device Characterization* (Wiley, New York, 1990).

[29] R. Winter, J. Ahn, P. C. McIntyre, and M. Eizenberg, "New method for determining flat-band voltage in high mobility semiconductors," J. Vac. Sci. Technol., B **31**(3), 030604 (2013).

[30] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, "A distributed model for border traps in Al_2O_3–InGaAs MOS devices," IEEE Electron Device Lett. **32**(4), 485–487 (2011).

[31] C. Hinkle, A. Sonnet, R. Chapman, and E. Vogel, "Extraction of the effective mobility of $In_{0.53}Ga_{0.47}As$ MOSFETs," IEEE Electron Device Lett. **30**(4), 316–318 (2009).

[32] R. Engle-Herbert, Y. Hwang, and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces," J. Appl. Phys. **108**(12), 124101-1–124101-15 (2010).

[33] K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," IEEE Trans. Electron Devices **55**(2), 547–556 (2008).

[34] G. Brammertz, A. Alian, D. H.-C. Lin, M. Meuris, M. Caymax, and W.-E. Wang, "A combined interface and border trap model for high-mobility substrate metal–oxide–semiconductor devices applied to $In_{0.53}Ga_{0.47}As$ and InP capacitors," IEEE Trans. Electron Devices **58**(11), 3890–3897 (2011).

© Author(s) 2021

[35]Y. Guo, L. Lin, and J. Robertson, "Nitrogen passivation at GaAs:Al_2O_3 interfaces," Appl. Phys. Lett. **102**(9), 091606 (2013).
[36]J. Robertson, Y. Guo, and L. Lin, "Defect state passivation at III-V oxide interfaces for complementary metal–oxide–semiconductor devices," J. Appl. Phys. **117**(11), 112806 (2015).
[37]N. Taoka, M. Yokoyama, S. H. Kim, R. Suzuki, R. Iida, S. Lee, T. Hoshii, W. Jevasuwan, T. Maeda, T. Yasuda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, "Impact of Fermi level pinning inside conduction band on electron mobility of $In_xGa_{1-x}As$ MOSFETs and mobility enhancement by pinning modulation," in *Proceedings of IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2011), pp. 610–613.
[38]L.-S. Wang, J.-P. Xu, L. Liu, Y. Huang, H.-H. Lu, and P.-T. Lai, "Influences of remote Coulomb and interface-roughness scatterings on electron mobility of InGaAs nMOSFET with high-κ stacked gate dielectric," IEEE Trans. Electron Devices **14**(5), 854–861 (2015).
[39]W. Zhu, J.-P. Han, and T. P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-κ dielectrics," IEEE Trans. Electron Devices **51**(1), 98–105 (2004).
[40]Y. Xuan, Y. Q. Wu, H. C. Lin, T. Shen, and P. D. Ye, "Submicrometer inversion-type enhancement-mode InGaAs MOSFET with atomic-layer-deposited Al_2O_3 as gate dielectric," IEEE Electron Device Lett. **28**(11), 935–938 (2007).

© Author(s) 2021