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Dual-logic-in-memory implementation with orthogonal polarization of van der Waals ferroelectric heterostructure

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Abstract

The rapid advancement of AI-enabled applications has resulted in an increasing need for energy-efficient computing hardware. Logic-in-memory is a promising approach for processing the data stored in memory, wherein fast and efficient computations are possible owing to the parallel execution of reconfigurable logic operations. In this study, a dual-logic-in-memory device, which can simultaneously perform two logic operations in four states, is demonstrated using van der Waals ferroelectric field-effect transistors (vdW FeFETs). The proposed dual-logic-in-memory device, which also acts as a two-bit storage device, is a single bidirectional polarization-integrated ferroelectric field-effect transistor (BPI-FeFET). It is fabricated by integrating an in-plane vdW ferroelectric semiconductor SnS and an out-of-plane vdW ferroelectric gate dielectric material—$CuInP_2S_6$. Four reliable resistance states with excellent endurance and retention characteristics were achieved. The two-bit storage mechanism in a BPI-FeFET was analyzed from two perspectives: carrier density and carrier injection controls, which originated from the out-of-plane polarization of the gate dielectric and in-plane polarization of the semiconductor, respectively. Unlike conventional multilevel FeFETs, the proposed BPI-FeFET does not require additional pre-examination or erasing steps to switch from/to an intermediate polarization, enabling direct switching between the four memory states. To utilize the fabricated BPI-FeFET as a dual-logic-in-memory device, two logical operations were selected (XOR and AND), and their parallel execution was demonstrated. Different types of logic operations could be implemented by selecting different initial states, demonstrating various types of functions required for numerous neural network operations. The flexibility and efficiency of the proposed dual-logic-in-memory device appear promising in the realization of next-generation low-power computing systems.

KEYWORDS

ferroelectric field-effect transistor, in-plane ferroelectricity, logic-in-memory, out-of-plane ferroelectricity

1 | INTRODUCTION

Owing to the rapid development of the data-driven AI era, there are new challenges faced by computing hardware and systems. To address the increasing data density, reduced energy consumption and cost are required.[1] However, certain fundamental issues constrain the development of future data-centric computing devices, such as slow device scaling beyond Moore's law in Si-based integrated circuits, because of physical limitations,[2] and von Neumann bottlenecks in conventional computing systems constituting physically separated processing and memory units.[3] To reduce the time and energy consumed by data transactions between processing and memory units in traditional von Neumann architectures, many hardware architectures have been proposed that can handle the complex computations required for neural networks constituting the storage. Logic-in-memory (LIM) is a promising approach for processing data within memory; it allows for efficient logic operation by enabling parallel execution and reconfigurability of the logic implemented in memory. To realize LIM hardware, it is important to implement practical logic operations within the memory, such as those often utilized by deep neural network operations, at high densities.

Owing to their single-device information storage and computing capacities, ferroelectric field-effect transistors (FeFETs) can meet the requirements of next-generation computing systems. However, conventional ferroelectrics such as oxides[4] and perovskites[5,6] suffer from low interface quality,[7] CMOS incompatibility,[8] charge trapping,[9] and gate leakage,[10] thus limiting their success in practical device applications. Recent advances in van der Waals (vdW) layered ferroelectrics that exhibit excellent performances have attracted widespread attention. Many different categories of vdW ferroelectric materials exist, such as out-of-plane ferroelectric $CuInP_2S_6$,[11–13] 1T-WTe_2,[14] in-plane ferroelectric SnS,[15] SnTe,[16] SnSe,[17] GeS,[18] β′-In_2Se_3,[19] BA_2PbCl_4,[20] interrelated ferroelectric α-In_2Se_3,[21] and ferroelectric heterostructures.[22] Several investigations on vdW FeFETs that possess nonvolatile memories have been conducted[22–27]; however, the majority of reports focused on one-bit storage, and little attention has been paid to multilevel storage. Ferroelectric memory stores one-bit information using two saturated polarization, and the intermediate degree of polarization can be obtained by altering the positive and negative domain ratios to achieve more memory states. However, the common method to obtain an intermediate polarization by adjusting the amplitude and width of the electric pulse is not consistent, because of the stochastic and complex nature of polarization, and such large variations remain a significant challenge in this field.[28,29] Moreover, direct switching to an intermediate memory state cannot always be achieved without knowing the current state and often requires an additional erasing step, and this incurs additional time and energy consumption with extra circuit overheads.[30–33]

In addition to being a nonvolatile memory device, vdW FeFETs exhibit significant potential as a computation device, particularly for in-memory computing applications. Certain computations are performed in the memory itself, which is arranged as a computational memory unit. This eliminates energy-intensive and time-consuming data movement in current designs. Computations performed with a new device can be divided into two categories depending on the processed signals: analog (e.g., artificial synapses) and digital (e.g., nonvolatile logic gates). Many studies have reported FeFETs containing α-In_2Se_3[34–37] or SnS[38] channels and their significant potential as artificial synapses; however, nonvolatile logic gates (LIM) have received less attention. Nonetheless, realizing in-memory computing in the form of a digital logic gate can create a substantially larger potential impact on AI acceleration hardware research because current practical AI acceleration hardware requires accelerating complex digital operations for neural network operations (such as multiplication and accumulation), rather than analog synaptic operations (such as integration and fire).

Since the proposal of stateful logic by Borghetti et al.[39] in 2010, resistance has been widely studied as a physical variable, representing Boolean logic states in circuits, and has been achieved in various devices such as 2D floating-gate transistors,[40,41] charge-trapping memristors,[42,43] and ferroelectric memristors.[33] However, studies on LIM are still limited; at the device level, most of the existing LIM architectures use only two resistance states (1-bit) in the FeFET and offer a limited number of logic functions, making it challenging to implement complex logic functions. Furthermore, the LIM research still uses conventional ferroelectrics predominantly, which suffer from numerous disadvantages (as mentioned above). This limits the storage density of the LIM circuit, which is not conducive to reducing the cost per bit, thereby restricting the improvement of

LIM performance to meet the requirements of future computing systems.

In this study, we propose a distinct conceptual approach for implementing two-bit storage, which also acts as a dual-logic gate in a single, bidirectional polarization, ferroelectric field-effect transistor (BPI-FeFET) by integrating the in-plane (IP) vdW ferroelectric semiconductor SnS and the out-of-plane (OOP) vdW ferroelectric gate dielectric material $CuInP_2S_6$ (CIPS). Owing to this unique integration, in which IP and OOP exist separately in the channel and gate dielectrics, respectively, these polarizations can be independently controlled. Notably, although the α-In_2Se_3 ferroelectric semiconductor has both IP and OOP, the polarizations are simultaneously flipped, making it unsuitable for our memory and logic-in-memory applications. Four different combinations were achieved because CIPS and SnS possess two different saturated polarization states each, resulting in four resistance states (two-bit storage) in a single device. The four resistances, namely, the high resistance state (HRS), mid-HRS, low resistance state, (LRS), and mid-LRS, exhibited sufficient differences; the on/off ratio between the highest and lowest channel currents was $>10^5$. The fabricated BPI-FeFET exhibited high switching endurance ($>10^4$ cycles) and stable retention characteristics ($>10^4$ s). The mechanism for two-bit storage in a single BPI-FeFET was analyzed from two perspectives: carrier density and carrier injection controls, originating from OOP polarization of the gate dielectric and IP polarization of the semiconductor, respectively. We can separately control the polarization directions of the CIPS and SnS because the OOP polarization is only reversed by the OOP electric field, whereas the IP polarization is only reversed by the IP electric field, enabling abrupt transitions from and to states with intermediate resistances. Thus, unlike the aforementioned multilevel FeFETs that require additional pre-examination or erasing steps, in the proposed system, direct transfer between four memory states was experimentally demonstrated. The potential of the BPI-FeFET for low-cost and high-density LIM computing circuits was further explored using the two-bit nonvolatile memory that acts as a dual-logic gate: a device that can perform two logical computations (e.g., XOR and AND) in parallel. These logical computations are reconfigurable with the initial state of the device. The device performed XOR and AND in one setup and performed NAND and AND computations in parallel in different setups, implying that a single BPI-FeFET device can perform half addition (sum with XOR and carry with AND), or can be potentially extended to any Boolean function (universal logic gate NAND).

2 | RESULT AND DISCUSSION

2.1 | Fabrication and operating principle of the BPI-FeFET

Figure 1A is a schematic of the BPI-FeFET that was fabricated using ferroelectric semiconductor SnS as the channel, ferroelectric CIPS as the gate dielectric, h-BN as the insulating layer between SnS and CIPS, and SiO_2 as the gate insulating layer, with p^+–Si as the bottom gate electrode. Insertion of a h-BN layer between CIPS and SnS improves the interface quality as the leakage current is reduced, acting as a passivation layer (Figure S12). Ti/Au (10/50 nm) electrodes were deposited at both ends of the SnS as the source and drain. Figure 1B shows a transmission electron microscopy (TEM) image of the CIPS-h-BN-SnS vdW heterostructured layers. The corresponding energy dispersive X-ray spectroscopy (EDS) elemental mapping of the CIPS/h-BN/SnS heterostructure is shown in Figure S1. An optical microscopy (OM) image of the fabricated device is presented in Figure 1C. The different layers can be distinguished with the dotted lines. The thicknesses of the SnS, h-BN, and CIPS layers were approximately 11, 10, and 75 nm, respectively, measured using atomic force microscopy (Figure S2). A thick CIPS was selected to achieve a sufficient memory window. A detailed illustration on the effect of the h-BN thickness is shown in Figure S12. The mechanically exfoliated CIPS, SnS, and h-BN flakes were measured using Raman spectroscopy, using a 532 nm excitation source (Figure S3). Piezoresponse force microscopy (PFM) measurements were performed to verify the room temperature (300 K) OOP ferroelectricity in CIPS and IP ferroelectricity in SnS (Figure 1D,E). A clear hysteresis loop and phase shift of ∼180° in the PFM phase, and a well-defined butterfly curve in the PFM amplitude verify the OOP ferroelectricity in CIPS and IP ferroelectricity in SnS. The dominant polarizations of OOP in CIPS and IP in SnS were confirmed using PFM phases and amplitude profiles along the CIPS (Figure S4) and SnS (Figure S5) flakes.

Figure S6 shows the crystal structures of CIPS and SnS along with their OOP and IP polarization mechanisms. The integration of OOP ferroelectricity in the gate dielectric and IP ferroelectricity in the channel allows the channel current modulation; importantly, the OOP polarization was reversed only by the OOP electric field, while the IP polarization was reversed only by the IP electric field. Independent control of these two polarization directions allows the demonstration of two-bit nonvolatile memory using a single BPI-FeFET. By integrating two types of polarization directions (OOP ferroelectricity in the gate dielectric and IP ferroelectricity in the channel),

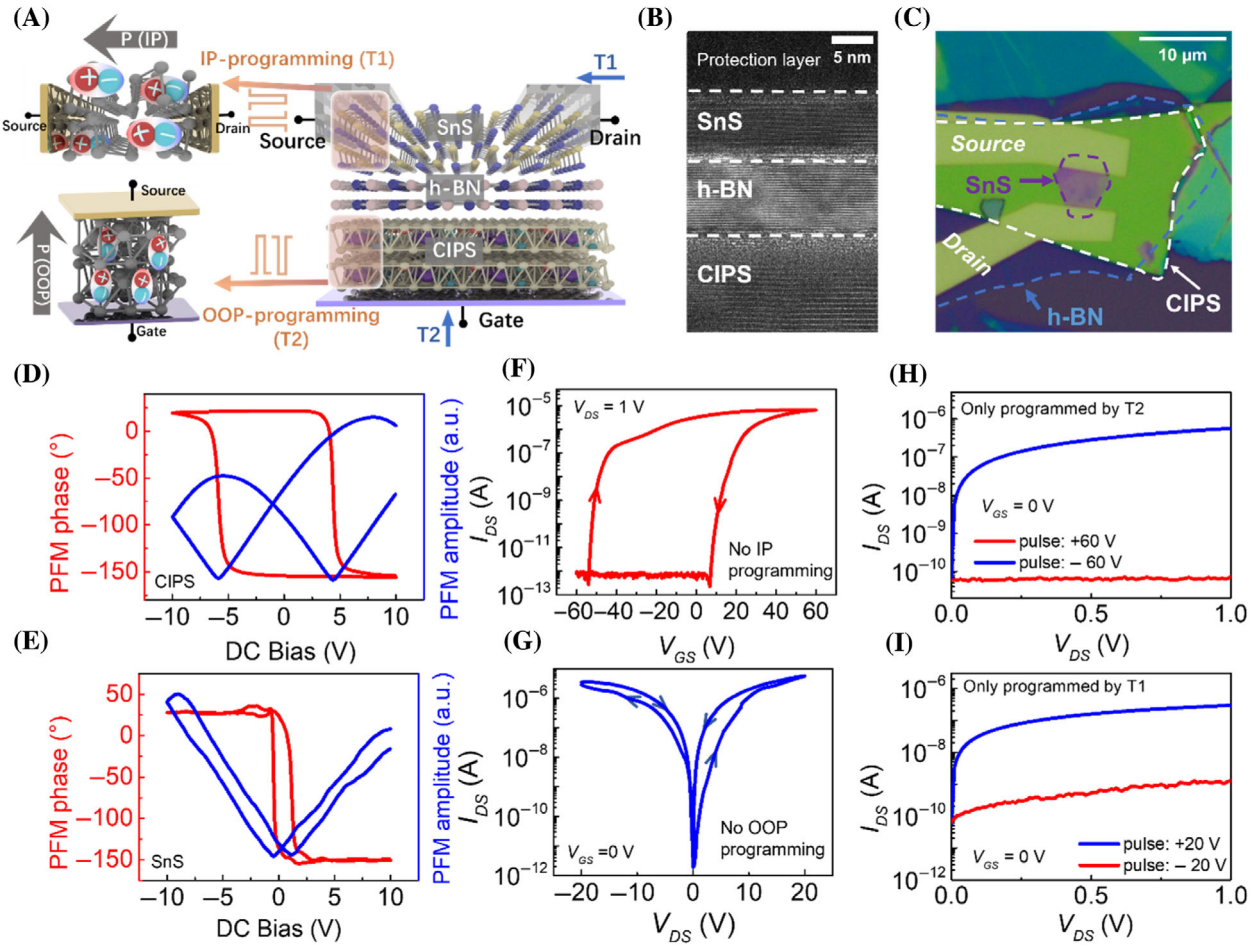

FIGURE 1 Device structure and fundamental characterization. (A) bottom gated dual-ferroelectric device structure with ferroelectric SnS as the channel material, CIPS as the ferroelectric gate dielectric, SiO_2 as the gate insulator, h-BN as an insulating layer between SnS and CIPS, p^{++}–Si as the gate terminal, and 10/50 nm Ti/Au as the source/drain terminal; (B) cross-sectional TEM image of the CIPS/h-BN/SnS heterostructure; (C) optical image of a vdW Fe-FET device based on CIPS/h-BN/SnS heterostructure; (D) PFM phase (red) and amplitude (black) hysteresis loops of a CIPS flake; (E) PFM phase (pink) and amplitude (blue) hysteresis loops of an SnS flake; (F), (G) I_{DS}–V_{GS} and I_{DS}–V_{DS} curves of the BPI-FeFET. Output characteristics for the BPI-FeFET after applying programming voltage pulses (pulse width: 1 s) only on T2 (H) and T1 (I) terminals.

and by independently controlling them, two-bit nonvolatile memory can be implemented using a single BPI-FeFET.

The I_{DS}−V_{GS} characteristics of the device are shown in Figure 1F. The gate voltage (V_{GS}) was swept from −60 to +60 V and then back to −60 V, while the drain voltage (V_{DS}) was maintained at 1 V without any programming voltage being applied across the source and drain terminals, implying that the SnS was in a fresh state. A hysteresis loop exhibiting a wide hysteresis window of 70 V and a high on/off current ratio of 10^5 was observed. A band diagram illustrating the modulation of the carrier density in the channel upon programming by the gate voltage is shown in Figure S8A. The gate current was measured to be below 10^{-10} A (Figure S7B), guaranteeing a high input impedance when used as the input to a logic gate circuit. The memory window extracted from the I_{DS}−V_{GS} curves gradually increased with increasing sweep range of the gate voltages (Figure S7A). This remarkable hysteresis resulted from the underlying CIPS layer. No appreciable hysteresis was observed in the transfer curve of the device, which employed the same configuration without an underlying CIPS (Figure S9). This is because the SnS ferroelectric dipoles were IP and no OOP dipoles were present; therefore, IP polarization can be only reversed by the IP electric field.[27] As shown in Figure S10, when we fabricated a device without an h-BN layer, hysteresis could be observed, indicating that h-BN did not act as a tunneling layer in the floating gate. As shown in Figure S11, the temperature dependence of the h-BN layer was measured, revealing that hysteresis reduced at higher temperatures, which is consistent with

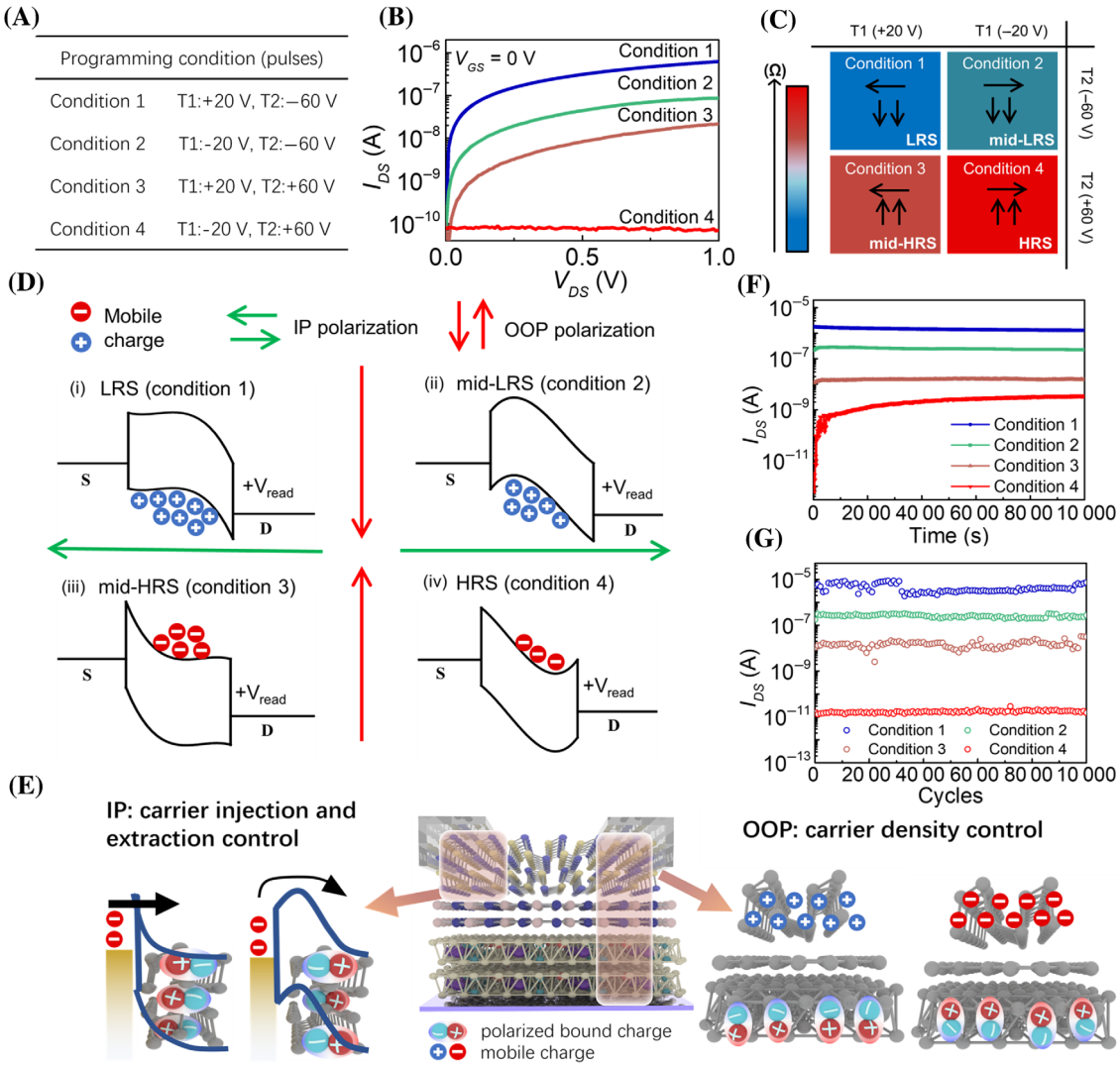

FIGURE 2 Performance of two-bit nonvolatile memory using a single 2D dual-ferroelectric FET: (A) summary of the programming conditions combining T1 and T2; (B) output characteristics of the BPI-FeFET after applying programming voltage pulses on T1 and T2; (C) map of the channel resistance levels and polarization directions regarding the different programming conditions; (D) energy band diagrams and charge carrier control regarding IP and OOP polarization; (E) retention of the four memory states after applying different programming voltage pulses, (F) endurance of the four memory states; and (G) schematic of charge density/injection control using OOP/IP polarization.

ferroelectric behavior.[44] A band diagram illustrating the modulation of the carrier density in the channel when programmed by the gate voltage and a discussion on hysteresis is shown in Figure S8A. In addition to the OOP programming using V_{GS}, the channel current can be modulated through the V_{DS} owing to the IP ferroelectricity of SnS. The $I_{DS}-V_{DS}$ characteristics presented in Figure 1G show that the channel current is modulated by the V_{DS}. V_{DS} was swept from −20 to 20 V and then back to −20 V, while the V_{GS} was maintained at 0 V, implying that CIPS was in a fresh state. The I_{DS}–V_{DS} curves for different V_{DS} sweep ranges are shown in Figure S7C. A band diagram illustrating the modulation of the Schottky barrier when programmed by the drain voltage and a discussion on hysteresis is shown in Figure S8B,C. After eliminating the programming voltages, memory states were read as the channel current under a small drain voltage. The output characteristics of the BPI-FeFET, programmed only by V_{GS} or V_{DS}, were measured in the 0–1 V V_{DS} range (1 V is lower than the coercive voltage of SnS, and polarization is not reversed). When programmed only by the V_{GS}, without any V_{DS} programming voltage (Figure 1H, i.e., OOP polarization programming), the channel resistance switching ratio was $\sim 10^4$ and the corresponding band diagram is shown in Figure S8B. When programmed only by V_{DS}, without any V_{GS} programming voltage (Figure 1I, i.e., IP polarization programming), the channel resistance switching

ratio was $\sim 10^2$ and Figure S8C shows the corresponding band diagram.

2.2 | Multibit memory with a direct transition between four states

The combination of the two types of resistance/conductance modulation widows formed through the OOP and IP polarization achieved four separate memory states. To better illustrate the two-bit memory implementation of the BPI-FeFET, a summary of the programming conditions combining T1 and T2 is shown in Figure 2A (programming pulses were simultaneously applied to T1 and T2). Figure 2B shows four nonvolatile drain current levels modulated by programming the 0–1 V V_{DS} range. The results show that the read current (channel current under a small drain voltage after removing the programming voltages) was tuned to four distinguishable levels using the four programming conditions 1–4. The four resistance/conductance levels were marked as HRS, mid-HRS, mid-LRS, and LRS; they exhibited significant differences: $I_{\text{LRS}}/I_{\text{mid-LRS}} = \sim 10$, $I_{\text{mid-LRS}}/I_{\text{mid-HRS}} = \sim 10$, and $I_{\text{mid-HRS}}/I_{\text{HRS}} = \sim 10^2$. To clarify the connection between the programming conditions and channel resistance, the channel resistance levels were mapped on different programming conditions and polarization directions of the CIPS (vertical) and SnS (lateral), and are shown in Figure 2C. The working mechanism of the two-bit storage performance of the BPI-FeFET can be explained by the carrier transport behaviors regarding OOP and IP polarization programming. Figure 2D shows the energy band diagrams after removing the programming voltages. In programming Condition 1, negative V_{GS} and positive V_{DS} were applied to T2 and T1, respectively. Holes were accumulated in the SnS channel, and the band was bent strongly upward owing to the OOP polarization of the CIPS. Hence, holes were easily injected into the SnS channel through both field and over-barrier thermionic emissions. Meanwhile, the SnS IP dipoles polarized to the left, and positively-bound charges appeared close to the source terminal, resulting in a lower Schottky barrier for hole carriers at the source–semiconductor junction, further decreasing the channel resistance. Therefore, an LRS state was formed (Figure 2D, (i)). For the mid-LRS state (Figure 2D, (ii)), the programming condition for T2 was the same as that for the LRS: holes were accumulated, and the band bent upward. The difference was that the programming condition for T1 was reversed and negatively-bound charges appeared close to the source terminal, resulting in a higher Schottky barrier that suppressed the extraction of holes. For the mid-HRS (Figure 2D, (iii)) and HRS (Figure 2D, (iv)), electrons were accumulated, and the band was bent downwards owing to the OOP polarization of the CIPS. Hence, electrons were only injected into the SnS channel through thermionic emission. Simultaneously, the SnS IP dipoles polarized to the left (right) and negative (positive) bound charges appeared close to the drain terminal, resulting in a lower (higher) Schottky barrier at the semiconductor–drain junction. This further decreased (increased) the channel resistance forming a mid-HRS (HRS) state. These explanations can be conceptually illustrated as shown in Figure 2E. The OOP (V_{GS}) programming voltage modulates the channel conductance by controlling the polarization-induced carrier density in the channel, whereas the IP (V_{DS}) programming voltage can alter band alignment between the channel and electrodes, thereby controlling the charge injection into and extraction from the channel. A retention test (Figure 2F) was performed, demonstrating that the four resistance states maintained a sufficient difference, which can be distinguished after 10^4 s. An endurance test was performed under the programming conditions, as shown in Figure 2C. All four resistance states exhibited stable endurances with insignificant variation after 10^4 cycles (Figure 2G). The obtained retention and endurance characteristics can be attributed to the suppressed depolarization effect and interface states of the device structure, suggesting that conductance perturbations through IP and OOP coupling are insignificant.

2.3 | Dual-logic-in-memory computing device

Because carrier density control is achieved by the OOP electric field, and IP polarization is reversed by the IP electric field, we can independently control both. Consequently, without any intermediate state transitions, any state can be directly converted into the other three states through a single writing step. Contrarily, conventional multibit FeFETs achieve alternative resistance states by obtaining intermediate polarization values between two saturated polarizations. Thus, an additional facile step is required when converting from saturated to intermediate polarizations, leading to additional energy and time consumption. The direct transition between the four resistance/conductance states was investigated, as shown in Figure 3. The resistance states of the BPI-FeFET are denoted as AB. A feasible digital configuration of AB is displayed in Figure 3A, where HRS, mid-HRS, mid-LRS, and LRS are encoded as "00", "01", "10", and "11", respectively. It is possible to switch between any resistance states by applying the transition rules shown in Figure 3B. For example, switching from "10" to "11"

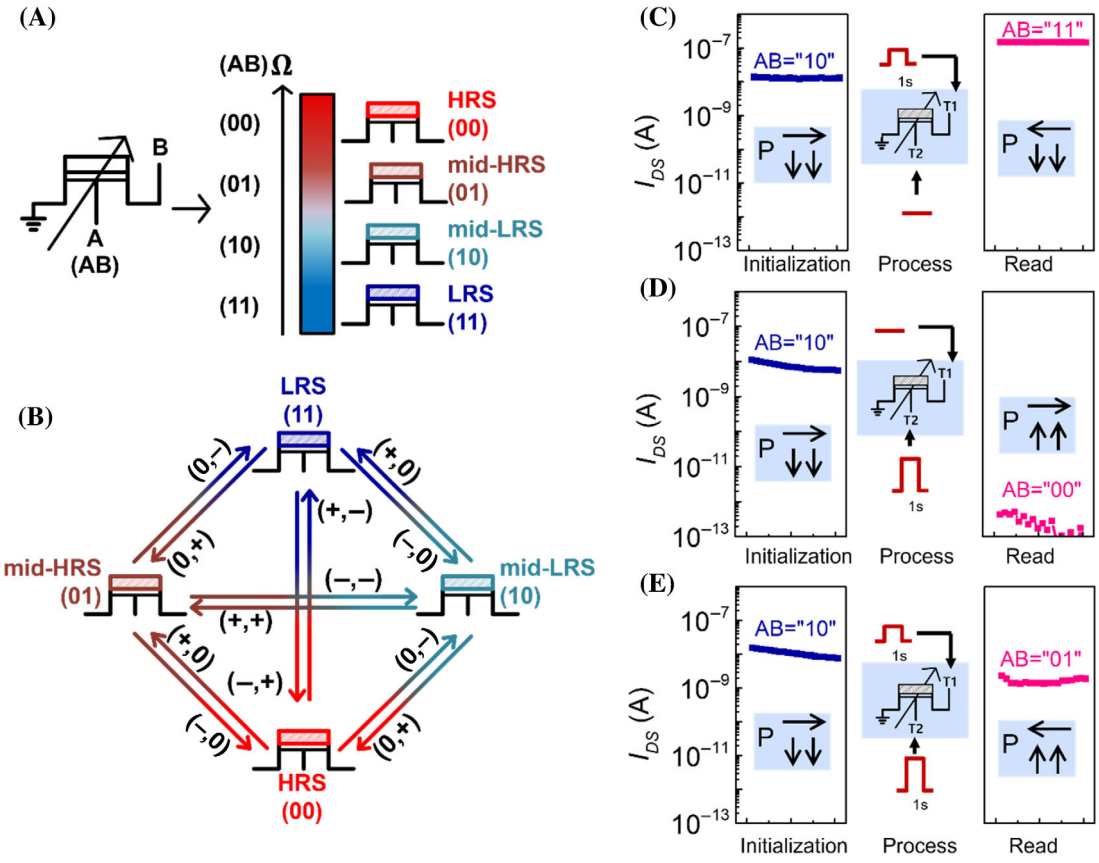

FIGURE 3 Direct transition between the four resistance/conductance states. (A) Feasible digital configuration of the resistance states for AB. (B) Schematic of the various transitions between the four resistance/conductance states. (C), (D), and (E) Experimental demonstration of the memory state transitions. Here, the initial state AB = "10" was selected as an example. Left column: initial state, middle column: the "minimum" operation required for the desired state transition, right column: final state.

requires only a positive programming pulse to be applied to T1, leaving T2 unmodified. Similarly, switching from "10" to "00" can be achieved by applying a positive programming pulse to T2. Positive pulses simultaneously applied to T1 and T2 achieve switching from "10" to "01". The experimental data for these conversion examples are shown in Figure 3C, where the left column presents the initial resistance, the middle column presents the transition process operation that includes the pulse signals applied to T1 and T2, and the right column presents the resistance state after the switching process. The experimental data for other conversion processes are shown in Figure S13. These transition rules present the "minimum" number of operations required for desired state transitions, based on the present resistance state. Unlike the earlier multistate memory implementations where the current state should be read before applying state-converting inputs,[30–32] the inputs to T1 and T2 for obtaining the desired state can be directly applied without knowing the present resistance state, as shown in Figure 2 (Conditions 1–4). This significantly simplifies the memory write process and hardware requisites because no read is required before applying the input for write, and the write input voltage does not need to be adjusted according to the current state.

Having clarified the transition rules for the four resistance states in the BPI-FeFET, its potential as a low-cost and high-storage-density LIM circuit can be explored. Ma et al.[33] demonstrated LIM in a single-multi-bit ferroelectric tunnel junction memristor cell and LIM computing in 2D FeFETs on a one-bit memory.[45–48] LIM computing realized using a two-bit 2D FeFET has not yet been investigated. The device diagram shown on the left of Figure 4A depicts the conventional concept of LIM computing in a single-one-bit FeFET.[46–48] The one-bit state initially stored in the FeFET was represented by A (initial state), logical input to the voltage signals (pulses) on the gate terminal was represented by C, and the final resistance state (after turning off the logical input signal) was read as the logical output (A'). For the proposed two-bit BPI-FeFET, a novel operation scheme for performing dual LIM computing was realized, as shown in the device diagram on the right of Figure 4A. AB represents the two-bit initial state and the logical inputs of voltage

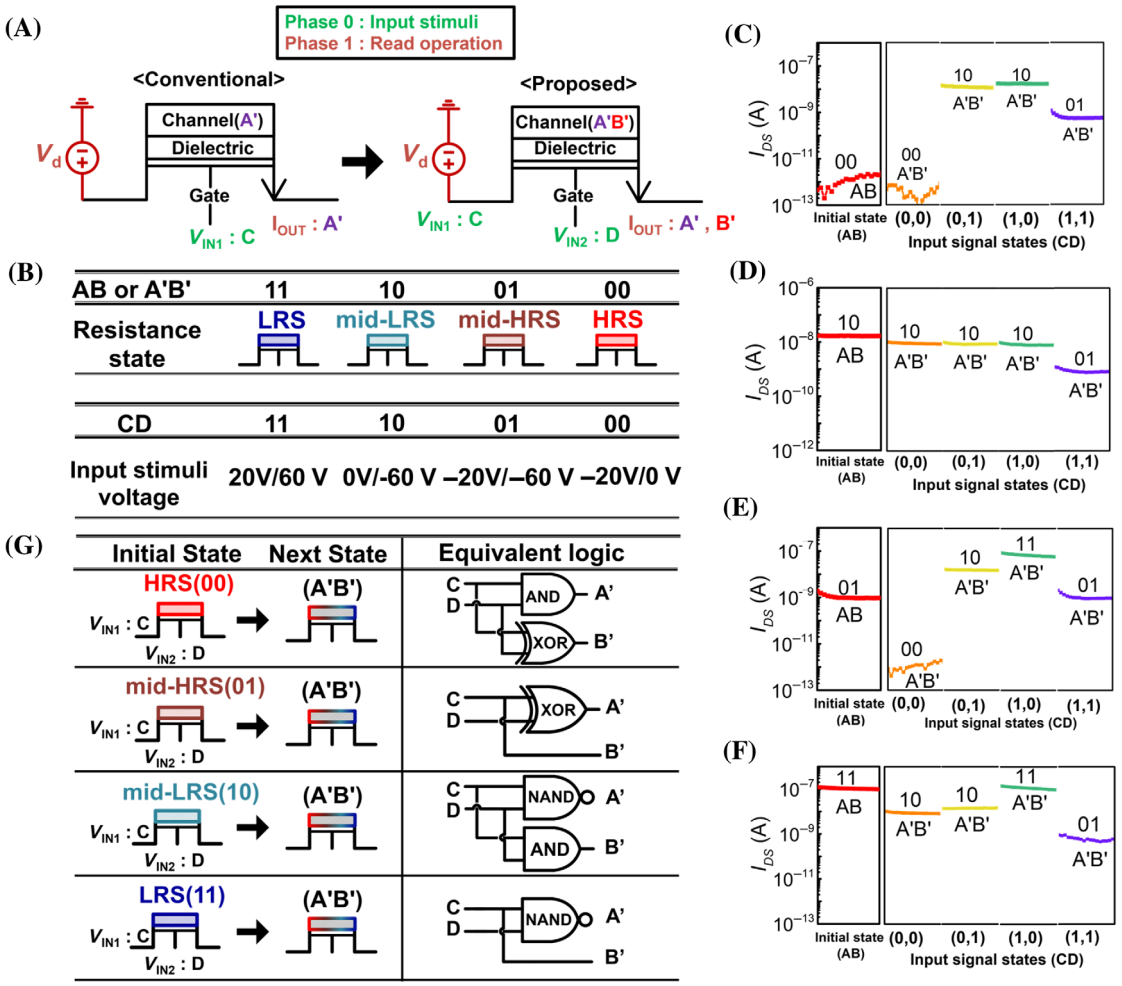

FIGURE 4 Reconfigurable and parallel logic-in-memory computing in a single BPI-FeFET. (A) Conventional method for performing logic-in-memory computing in a single one-bit FeFET (left). A newly-designed method for logic-in-memory in a single two-bit BPI-FeFET (right). (B) Feasible-digital configuration of the initial resistance/conductance state AB, final resistance/conductance state A'B' (which serves as the output signal of the logic operation), and voltage pulses for CD (which serves as the input signal of the logic operation). (C) Output resistance/conductance under different input states for parallelly executed XOR and AND logic outputs when the initial state AB is preprogrammed to "00". (D) Output resistance/conductance under different input states for parallelly executed NAND and AND logic outputs when the initial state AB is preprogrammed to "10". (E) Output resistance/conductance under different input states for parallelly executed XOR and Transfer logic outputs when the initial state AB is preprogrammed to "01". (F) Output resistance/conductance under different input states for parallelly executed NAND and Transfer logic outputs when the initial state AB is preprogrammed to "11". (G) Summary of the logic functions under different initial states.

signals (pulses) to the source (T1) and gate (T2) terminals were encoded as CD. The final resistance state, which is also two-bit, can be read as logical outputs A′ and B′. Based on the transition rules of the four-resistance states in the proposed device (Figure 3), we adopted a special encoding method for the input signal "CD". As shown in Figure 4B, "+20 V/+60 V" was encoded as "11", "0 V/−60 V" was encoded as "10", "−20 V/−60 V" was encoded as "01", and "−20 V/0 V" was encoded as "00". Experimental demonstrations of the device states after the application of different combinations of C and D input pulses are plotted in Figure 4C–F. For this measurement, a programming step was performed to set the different initial states. Subsequently, input signals for C and D were applied, and finally, the logic outputs were read as the channel current/resistance under a small drain voltage (all the read voltages were 1 V) after turning off the input signals. When the initial state was set as AB = "00" (Figure 4C), the output resistance/conductance under different input states simultaneously executed XOR and AND logic operations, that is, $A' = C \oplus D$ (logic XOR function) and $B' = CD$ (logic AND function). This configuration enables the implementation of a half adder using a single BPI-FeFET

device, where B′ is the carry output and A′ is the summation output of the half adder with inputs C and D. Figure S14A shows the truth table of the logic operation presented in Figure 4C. Various other logic operations were performed by configuring AB with different initial states. For example, when the initial state was set to AB = "10" (Figure 4D), the logic operation of NAND and AND can be simultaneously performed in parallel as $A' = \overline{C \wedge D}$ (logic NAND function) and B′ = CD (logic AND function). The truth table for this logic operation is shown in Figure S14C. Notably, a functionally complete NAND gate was thus achieved, implying that our logic can be extended to any Boolean function. This would also potentially enable an energy-efficient and dense AI accelerator using an array of BPI-FeFET devices for large, parallel execution of multiple (logical AND), and accumulation (addition of XOR and AND operations) operations that are required in neural network operations for AI acceleration. Additional configurations also add flexibility to the type of logic that can be implemented using the BPI-FeFET devices. For example, when the initial state was set to AB = "01", the outputs were $A' = C \bigoplus D$ and B′ = C (Figure 4E), and when the initial state was set to AB = "11", the outputs were $A' = \overline{C \wedge D}$ and B′ = C (Figure 4F). The truth table for these two logic operations is presented in Figure S14B,D. The logical functions under different initial states are shown in Figure 4G. Further, the effectiveness and flexibility of this multibit LIM strategy can be improved using a multiencoding method. Figure S15 shows an example; a different definition of the input signal CD is shown in Figure S15A. In this setting, the logical functions were changed (Figure S15B), and functionally complete NAND and NOR gates were achieved, implying that our logic can be extended to any Boolean function. Table S1 compares the key characteristics and performances of the LIM devices reported in this study, demonstrating the flexibility and efficiency of the proposed dual-logic-in-memory devices utilizing bidirectional polarization integration.

3 | CONCLUSION

In summary, multilevel memory and logic-in-memory in CIPS/h-BN/SnS vdW ferroelectric heterojunctions were demonstrated by integrating the IP and OOP ferroelectricities. For multilevel memory, four resistance states (two-bit storage) were achieved in a single device by combining two different saturated polarization states existing in the OOP ferroelectric CIPS and IP ferroelectric SnS. The four resistance states exhibited sufficient resistance differences; the on/off ratio between the highest and lowest channel currents was $>10^5$, allowing for small deviations during the read and write operations. In addition, high switching endurance ($>10^3$ cycles) and stable retention characteristics ($>10^3$ s) were achieved. Furthermore, the two-bit storage mechanism is discussed in terms of two degrees of freedom that can be controlled in a single BPI-FeFET-carrier density in the channel and band alignment between the channel and electrodes. Such multilevel memory performances can be also achieved using other possible combinations of OOP gate-dielectrics and IP semiconducting materials. Moreover, unlike indirect conversion in conventional multilevel ferroelectric memory, direct conversion between the four-memory states (two bits) in the proposed device was experimentally demonstrated. For in-memory computing, Boolean logic was designed in two-bit FeFET memory. In the fabricated BPI-FeFET, the two-bit nonvolatile memory can simultaneously perform two logical computations (XOR and AND). Furthermore, these logical computations are reconfigurable when the initial state of the device is set to a different resistance value. The results not only suggest significant potential for improving the storage density and reducing the cost per bit in a logic-in-memory circuit but also demonstrate that the integration of vdW OOP ferroelectric dielectrics with IP ferroelectric channels is promising for future information storage and electronic computing applications.

4 | EXPERIMENTAL SECTION

4.1 | Device fabrication

Bulk SnS and h-BN were purchased from 2D semiconductors and bulk CIPS was purchased from HQ graphene. After mechanical exfoliation, thin flakes of CIPS, h-BN, and SnS were transferred onto a 285 nm Si/SiO_2 wafer. The source and drain electrodes were patterned using electron beam lithography, followed by deposition of Ti/Au (10 nm/50 nm) using e-beam evaporation.

4.2 | Device and material characterization

An optical microscope (Olympus, BX51M) was used to confirm the sizes and shapes of the flakes and devices. The thickness of the thin flakes was measured using atomic force microscopy (AFM; Park-NX10, M/s Park Systems Corp.) in noncontact mode. Standard piezoelectric force microscopy (PFM) was performed using the aforementioned AFM system in contact mode.

A conductive tip containing a Cr/Pt coating was employed (Multi75E-G, BudgetSensors, tip radius = 25 nm, spring constant $k \approx 3\ \mathrm{Nm}^{-1}$, resonance frequency $f \approx 75$ kHz). The frequency and amplitude of the alternating voltage Vac for the OOP and IP PFM characterization studies were 17 kHz and 4 V, respectively. OOP polarization was estimated by tracking the vertical cantilever deflection, while IP polarization was determined from the lateral torsion of the cantilever. Local piezoresponse hysteresis loops were collected using a combination of changing DC bias and 4 V AC bias. The entire electrical characterization was performed at room temperature (300 K) using a Keithley 4200 semiconductor characterization system (M/s Tektronix Inc.), while the device was placed inside a probe station under vacuum. Raman spectroscopy was performed using a Raman spectrometer (WITEC Alpha 300 M) equipped with a 532 nm laser. Cross-sectional TEM (JEOL, JEM ARM 200F) measurements were conducted for structural analysis.

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CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

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SUPPORTING INFORMATION

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