Research Article Vol. 34, No. 11 / 1 Jun 2026 / Optics Express 20833
Optics EXPRESS

56-Gb/s 3D-integrated silicon optical transmitter based on micro-transfer printing

TINUS PANNIER,[1,†,*] HE LI,[2,†] YE GU,[1] XIN WANG,[1] PRASANNA RAMASWAMY,[3] RUGGERO LOI,[3] PATRICK HEISE,[4,5] SENBIAO QIN,[2] BIWEI PAN,[2] JING ZHANG,[2] NEHA SINGH,[6] DIETER BODE,[6] DIMITRIOS VELENIS,[6] JORIS VAN CAMPENHOUT,[6] GÜNTHER ROELKENS,[2] AND PETER OSSIEUR[1]

[1]*IDLab, Dept. of Information Technology, Ghent University - imec, Technologiepark-Zwijnaarde 126, 9052 Ghent, Belgium*
[2]*Photonics Research Group, Dept. of Information Technology, Ghent University - imec, Technologiepark-Zwijnaarde 126, 9052 Ghent, Belgium*
[3]*X-Celeprint Ltd., Cork, Ireland*
[4]*IHP - Leibniz Institute for High Performance Microelectronics, 15236 Frankfurt (Oder), Germany*
[5]*Technical University of Applied Sciences Mittelhessen, 35390 Gießen, Germany*
[6]*imec, Kapeldreef 75, 3001 Leuven, Belgium*
[†]These authors contributed equally to this work.
[*]*tinus.pannier@ugent.be*

Abstract: We present an optical transmitter consisting of a SiGe BiCMOS driver amplifier heterogeneously integrated through micro-transfer printing onto a silicon photonic chip that contains a Mach-Zehnder modulator (MZM) and optical couplers. The driver has a footprint of only 200 µm × 300 µm, and features small bond pads of 20 µm × 20 µm. It was fabricated using a modified SiGe BiCMOS on SOI process to enable the release process prior to micro-transfer printing. The post-print metallization process to contact the EIC with the PIC consists of spin coating a layer of divinylsiloxane-bis-benzocyclobutene (DVS-BCB) to create a ramp to overcome the 20 µm step height, after which a gold metal layer is deposited to connect the driver to the MZM. To verify the operation of the optical transmitter, a high-speed measurement setup is used to capture eye diagrams. The 3D-integrated transmitter achieves 56 Gb/s non-return to zero (NRZ) with a 5-tap feed-forward equalizer (FFE) and 28 GBd 4-level pulse amplitude modulation (PAM-4) with a 5-tap FFE and nonlinearity pre-compensation, both at a total transmitter power efficiency of 9.1 pJ/bit. Integration through micro-transfer printing offers the possibility of greatly increasing scalability and fabrication throughput of short-reach optical transceivers for data centers.

1. Introduction

The continuous development of artificial intelligence is putting huge demands on data center infrastructure. To cope with the enormous I/O bandwidth requirements of thousands of computational nodes, data centers are turning to optical interconnects to bridge ever shorter distances. The high-speed optical interconnect market is dominated by pluggable modules (mostly using QSFP-DD and OSFP form factors), providing 800 Gigabit Ethernet connectivity, with 1.6 Terabit Ethernet (1.6 TbE) currently under development [1]. To meet the requirements of 1.6 TbE and beyond, optical transceivers need to rely on various technology platforms (such as CMOS, SiGe BiCMOS, InP, silicon photonics, thin-film lithium niobate, etc.) to maximize the performance of each electronic or photonic subsystem. However, the co-integration of these electronic and photonic circuits is of critical importance to overall transceiver performance and

#586228 https://doi.org/10.1364/OE.586228
Journal © 2026 Received 1 Dec 2025; revised 10 Mar 2026; accepted 15 Mar 2026; published 29 May 2026

Optics EXPRESS

scalability, and has led to significant research interest in monolithic [2–6] and heterogeneous integration approaches [7–11].

Monolithic integration has the advantage of natively providing both electronic and photonic devices in the same process [2,3], and is therefore frequently regarded as the ultimate integration approach. It offers the possibility of designing compact electronic-photonic integrated circuits (EPICs) with short interconnections, enabling high-bandwidth optical transceiver front-ends [4–6]. However, monolithic platforms offer only a limited choice of materials, with little flexibility to pick and choose dedicated electronic and photonic technologies. Moreover, each new generation requires dedicated development of such a monolithic platform with limited applications beyond that generation of transceivers, a route that may be cost prohibitive [12].

Conventionally, optical transceiver assemblies have relied on wire bonding to interconnect electronic and photonic chips. However, the bandwidth required by recent generations of optical transceivers has moved to a point where high-speed performance is limited by bond wire parasitics. Moreover, wire bonding is an inherently sequential process, and because optical transceivers can require thousands of bond wires [13], more scalable solutions with less parasitics are required. Shorter interconnect can be obtained by directly mounting the EIC on top of the PIC using flip-chip integration [7,8,11]. In this approach, the PIC presents itself as an interposer for the optical transceiver assembly. Research has mainly focused on silicon photonics interposers [11,14] because of the scalability advantages offered by the platform. However, during flip-chip integration, dies need to be diced and handled individually [9], making the process sequential in nature, hence more advanced massively parallel integration processes are required to reduce cost and scale up fabrication throughput of short-reach optical transceivers.

One approach that has the potential to offer massively-parallel heterogeneous integration on wafer scale is micro-transfer printing [10]. This emerging technology has been successfully demonstrated to bring non-native materials and functionality to silicon and silicon nitride platforms [9]. The approach does not rely on the handling of individual dies, instead, components (referred to as coupons or chiplets) can be released from the source wafer and transferred to the target wafer in parallel. Moreover, micro-transfer printing is compatible with a wide range of materials and technology platforms, as long as the source wafer can be designed to accommodate the necessary sacrificial layer and tethering system for release processing, and the target substrate is locally flat [15]. Because micro-transfer printed components can be very thin ($\sim 10\,\mu m$) and printed with $<1.0\mu m$ 3σ alignment accuracy [16], electrical connections can be made using a photolithographic metallization process, allowing for much smaller bond pads ($20\,\mu m \times 20\,\mu m$ or even less), and as a result, much smaller parasitic capacitance.

This paper is a continuation of [17–19] and utilizes a further developed micro-transfer printing process to realize a 3D heterogeneously integrated optical transmitter consisting of a SiGe BiCMOS driver and a silicon photonics MZM. To the best of our knowledge, this is the first demonstration of an optical transmitter EPIC using micro-transfer printing. The transmitter achieves 56 Gb/s NRZ with a 5-tap FFE and 28 GBd PAM-4 with a 5-tap FFE and nonlinearity pre-compensation.

An overview of the 3D-integrated optical transmitter and its design is presented in Section 2, after which Section 3 covers the details of the fabrication process, including micro-transfer printing and metal contacting. Subsequently, high-speed measurement results of the fabricated device are provided in Section 4. Finally, Section 5 concludes this paper.

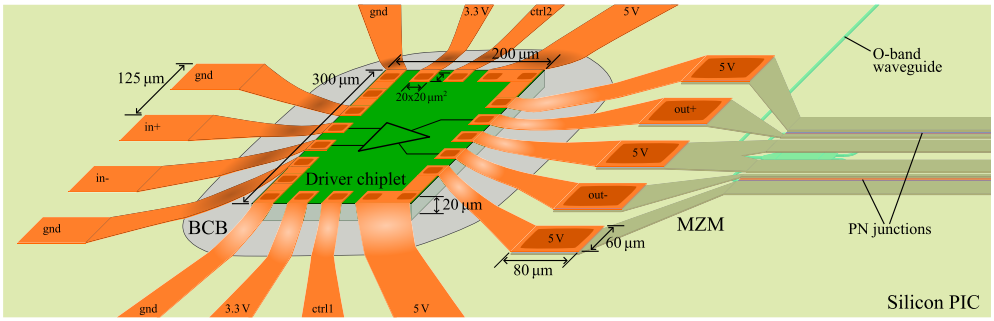
2. Design

2.1. EPIC design and fabrication

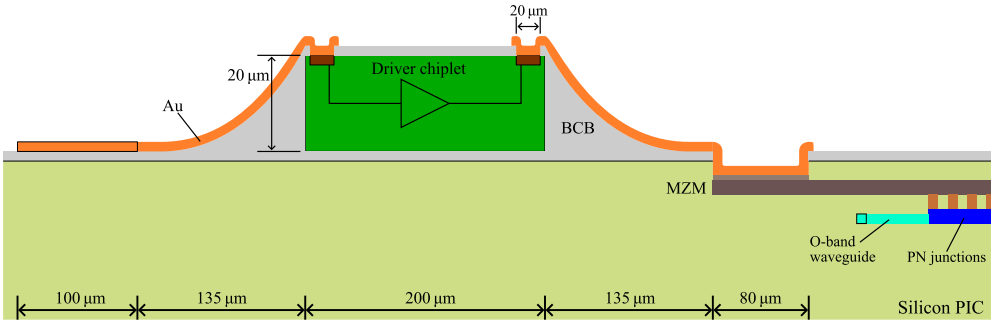
A drawing of the transmitter EPIC design is shown in Fig. 1. A $20\,\mu m$ thin, $200\,\mu m \times 300\,\mu m$ footprint SiGe BiCMOS driver chiplet was released from its silicon-on-insulator (SOI) source wafer and micro-transfer printed onto a silicon PIC, where it is connected to a depletion-type

Optics EXPRESS

MZM using a photolithographic gold (Au) metallization process. Since the design is intended for data center applications, it is optimized for operation in the O-band (1310 nm). DVS-BCB has been spin coated on the PIC as an adhesive layer before printing, and again after printing to create a ramp around the chiplet to overcome the 20 µm step. The driver is placed about 135 µm from the MZM for the formation of the ramp, but this distance could be decreased by further process optimization. The micro-transfer printing approach allows to greatly reduce the size of bond pads, resulting in considerably less parasitic capacitance. The bond pads on the driver chiplet measure only 20 µm × 20 µm, and electromagnetic simulations show that their parasitic capacitance is only 4.75 fF. For the current process (discussed in Section 3), measurements using DC probe tips show that the contact resistance between the chiplet bond pads and the gold interconnections is typically around 2 Ω, with outliers below 4 Ω. In this prototype design, a conventional MZM with regularly sized bond pads (80 µm × 60 µm) suitable for probing or wire bonding is used, but a dedicated micro-transfer printing design with smaller bond pads can further reduce interconnect parasitics. The inputs of the driver chiplet are fanned out to 125 µm pitch to accommodate a high-speed GSSG probe. The driver EIC requires 3.3 V and 5 V supplies, and can be controlled by writing to a 4-bit shift register using two low-frequency control signals. The DC and low-frequency connections are fanned out and routed away from the EIC for wire bonding to a printed circuit board (PCB).



(a) 3D interpretation



(b) Cross section

Fig. 1. A drawing of the prototype transmitter EPIC: a driver chiplet has been micro-transfer printed onto a silicon PIC and connected to a MZM.

A micrograph of the fabricated design is shown in Fig. 2. The driver chiplet was accurately aligned during transfer printing and sits on top of the silicon PIC's surface. The subsequently applied gold (Au) metallization is clearly visible in the image, where relevant dimensions concerning the driver EIC have been indicated. The MZM has a length of 2 mm and is electrically terminated by on-chip termination resistors. Optical biasing is achieved by controlling the

Optics EXPRESS

thermo-optic phase shifters (heaters). To reduce coupling losses, openings were etched in the DVS-BCB to expose the input and output fiber grating couplers (FGCs), as well as to access the metal bond pads. The silicon PIC was fabricated in imec's iSiPP300 technology platform [20].

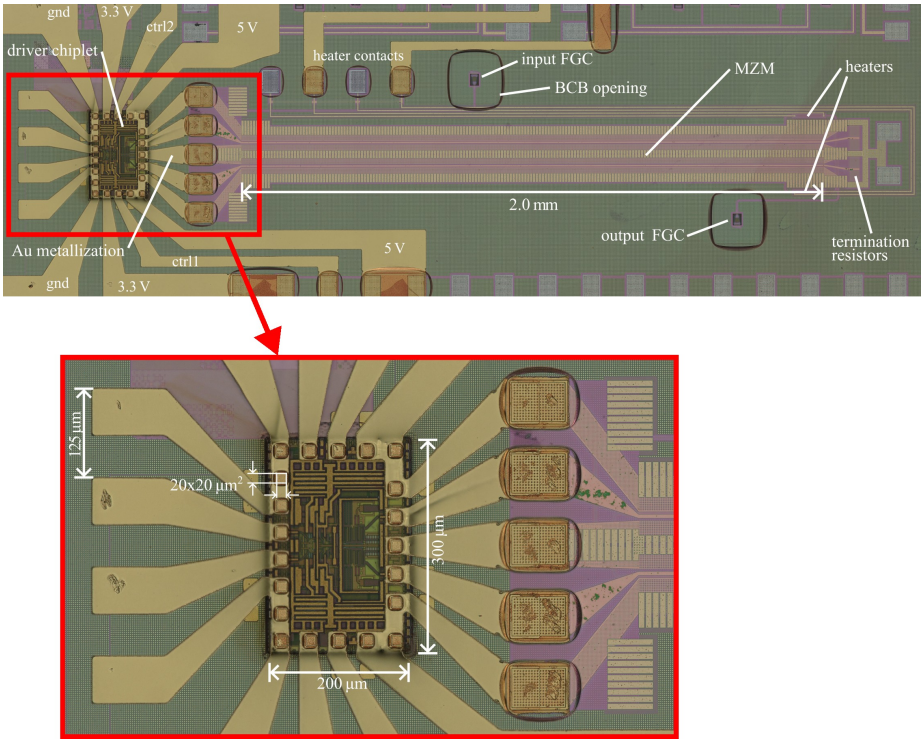


Fig. 2. Micrograph of the fabricated design. The 20 µm thin driver EIC sits on top of the PIC's surface.

2.2. SiGe BiCMOS driver design

Both the driver EIC and the MZM are designed to operate in a 50 Ω environment for maximum flexibility, even though the compact integration of driver and modulator allows for a more customized choice of impedance level. The MZM termination resistors are sized at 30 Ω to increase the electro-optical modulator bandwidth [21]. The MZM matches the driver's pad layout, such that the PN junctions are reverse-biased through the driver via a compact DC-coupled connection. To balance modulator bandwidth against optical modulation amplitude (OMA), a modulator length of 2 mm was chosen, resulting in a specified V_π of 6 V. The driver EIC was designed in a 130 nm SiGe BiCMOS process, and fabricated on SOI wafers (instead of bulk silicon) to allow the release processing of coupons from the source wafer for micro-transfer printing [17]. The circuit schematic of the driver amplifier connected to the MZM is shown in Fig. 3. The driver consists of a differential pair input stage (Q1), two emitter follower (EF) stages (Q2-Q3), and a cascoded differential pair output stage (Q4-Q5). The small 200 µm × 300 µm chiplet footprint does not allow to include a complete digital controller, so a more compact 4-bit shift register is implemented instead to control the bias currents of the four amplifier stages. Data can be written to the shift register by applying the desired bit sequence and a clock signal to the ctrl1 and ctrl2 contacts, respectively. In this design, the small footprint also does not allow the use of on-chip inductors for inductive peaking. ESD protection diodes were put in place underneath the 20 µm × 20 µm bond pads to save design area. The output stage includes a 150 fF

Optics EXPRESS

capacitor at the base of the cascode transistor Q5 to prevent potential breakdown of this device by equally distributing the voltage swing over both transistors Q5 and Q4 [22]. Additionally, a 6 Ω degeneration resistor was added to improve linearity. The low-frequency maximum peak-to-peak differential voltage swing that can be generated by the output stage at the input of the MZM is given by

$$V_{max,ppd} = 2\, I_{tail}\, \frac{R_c(R_m + R_t)}{R_c + R_m + R_t} \tag{1}$$

where I_{tail} is the output stage tail current, $R_c = 50\Omega$ is the resistor at the collector of Q5, $R_m = 12\Omega$ is the metal series resistance of the 2 mm modulator transmission line (which could be reduced by making efficient use of the available metal layers in the silicon photonics platform), and $R_t = 30\Omega$ is the modulator termination resistor. The output stage tail current I_{tail} is set to 53 mA, resulting in a maximum voltage swing of $2.4V_{ppd}$ at the input of the modulator, and a 0.6 V reverse bias of the MZM PN junctions. Including all bias circuits (not shown), the driver draws 41 mA and 74 mA from the 3.3 V and 5 V supplies, respectively, resulting in a total driver power consumption of 505 mW.

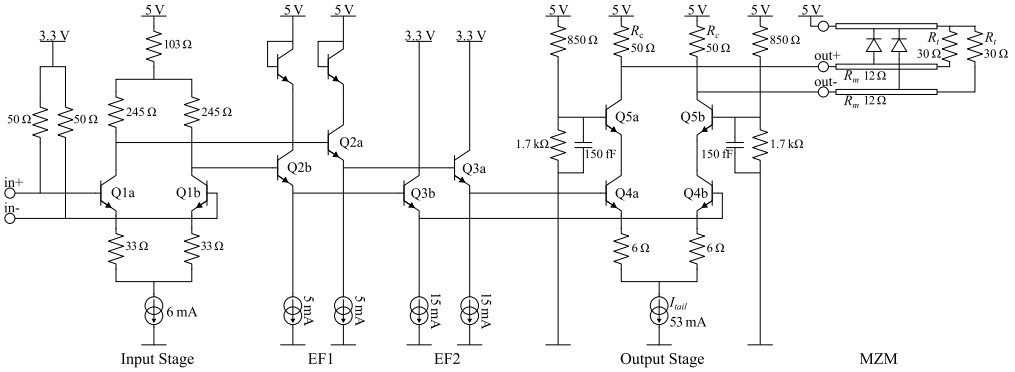


Fig. 3. Schematic of the driver connected to the MZM.

3. Processing

The driver EIC was designed in a 130 nm SiGe BiCMOS process, and fabricated by IHP on SOI instead of bulk silicon. Subsequently, the EIC chiplet is processed by X-Celeprint to enable its release from the source wafer for micro-transfer printing. This release process is illustrated in Fig. 4. The singulation of the chiplets to the buried oxide (BOX) layer and the definition of the encapsulation patio is achieved by lithography and inductively coupled plasma (ICP). After this, the chiplets are fully encapsulated in a dielectric. With all the tethers defined, the chiplets can then be released with wet etch undercut by tetramethylammoniumhydroxide (TMAH) [17].

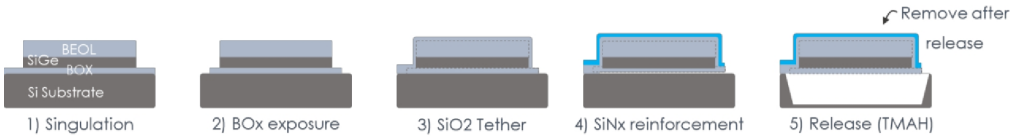


Fig. 4. The process steps to encapsulate the EICs, add tethers and release them from the native substrate. Figure from [17].

The process of micro-transfer printing and post-printing metallization is illustrated in Fig. 5. Before printing, the silicon PIC undergoes a wet cleaning process utilizing acetone, isopropyl

Optics EXPRESS

alcohol (IPA), and deionized (DI) water. Subsequently, lithography and lift-off are carried out for the deposition of titanium/gold (Ti/Au) as alignment markers for micro-transfer printing, and to contact the aluminum bond pads on the silicon PIC. After another wet cleaning process and oxygen plasma cleaning, a layer of AP3000 is spin-coated, followed by a thin layer of spin-coated DVS-BCB for the adhesion of transfer printed coupons. The DVS-BCB layer undergoes an initial soft bake at 150°C for 15 min. The driver is then micro-transfer printed, and the DVS-BCB is fully cured in a vacuum oven at 200°C. Another DVS-BCB layer is applied and cured to cover the 20 µm coupon step. Lithography and dry etch are performed to open vias over the contact pads and FGCs, followed by a second Ti/Au metal layer for interconnection. The contact resistance between the 20µm × 20µm coupon bond pads and the gold interconnection is typically around 2 Ω, with outliers below 4 Ω (measured using DC probe tips). Contact resistance could be reduced by further process optimizations, or by employing an aluminum-based metallization process with a pre-sputtering treatment on the contact pads, with which sub-ohm connections have been realized [19].

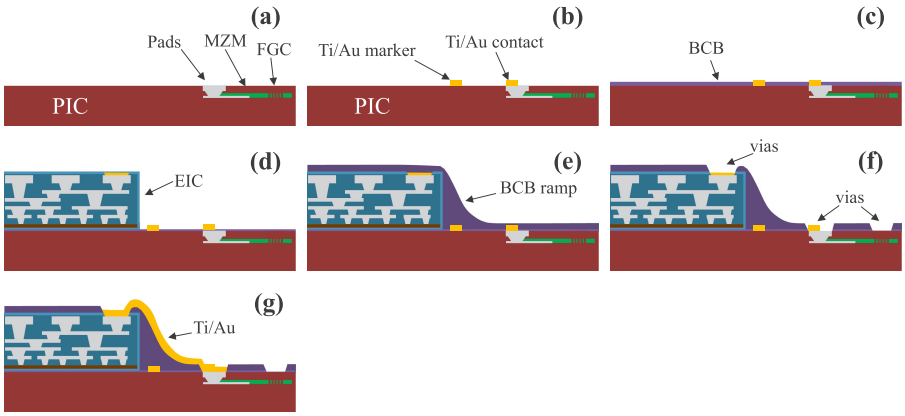


Fig. 5. Process flow for the heterogeneous integration of the driver EIC onto the silicon PIC: (a) silicon PIC preparation, (b) Ti/Au deposition, (c) spin coating of DVS-BCB, (d) micro-transfer printing of driver EIC, (e) DVS-BCB ramp formation, (f) open vias, (g) Ti/Au metallization.

Following the post-printing metallization process, the PIC is diced to match the dimensions of the PCB and then attached to the metal base using silver epoxy. After the epoxy has been cured, wire bonding is performed to connect the DC and control signal pads to the PCB for easier measurement. As RF probes are used to connect the driver input, high-speed wire bonds are not required.

4. Measurement setup and results

The performance of the optical transmitter EPIC, mounted on a PCB, is verified using the measurement setup shown in Fig. 6. A 1310 nm (O-band) 13 dBm continuous wave laser is coupled into the silicon MZM by aligning the polarization to the TE mode of the input grating coupler using an external polarization controller (PC). The output of the MZM is coupled into a fiber probe and connected to an A/B switch to easily monitor the alignment of the fiber probes with very low loss. A praseodymium-doped fiber amplifier (PDFA), in conjunction with an optical tunable filter (OTF) (set to 2 nm optical bandwidth), is used to first amplify and then filter the transmitter output signal. The average power level at the high-speed photodetector (XPDV3120R) is controlled by a variable optical attenuator (VOA) and is set to 9 dBm. The photodetector is connected directly to the 70 GHz remote sampling head of the sampling oscilloscope (Keysight

Optics EXPRESS

DCA-X). At the electrical input side, a high-speed data pattern (NRZ or PAM-4, both from a PRBS9 bit sequence) is generated by the arbitrary waveform generator (AWG) (Keysight M8196A) and applied to the input of the driver using a GSSG RF probe.

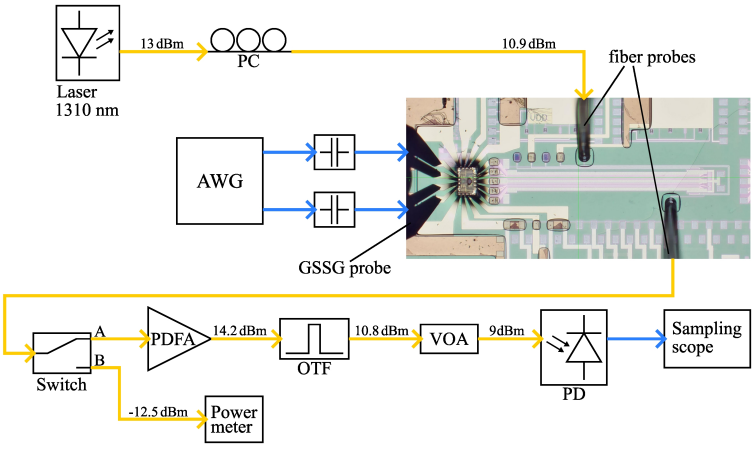
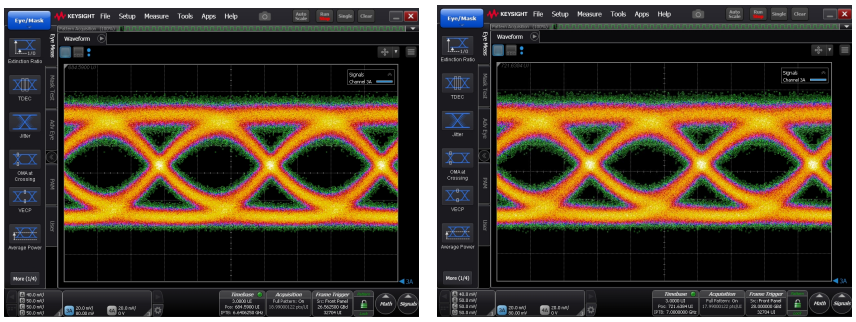


Fig. 6. Measurement setup. The annotated average optical power levels are for QP biasing.

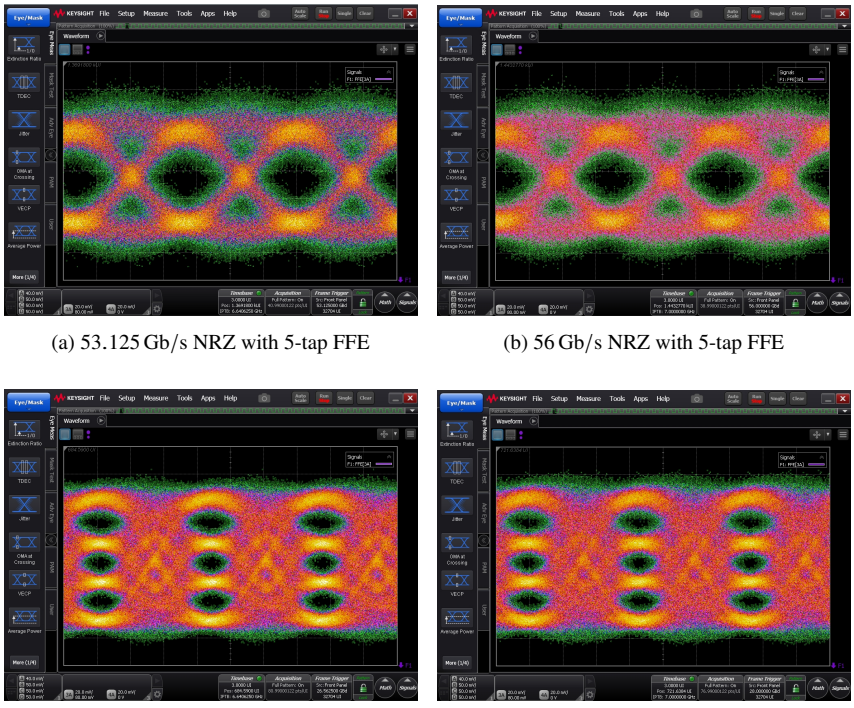
The MZM is biased at quadrature point (QP) using the heaters (consuming around 30 mW) on the PIC, and a low-frequency data pattern is applied to the EIC's shift register to set the bias currents throughout the driver. In the chosen configuration, the driver draws 39 mA and 70 mA from the 3.3 V and 5 V supplies, respectively, totaling a driver power consumption of 480 mW. These currents are slightly lower than expected (39 mA vs. 41 mA and 70 mA vs. 74 mA), possibly due to a small voltage drop over the supply nets of the transmitter EPIC. The AWG was calibrated to compensate for the losses of the cables between the AWG and the GSSG probe, and is set to a signal amplitude of $500mV_{ppd}$ for NRZ and $400mV_{ppd}$ for PAM-4. Under these circumstances, the signal amplitude at the modulator input is expected to be close to $2.4V_{ppd}$. In the case of PAM-4, pre-distortion was applied to compensate driver nonlinearity and equalize the outer and center eye heights. The average optical power levels throughout the measurement setup are annotated in Fig. 6 for QP biasing. The transmitted signals are captured using the sampling oscilloscope. Eye diagrams for 26.5625 Gb/s NRZ and 28 Gb/s NRZ (without any receiver side equalization) are shown in Fig. 7. The transmitter reaches an extinction ratio (ER) of 3.44 dB for 26.5625 Gb/s NRZ. Using a 5-tap FFE at the sampling oscilloscope, the transmitter EPIC achieves up to 56 Gb/s NRZ and 28 GBd PAM-4 operation. These results are presented in Fig. 8. Considering a total transmitter power consumption of 510 mW (including driver and heaters), this corresponds to 9.1 pJ/bit.

Optics EXPRESS



(a) 26.5625 Gb/s NRZ (b) 28 Gb/s NRZ

Fig. 7. Eye diagrams captured with the sampling oscilloscope without any receiver side equalization.



(a) 53.125 Gb/s NRZ with 5-tap FFE (b) 56 Gb/s NRZ with 5-tap FFE

(c) 26.5625 GBd PAM-4 with 5-tap FFE and nonlinearity pre-compensation (d) 28 GBd PAM-4 with 5-tap FFE and nonlinearity pre-compensation

Fig. 8. Eye diagrams captured with the sampling oscilloscope.

5. Conclusion

We successfully demonstrated a high-speed optical transmitter, relying on micro-transfer printing to heterogeneously integrate a SiGe BiCMOS driver amplifier with a silicon photonics MZM. To the best of our knowledge, this is the first demonstration of an optical transmitter EPIC based on micro-transfer printing. After fabrication, the performance of the 3D-integrated device was verified using a high-speed measurement setup. Eye diagrams were captured for 56 Gb/s NRZ using a 5-tap FFE, and 28 GBd PAM-4 using a 5-tap FFE and nonlinearity

Optics EXPRESS

pre-compensation. Heterogeneous integration using micro-transfer printing offers the prospect of increasing fabrication throughput and scalability of high-speed optical transceivers for data centers. The design of the transmitter could be further improved by optimizing the process to reduce the 135 µm horizontal length of the DVS-BCB ramps, and to reduce contact resistance. A dedicated MZM design with smaller bond pads will also reduce interconnect parasitics and result in a more compact overall design.

Funding. Research Foundation - Flanders (1SB7720N, 1SB7722N); Horizon Europe (CALADAN 825453).

Acknowledgment. The authors would like to thank Jakob Declercq for wire bonding, and Elif Özçeri İyikanat, Peter Geerinck, Steven Verstuyft, Ali Uzun, and Liesbet Van Landschoot for their assistance with coating, metallization, and characterization.

Disclosures. The authors declare no conflicts of interest.

Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

References

1. Ethernet Alliance, "Ethernet Roadmap 2025," (2025). www.ethernetalliance.org.
2. S. Lischke, D. Knoll, L. Zimmermann, *et al.*, "Photonic BiCMOS Technology — Enabler for Si-Based, Monolithically Integrated Transceivers Towards 400 Gbps," in *2016 46th European Microwave Conference (EuMC)*, (2016), pp. 1385–1388.
3. M. Rakowski, C. Meagher, K. Nummy, *et al.*, "45nm CMOS - Silicon Photonics Monolithic Technology (45CLO) for next-generation, low power and high speed optical interconnects," in *Optical Fiber Communication Conference (OFC) 2020*, (Optica Publishing Group, 2020), pp. T3H.3.
4. Y. Jo, M. Oberon, A. Peczek, *et al.*, "Novel Monolithic All-Silicon Coherent Transceiver Sub-Assembly Based on Ring Modulators," J. Lightwave Technol. **42**(20), 7298–7306 (2024).
5. U. Koch, C. Uhl, H. Hettrich, *et al.*, "A monolithic bipolar CMOS electronic–plasmonic high-speed transmitter," Nat. Electron. **3**(6), 338–345 (2020).
6. G. Movaghar, V. Arrunategui, J. Liu, *et al.*, "A Monolithic O-Band Coherent Optical Receiver for Energy-Efficient Links," IEEE J. Solid-State Circuits **59**(5), 1409–1420 (2024).
7. H. Wakita, M. Nagatani, Y. Ogiso, *et al.*, "InP-Based on-Board Coherent Tx Front-End With 100-GHz Bandwidth Utilizing Flip-Chip Technology Enabling 2-Tb/s/λ Optical Transmission," J. Lightwave Technol. **43**(4), 1819–1825 (2025).
8. K. Li, D. J. Thomson, S. Liu, *et al.*, "An integrated CMOS–silicon photonics transmitter with a 112 gigabaud transmission and picojoule per bit energy efficiency," Nat. Electron. **6**(11), 910–921 (2023).
9. G. Roelkens, J. Zhang, L. Bogaert, *et al.*, "Micro-Transfer Printing for Heterogeneous Si Photonic Integrated Circuits," IEEE J. Sel. Top. Quantum Electron. **29**(3: Photon. Elec. Co-Inte. and Ad), 1–14 (2023).
10. R. Loi, J. O'Callaghan, B. Roycroft, *et al.*, "Transfer Printing of AlGaInAs/InP Etched Facet Lasers to Si Substrates," IEEE Photonics J. **8**(6), 1–10 (2016).
11. D. Guermandi, L. Bogaerts, M. Rakowski, *et al.*, "TSV-assisted Hybrid FinFET CMOS — Silicon Photonics Technology for High Density Optical I/O," in *45th European Conference on Optical Communication (ECOC 2019)*, (2019), pp. 1–4.
12. P. Ossieur, B. Moeneclaey, G. Coudyzer, *et al.*, "Integrated Photonics and Electronics for Optical Transceivers Supporting AI/ML Applications," IEEE J. Sel. Top. Quantum Electron. **31**(3: AI/ML Integrated Opto), 1–16 (2025).
13. F. Kish, V. Lal, P. Evans, *et al.*, "System-on-Chip Photonic Integrated Circuits," IEEE J. Sel. Top. Quantum Electron. **24**(1), 1–20 (2018).
14. K. Miyaguchi, Y. Ban, N. Pantano, *et al.*, "110GHz Through-Silicon Via's Integrated in Silicon Photonics Interposers for Next-Generation Optical Modules," in *2021 European Conference on Optical Communication (ECOC)*, (2021), pp. 1–4.
15. B. Corbett, R. Loi, J. O'Callaghan, *et al.*, "Transfer Printing for Silicon Photonics," in *Semiconductors and Semimetals*, vol. 99 (Elsevier, 2018), pp. 43–70.
16. D. Gomez, J. Thostenson, T. Moore, *et al.*, "Micro Transfer Printing for Micro Assembly of Heterogeneous Integrated Compound Semiconductor Components," in *International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH)*, (Monterey, CA, USA, 2022).
17. R. Loi, P. Ramaswamy, A. Farrell, *et al.*, "Micro transfer printing of electronic integrated circuits on Silicon photonics substrates," in *23rd European Conference on Integrated Optics (ECIO)*, (2022), pp. 342–344.
18. H. Li, T. Pannier, Y. Gu, *et al.*, "Electronic-Photonic Integrated Circuits through Micro-Transfer Printing," in *2025 IEEE Silicon Photonics Conference (SiPhotonics)*, (2025), pp. 1–2.
19. H. Li, T. Pannier, Y. Gu, *et al.*, "Micro-Transfer Printing of SiGe BiCMOS Electronic Chiplets on Silicon," IEEE J. Sel. Top. Quantum Electron. **32**, 1–8 (2026).

Optics EXPRESS

20. F. J. Ferraro, P. D. Heyn, M. Kim, *et al.*, "Imec Silicon Photonics Platforms: Performance Overview and Roadmap," in *Next-Generation Optical Communication: Components, Sub-Systems, and Systems XII*, vol. 12429 G. Li, K. Nakajima, and A. K. Srivastava, eds., International Society for Optics and Photonics, (SPIE, 2023), pp. 1242909.
21. H. Yu and W. Bogaerts, "An Equivalent Circuit Model of the Traveling Wave Electrode for Carrier-Depletion-Based Silicon Optical Modulators," J. Lightwave Technol. **30**(11), 1602–1609 (2012).
22. M. S. Dadash, D. Harame, and S. P. Voinigescu, "Large-Swing 22nm Si/SiGe FDSOI Stacked Cascodes for 56GBaud Drivers and 5G PAs," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, (2018), pp. 267–270.